GigaDevice Semiconductor Inc.

GD32F130xx
ARM® Cortex®-M3 32-bit MCU

Datasheet

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1. General description

The GD32F130xx device belongs to the value line of GD32 MCU family. It is a 32-bit general-purpose microcontroller based on the high performance ARM® Cortex®-M3 RISC core with best ratio in terms of processing power, reduced power consumption and peripheral set. The Cortex®-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The GD32F130xx device incorporates the ARM® Cortex®-M3 32-bit processor core operating at 72 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 64 KB on-chip Flash memory and up to 8 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer one 12-bit ADC, up to five general 16-bit timers, a general 32-bit timer, a PWM advanced timer, as well as standard and advanced communication interfaces: up to two SPIs, two I2Cs and two USARTs.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32F130xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike and so on.

2. Device overview

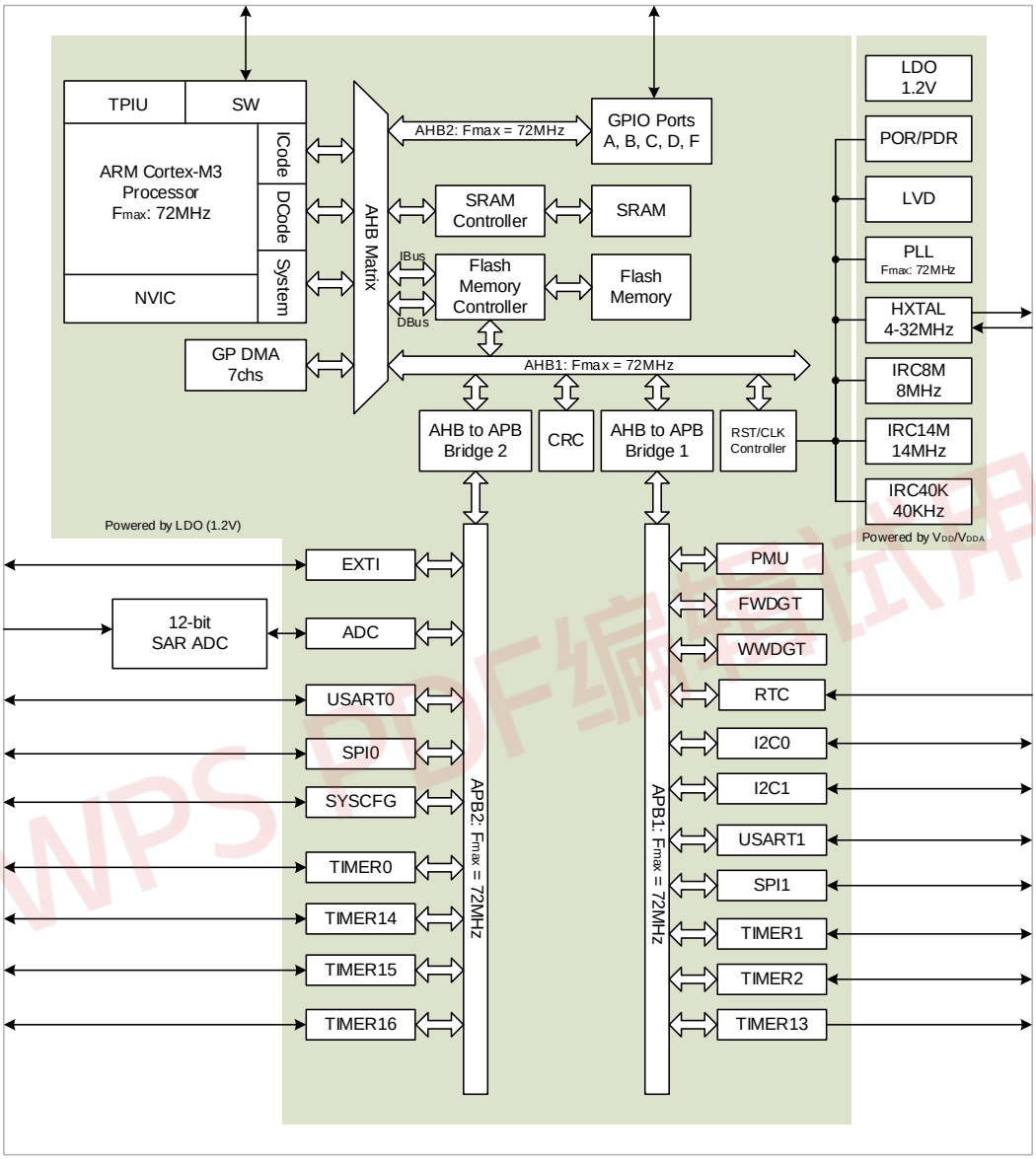
2.1. Device information

Table 2-1. GD32F130xx devices features and peripheral list

Part Number		GD32F130xx												
		F4	F6	F8	G4	G6	G8	K4	K6	K8	C4	C6	C8	R8
Flash (KB)		16	32	64	16	32	64	16	32	64	16	32	64	64
SRAM (KB)		4	4	8	4	4	8	4	4	8	4	4	8	8
Timers	General timer(32-bit)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)
	General timer(16-bit)	4 (2,13,15-16)	4 (2,13,15-16)	4 (2,13,15-16)	4 (2,13,15-16)	4 (2,13,15-16)	5 (2,13-16)	4 (2,13,15-16)	4 (2,13,15-16)	5 (2,13-16)	4 (2,13,15-16)	4 (2,13,15-16)	5 (2,13-16)	5 (2,13-16)
	Advanced timer(16-bit)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
	SysTick	1	1	1	1	1	1	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1	1	1	1	1
Connectivity	USART	1 (0)	2 (0-1)	2 (0-1)	1 (0)	2 (0-1)	2 (0-1)	1 (0)	2 (0-1)	2 (0-1)	1 (0)	2 (0-1)	2 (0-1)	2 (0-1)
	I2C	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	2 (0-1)
	SPI	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	2 (0-1)
GPIO		15	15	15	23	23	23	27	27	27	39	39	39	55
EXTI		16	16	16	16	16	16	16	16	16	16	16	16	16
ADC	Units	1	1	1	1	1	1	1	1	1	1	1	1	1
	Channels (External)	9	9	9	10	10	10	10	10	10	10	10	10	16
	Channels (Internal)	3	3	3	3	3	3	3	3	3	3	3	3	3
Package		TSSOP20			QFN28			QFN32 LQFP32			LQFP48			LQFP 64

2.2. Block diagram

Figure 2-1. GD32F130xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32F130Rx LQFP64 pinouts

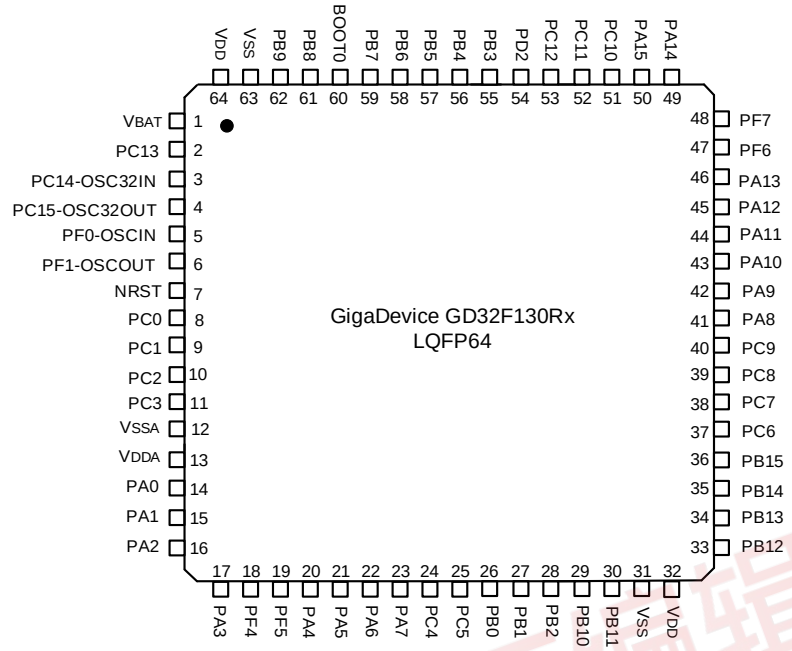


Figure 2-3. GD32F130Cx LQFP48 pinouts

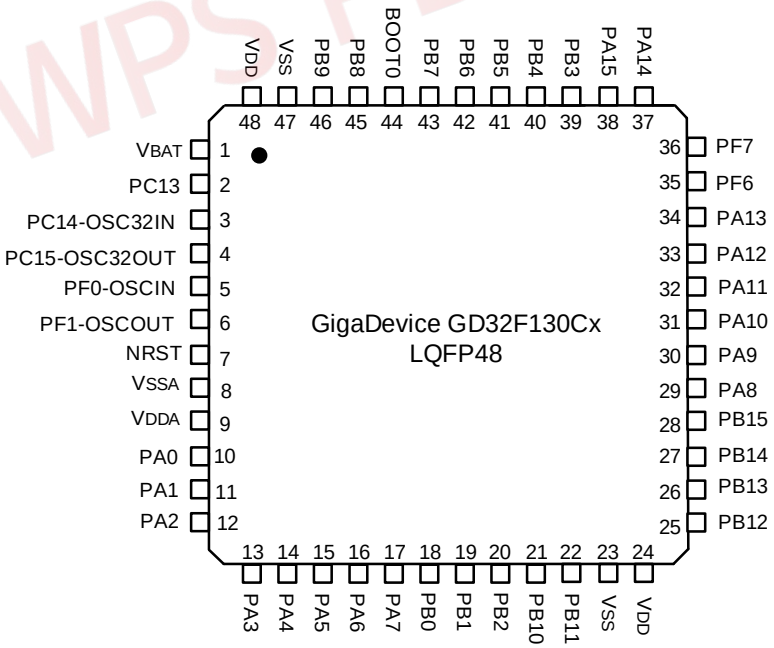


Figure 2-4. GD32F130Cx LQFP32 pinouts

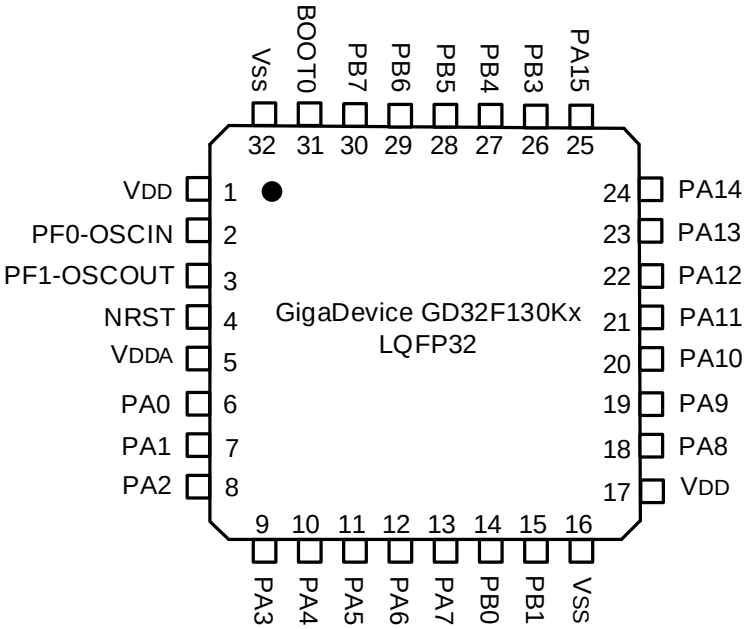


Figure 2-5. GD32F130Kx QFN32 pinouts

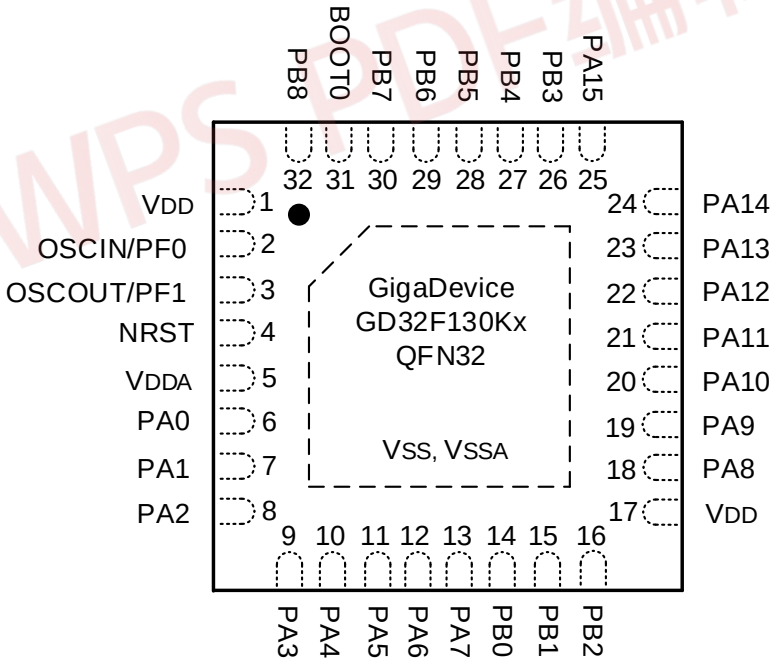


Figure 2-6. GD32F130Gx QFN28 pinouts

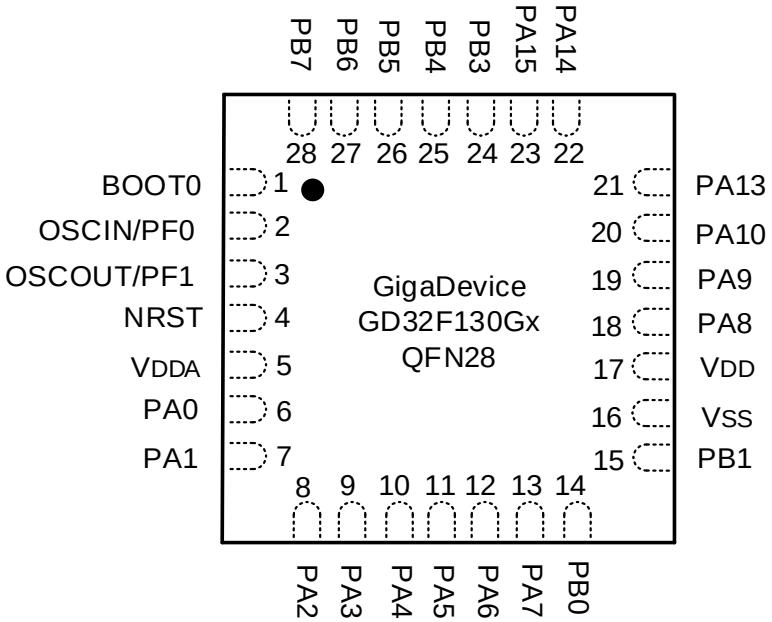
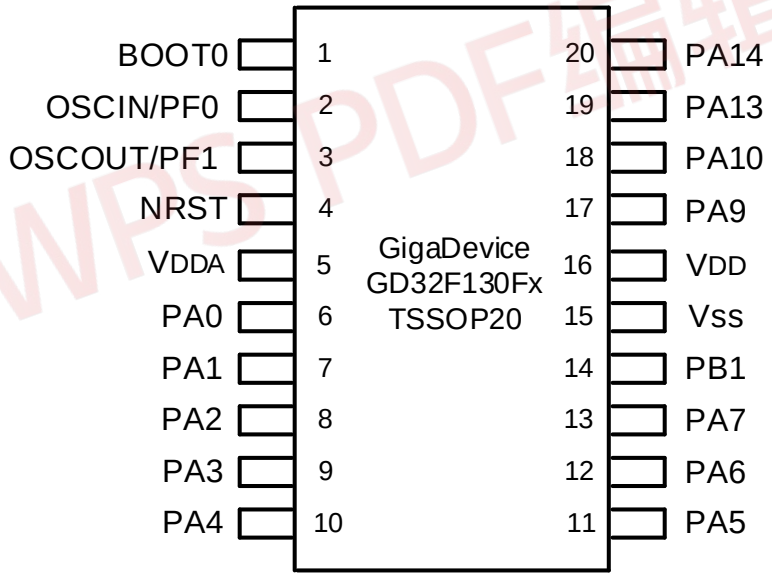


Figure 2-7. GD32F130Fx TSSOP20 pinouts



2.4. Memory map

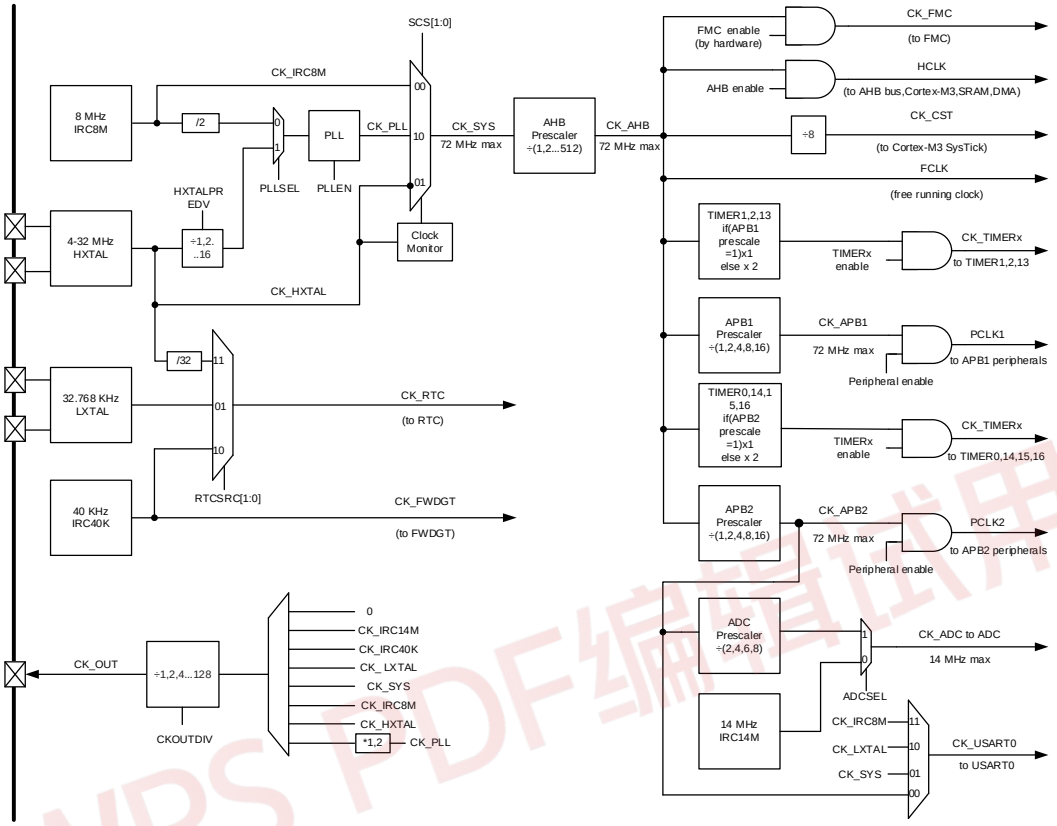
Table 2-2. GD32F130xx memory map

Pre-defined Regions	Bus	Address	Peripherals
		0xE000 0000 - 0xE00F FFFF	Cortex-M3 internal peripherals
External Device		0xA000 0000 - 0xDFFF FFFF	Reserved
External RAM		0x6000 0000 - 0x9FFF FFFF	Reserved
Peripherals	AHB1	0x5000 0000 - 0x5FFF FFFF	Reserved
	AHB2	0x4800 1800 - 0x4FFF FFFF	Reserved
		0x4800 1400 - 0x4800 17FF	GPIOF
		0x4800 1000 - 0x4800 13FF	Reserved
		0x4800 0C00 - 0x4800 0FFF	GPIOD
		0x4800 0800 - 0x4800 0BFF	GPIOC
		0x4800 0400 - 0x4800 07FF	GPIOB
		0x4800 0000 - 0x4800 03FF	GPIOA
	AHB1	0x4002 4400 - 0x47FF FFFF	Reserved
		0x4002 4000 - 0x4002 43FF	Reserved
		0x4002 3400 - 0x4002 3FFF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1400 - 0x4002 1FFF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0400 - 0x4002 0FFF	Reserved
		0x4002 0000 - 0x4002 03FF	DMA
	APB2	0x4001 4C00 - 0x4001 FFFF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER16
		0x4001 4400 - 0x4001 47FF	TIMER15
		0x4001 4000 - 0x4001 43FF	TIMER14
		0x4001 3C00 - 0x4001 3FFF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	Reserved
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	Reserved
		0x4001 2400 - 0x4001 27FF	ADC
		0x4001 0800 - 0x4001 23FF	Reserved
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	SYSCFG
	APB1	0x4000 C400 - 0x4000 FFFF	Reserved
		0x4000 C000 - 0x4000 C3FF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x4000 7C00 - 0x4000 BFFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	Reserved
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6400 - 0x4000 6FFF	Reserved
		0x4000 6000 - 0x4000 63FF	Reserved
		0x4000 5C00 - 0x4000 5FFF	Reserved
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 4800 - 0x4000 53FF	Reserved
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	Reserved
		0x4000 3800 - 0x4000 3BFF	SPI1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 1400 - 0x4000 1FFF	Reserved
		0x4000 1000 - 0x4000 13FF	Reserved
		0x4000 0800 - 0x4000 0FFF	Reserved
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM		0x2000 2000 - 0x3FFF FFFF	Reserved
		0x2000 0000 - 0x2000 1FFF	SRAM
Code		0x1FFF F810 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF F80F	Option bytes
		0x1FFF EC00 - 0x1FFF F7FF	System memory
		0x0801 0000 - 0x1FFF EBFF	Reserved
		0x0800 0000 - 0x0800 FFFF	Main Flash memory
		0x0000 0000 - 0x07FF FFFF	Aliased to Flash or system memory

2.5. Clock tree

Figure 2-8. GD32F130xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillators

IRC40K: Internal 40K RC oscillator

IRC14M: Internal 14M RC oscillators

2.6. Pin definitions

2.6.1. GD32F130R8 LQFP64 pin definitions

Table 2-3. GD32F130R8 LQFP64 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{BAT}	1	P		Default: V_{BAT}
PC13-TAMPER-RTC	2	I/O		Default: PC13 Additional: RTC_TAMP0, RTC_TS, RTC_OUT, WKUP1
PC14-OSC32IN	3	I/O		Default: PC14 Additional: OSC32IN
PC15-OSC32OUT	4	I/O		Default: PC15 Additional: OSC32OUT
PF0-OSCIN	5	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	6	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	7	I/O		Default: NRST
PC0	8	I/O		Default: PC0 Alternate: EVENTOUT Additional: ADC_IN10
PC1	9	I/O		Default: PC1 Alternate: EVENTOUT Additional: ADC_IN11
PC2	10	I/O		Default: PC2 Alternate: EVENTOUT Additional: ADC_IN12
PC3	11	I/O		Default: PC3 Alternate: EVENTOUT Additional: ADC_IN13
V_{SSA}	12	P		Default: V_{SSA}
V_{DDA}	13	P		Default: V_{DDA}
PA0-WKUP	14	I/O		Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, I2C1_SCL Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	15	I/O		Default: PA1 Alternate: USART1_RTS, TIMER1_CH1, I2C1_SDA,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				EVENTOUT Additional: ADC_IN1
PA2	16	I/O		Default: PA2 Alternate: USART1_TX, TIMER1_CH2, TIMER14_CH0 , Additional: ADC_IN2
PA3	17	I/O		Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PF4	18	I/O	5VT	Default: PF4 Alternate: SPI1_NSS, EVENTOUT
PF5	19	I/O	5VT	Default: PF5 Alternate: EVENTOUT
PA4	20	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, TIMER13_CH0, SPI1_NSS Additional: ADC_IN4
PA5	21	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5
PA6	22	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	23	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PC4	24	I/O		Default: PC4 Alternate: EVENTOUT Additional: ADC_IN14
PC5	25	I/O		Default: PC5 Additional: ADC_IN15
PB0	26	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX, EVENTOUT Additional: ADC_IN8
PB1	27	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK Additional: ADC_IN9
PB2	28	I/O	5VT	Default: PB2
PB10	29	I/O	5VT	Default: PB10 Alternate: I2C1_SCL, TIMER1_CH2

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PB11	30	I/O	5VT	Default: PB11 Alternate: I2C1_SDA, TIMER1_CH3, EVENTOUT
V_{SS}	31	P		Default: V_{SS}
V_{DD}	32	P		Default: V_{DD}
PB12	33	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, TIMER0_BRKIN, I2C1_SMBA, EVENTOUT
PB13	34	I/O	5VT	Default: PB13 Alternate: SPI1_SCK, TIMER0_CH0_ON
PB14	35	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, TIMER0_CH1_ON, TIMER14_CH0
PB15	36	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1 Additional: RTC_REFIN
PC6	37	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0
PC7	38	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1
PC8	39	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2
PC9	40	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3
PA8	41	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX, EVENTOUT
PA9	42	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL
PA10	43	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA11	44	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT
PA12	45	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT
PA13	46	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO
PF6	47	I/O	5VT	Default: PF6 Alternate: I2C1_SCL
PF7	48	I/O	5VT	Default: PF7 Alternate: I2C1_SDA

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PA14	49	I/O	5VT	Default: PA14 Alternate: USART1_TX, SWCLK, SPI1_MOSI
PA15	50	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, USART1_RX, TIMER1_CH0, TIMER1_ETI, SPI1_NSS, EVENTOUT
PC10	51	I/O	5VT	Default: PC10
PC11	52	I/O	5VT	Default: PC11
PC12	53	I/O	5VT	Default: PC12
PD2	54	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI
PB3	55	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT
PB4	56	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT
PB5	57	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
PB6	58	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	59	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON
BOOT0	60	I		Default: BOOT0
PB8	61	I/O	5VT	Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0
PB9	62	I/O	5VT	Default: PB9 Alternate: I2C0_SDA, IFRP_OUT, TIMER16_CH0, EVENTOUT
V_{SS}	63	P		Default: V_{SS}
V_{DD}	64	P		Default: V_{DD}

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.2. GD32F130Cx LQFP48 pin definitions

Table 2-4. GD32F130Cx LQFP48 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{BAT}	1	P		Default: V_{BAT}
PC13-TAMPER-RTC	2	I/O		Default: PC13 Additional: RTC_TAMP0, RTC_TS, RTC_OUT, WKUP1
PC14-OSC32IN	3	I/O		Default: PC14 Additional: OSC32IN
PC15-OSC32OUT	4	I/O		Default: PC15 Additional: OSC32OUT
PF0-OSCIN	5	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	6	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	7	I/O		Default: NRST
V_{SSA}	8	P		Default: V_{SSA}
V_{DDA}	9	P		Default: V_{DDA}
PA0-WKUP	10	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	11	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	12	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 Additional: ADC_IN2
PA3	13	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PA4	14	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	15	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PA6	16	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	17	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	18	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT Additional: ADC_IN8
PB1	19	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
PB2	20	I/O	5VT	Default: PB2
PB10	21	I/O	5VT	Default: PB10 Alternate: I2C1_SCL(5), TIMER1_CH2
PB11	22	I/O	5VT	Default: PB11 Alternate: I2C1_SDA(5), TIMER1_CH3, EVENTOUT
V_{SS}	23	P		Default: V_{SS}
V_{DD}	24	P		Default: V_{DD}
PB12	25	I/O	5VT	Default: PB12 Alternate: SPI0_NSS(3), SPI1_NSS(5), TIMER0_BRKIN, I2C1_SMBA(5), EVENTOUT
PB13	26	I/O	5VT	Default: PB13 Alternate: SPI0_SCK(3), SPI1_SCK(5), TIMER0_CH0_ON
PB14	27	I/O	5VT	Default: PB14 Alternate: SPI0_MISO(3), SPI1_MISO(5), TIMER0_CH1_ON, TIMER14_CH0
PB15	28	I/O	5VT	Default: PB15 Alternate: SPI0_MOSI(3), SPI1_MOSI(5), TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1 Additional: RTC_REFIN
PA8	29	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX(4), EVENTOUT
PA9	30	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL
PA10	31	I/O	5VT	Default: PA10

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA11	32	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT
PA12	33	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT
PA13	34	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)
PF6	35	I/O	5VT	Default: PF6 Alternate: I2C1_SCL(5), I2C0_SCL(6)
PF7	36	I/O	5VT	Default: PF7 Alternate: I2C1_SDA(5), I2C0_SCL(6)
PA14	37	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	38	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS(5), EVENTOUT
PB3	39	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT
PB4	40	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT
PB5	41	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
PB6	42	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	43	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON
BOOT0	44	I		Default: BOOT0
PB8	45	I/O	5VT	Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0,
PB9	46	I/O	5VT	Default: PB9 Alternate: I2C0_SDA, IFRP_OUT, TIMER16_CH0, EVENTOUT
V_{SS}	47	P		Default: V_{SS}
V_{DD}	48	P		Default: V_{DD}

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32F130C4 devices only.

(4) Functions are available on GD32F130C8/6 devices.

(5) Functions are available on GD32F130C8 devices.

(6) Functions are available on GD32F130C4/6 devices.

2.6.3. GD32F130Kx LQFP32 pin definitions

Table 2-5. GD32F130Kx LQFP32 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{DD}	1	P		Default: V_{DD}
PF0-OSCIN	2	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 Additional: ADC_IN2
PA3	9	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	14	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT Additional: ADC_IN8
PB1	15	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
Vss	16	P	5VT	Default: Vss
V_{DD}	17	P		Default: V_{DD}
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX(4), EVENTOUT
PA9	19	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA11	21	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT
PA12	22	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT
PA13	23	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)
PA14	24	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	25	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS(5), EVENTOUT
PB3	26	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT
PB4	27	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT
PB5	28	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
PB6	29	I/O	5VT	Default: PB6

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	30	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON
BOOT0	31	I		Default: BOOT0
Vss	32	P		Default: Vss

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32F130K4 devices only.

(4) Functions are available on GD32F130K8/6 devices.

(5) Functions are available on GD32F130K8 devices.

2.6.4. GD32F130Kx QFN32 pin definitions

Table 2-6. GD32F130Kx QFN32 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{DD}	1	P		Default: V_{DD}
PF0-OSCIN	2	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 Additional: ADC_IN2
PA3	9	I/O		Default: PA3

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	14	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT Additional: ADC_IN8
PB1	15	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
PB2	16	I/O	5VT	Default: PB2
V_{DD}	17	P		Default: V_{DD}
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX(4), EVENTOUT
PA9	19	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA11	21	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT
PA12	22	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT
PA13	23	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PA14	24	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	25	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS(5), EVENTOUT
PB3	26	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT
PB4	27	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT
PB5	28	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
PB6	29	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	30	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON
BOOT0	31	I		Default: BOOT0
PB8	32	I/O	5VT	Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0

Notes:

(6) Type: I = input, O = output, P = power.

(7) I/O Level: 5VT = 5 V tolerant.

(8) Functions are available on GD32F130K4 devices only.

(9) Functions are available on GD32F130K8/6 devices.

(10) Functions are available on GD32F130K8 devices.

2.6.5. GD32F130Gx QFN28 pin definitions

Table 2-7. GD32F130Gx QFN28 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
BOOT0	1	I		Default: BOOT0
PF0-OSCIN	2	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 Additional: ADC_IN2
PA3	9	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	14	I/O		Default: PB0

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT Additional: ADC_IN8
PB1	15	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
V_{SS}	16	P		Default: V_{SS}
V_{DD}	17	P		Default: V_{DD}
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX(4), EVENTOUT
PA9	19	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN , I2C0_SCL
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA13	21	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)
PA14	22	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	23	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS(5), EVENTOUT
PB3	24	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT
PB4	25	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT
PB5	26	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
PB6	27	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	28	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32F130G4 devices only.

(4) Functions are available on GD32F130G8/6 devices.

(5) Functions are available on GD32F130G8 devices.

2.6.6. GD32F130Fx TSSOP20 pin definitions

Table 2-8. GD32F130Fx TSSOP20 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
BOOT0	1	I		Default: BOOT0
PF0-OSCIN	2	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 Additional: ADC_IN2
PA3	9	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB1	14	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
V_{SS}	15	P		Default: V_{SS}
V_{DD}	16	P		Default: V_{DD}
PA9	17	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL
PA10	18	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA13	19	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)
PA14	20	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32F130F4 devices only.

(4) Functions are available on GD32F130F8/6 devices.

(5) Functions are available on GD32F130F8 devices.

2.6.7. GD32F130xx pin alternate functions

Table 2-9. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PA0		USART0_CTS(1) USART1_CTS(2)	TIMER1_CH0 TIMER1_ETI		I2C1_SCL(3)		
PA1	EVENTOUT	USART0_RTS(1) USART1_RTS(2)	TIMER1_CH1		I2C1_SDA(3)		
PA2	TIMER14_CH0	USART0_TX(1) USART1_TX(2)	TIMER1_CH2				
PA3	TIMER14_CH1	USART0_RX(1) USART1_RX(2)	TIMER1_CH3				
PA4	SPI0_NSS	USART0_CK(1) USART1_CK(2)			TIMER13_CH0		SPI1_NSS(3)
PA5	SPI0_SCK		TIMER1_CH0 TIMER1_ETI				
PA6	SPI0_MISO	TIMER2_CH0	TIMER0_BRKIN			TIMER15_CH0	EVENTOUT
PA7	SPI0_MOSI	TIMER2_CH1	TIMER0_CH0_ON		TIMER13_CH0	TIMER16_CH0	EVENTOUT
PA8	CK_OUT	USART0_CK	TIMER0_CH0	EVENTOUT	USART1_TX(2)		
PA9	TIMER14_BRKIN	USART0_TX	TIMER0_CH1		I2C0_SCL		
PA10	TIMER16_BRKIN	USART0_RX	TIMER0_CH2		I2C0_SDA		
PA11	EVENTOUT	USART0_CTS	TIMER0_CH3				
PA12	EVENTOUT	USART0_RTS	TIMER0_ETI				
PA13	SWDIO	IFRP_OUT					SPI1_MISO(3)
PA14	SWCLK	USART0_TX(1) USART1_TX(2)					SPI1_MOSI(3)
PA15	SPI0_NSS	USART0_RX(1) USART1_RX(2)	TIMER1_CH0 TIMER1_ETI	EVENTOUT			SPI1_NSS(3)

Notes:

(1) Functions are available on GD32F130x4 devices only.

(2) Functions are available on GD32F130x8/6 devices.

(3) Functions are available on GD32F130x8 devices.

Table 2-10. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PB0	EVENTOUT	TIMER2_CH2	TIMER0_CH1_ON		USART1_RX(2)		
PB1	TIMER13_CH0	TIMER2_CH3	TIMER0_CH2_ON				SPI1_SCK(3)
PB2							
PB3	SPI0_SCK	EVETOUT	TIMER1_CH1				
PB4	SPI0_MISO	TIMER2_CH0	EVENTOUT				
PB5	SPI0_MOSI	TIMER2_CH1	TIMER15_BRKIN	I2C0_SMBA			
PB6	USART0_TX	I2C0_SCL	TIMER15_CH0_ON				
PB7	USART0_RX	I2C0_SDA	TIMER16_CH0_ON				
PB8		I2C0_SCL	TIMER15_CH0				
PB9	IFRP_OUT	I2C0_SDA	TIMER16_CH0	EVENTOUT			
PB10		I2C1_SCL(3)	TIMER1_CH2				
PB11	EVENTOUT	I2C1_SDA(3)	TIMER1_CH3				
PB12	SPI0_NSS(1) SPI1_NSS(3)	EVENTOUT	TIMER0_BRKIN		I2C1_SMBA(3)		
PB13	SPI0_SCK(1) SPI1_SCK(3)		TIMER0_CH0_ON				
PB14	SPI0_MISO(1) SPI1_MISO(3)	TIMER14_CH0	TIMER0_CH1_ON				
PB15	SPI0_MOSI(1) SPI1_MOSI(3)	TIMER14_CH1	TIMER0_CH2_ON	TIMER14_CH0_ON			

Notes:

(1) Functions are available on GD32F130x4 devices only.

(2) Functions are available on GD32F130x8/6 devices.

(3) Functions are available on GD32F130x8 devices.

Table 2-11. Port C & D & F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PC0	EVENTOUT						
PC1	EVENTOUT						
PC2	EVENTOUT						
PC3	EVENTOUT						
PC4	EVENTOUT						
PC6	TIMER2_CH0						
PC7	TIMER2_CH1						
PC8	TIMER2_CH2						
PC9	TIMER2_CH3						
PD2	TIMER2_ETI						
PF4	SPI1_NSS,EVENTOUT						
PF5	EVENTOUT						
PF6	I2C0_SCL(1) I2C1_SCL(2)						
PF7	I2C0_SDA(1) I2C1_SDA(2)						

Notes:

(1) Functions are available on GD32F130x4/6 devices.

(2) Functions are available on GD32F130x8 devices only.

3. Functional description

3.1. ARM® Cortex®-M3 core

The Cortex®-M3 processor is the latest generation of ARM® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

- 32-bit ARM® Cortex®-M3 processor core
- Up to 72 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

3.2. On-chip memory

- Up to 64 Kbytes of Flash memory
- Up to 8 Kbytes of SRAM with hardware parity checking

The ARM® Cortex®-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 64 Kbytes of inner Flash and 8 Kbytes of inner SRAM at most is available for storing programs and data, both accessed (R/W) at CPU clock speed with zero wait states. The ***Table 2-2. GD32F130xx memory map*** shows the memory map of the GD32F130xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator

- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB and two APB domains is 72 MHz. See ***Figure 2-8. GD32F130xx clock tree*** for details on the clock tree.

GD32F1x0 Reset Control includes the control of three kinds of reset: power reset, system reset and backup domain reset. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller and the Backup domain. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.6 V and down to 1.8V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a wake up message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10) or USART1 (PA2 and PA3, PA14 and PA15).

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance

between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, the RTC tamper and Timestamp, the USART0 wakeup and the CEC wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.
- **Standby** mode
  In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except Backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pin.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC engine with up to 1 MSPS conversion rate
- Input voltage range: V_{SSA} to V_{DDA} (2.6 to 3.6 V)
- Temperature sensor

One 12-bit 1 μs multi-channel ADCs are integrated in the device. It is a total of up to 16 multiplexed external channels and 3 internal channels for temperature sensor, voltage reference, V_{BAT} voltage measurement. The conversion range is between 2.6 V < V_{DDA} < 3.6 V. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages. The ADC can be triggered from the events generated by the general timers (TIMERx=1,2,14) and the advanced timers (TIMER0) with internal connection.

The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value. Each device is factory-calibrated to improve the accuracy and the calibration data are stored in the system memory area.

3.7. DMA

- 7 channel DMA controller
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.8. General-purpose inputs/outputs (GPIOs)

- Up to 55 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 55 general purpose I/O pins (GPIO) in GD32F130xx, named PA0 ~ PA15 and PB0 ~ PB15, PC0 ~ PC15, PD2, PF0, PF1, PF4-PF7 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.9. Timers and PWM generation

- One 16-bit advanced timer (TIMER0), one 32-bit general timer (TIMER1), five 16-bit general timers (TIMER2, TIMER13 ~ TIMER16)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, compare match output, generation of PWM waveform (edge-aligned and center-aligned Mode) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other

general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER13 ~ TIMER16 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The GD32F130xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler, It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in stop and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wake up interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.10. Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with five 32-bit backup registers
- Calendar with subsecond, seconds, minutes, hours, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 1 ppm resolution for compensation of quartz crystal inaccuracy

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from

external crystal oscillator.

3.11. Inter-integrated circuit (I2C)

- Up to two I2Cs bus interfaces can support both master and slave mode with a frequency up to 400 KHz
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides transfer rate of up to 100 KHz in standard mode and up to 400 KHz in fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.12. Serial peripheral interface (SPI)

- Up to two SPIs interfaces with a frequency of up to 18 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.13. Universal synchronous asynchronous receiver transmitter (USART)

- Up to two USARTs with operating frequency up to 9 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous

transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.14. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.15. Package and operation temperature

- LQFP64 (GD32F130Rx), LQFP48 (GD32F130Cx), LQFP32 (GD32F130Kx), QFN32 (GD32F130Kx), QFN28 (GD32F130Gx) and TSSOP20 (GD32F130Fx)
- Operation temperature range: -40°C to +85°C (industrial level)

4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin	V_{SS} - 0.3	V_{DD} + 4.0	V
	Input voltage on other I/O	V_{SS} - 0.3	4.0	V
I_{IO}	Maximum current for GPIO pins	—	25	mA
T_A	Operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C

4.2. Recommended DC characteristics

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	—	2.6	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.6	3.3	3.6	V
V_{BAT}	Battery supply voltage	—	1.8	—	3.6	V

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-3. Power consumption characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current (Run mode)	V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, System clock=48 MHz, All peripherals enabled	—	17.26	—	mA
		V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, System clock =48 MHz, All peripherals disabled	—	12.23	—	mA
		V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, System clock =24 MHz, All peripherals enabled	-—	9.26	—	mA
		V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, System Clock =24 MHz, All peripherals disabled	—	6.75	—	mA
	Supply current (Sleep mode)	V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, CPU clock off, System clock =48 MHz, All peripherals enabled	—	9.76	—	mA
		V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, CPU clock off, System clock =48 MHz, All peripherals disabled	—	3.89	—	mA
	Supply current (Deep-Sleep mode)	V_{DD}=V_{BAT}=3.3V, Regulator in run mode, IRC40K on, RTC on, All GPIOs analog mode	—	155.14	—	µA
		V_{DD}=V_{BAT}=3.3V, Regulator in low power mode, IRC40K on, RTC on, All GPIOs analog mode	—	143.17	—	µA
	Supply current (Standby mode)	V_{DD}=V_{BAT}=3.3V, LXTAL off, IRC40K on, RTC on	—	7.38	—	µA
		V_{DD}=V_{BAT}=3.3V, LXTAL off, IRC40K on, RTC off	—	6.94	—	µA
		V_{DD}=V_{BAT}=3.3V, LXTAL off, IRC40K off, RTC off	—	5.74	—	µA
I_{BAT}	Battery supply current	V_{DD} not available, V_{BAT}=3.6 V, LXTAL on with external crystal, RTC on, Higher driving	—	3.08	—	µA
		V_{DD} not available, V_{BAT}=3.3 V, LXTAL on with external crystal, RTC on, Higher driving	—	2.78	—	µA
		V_{DD} not available, V_{BAT}=2.6 V, LXTAL on with external crystal, RTC on, Higher driving	—	2.12	—	µA
		V_{DD} not available, V_{BAT}=3.6 V, LXTAL on with external crystal, RTC on, Lower driving	—	1.37	—	µA
		V_{DD} not available, V_{BAT}=3.3 V, LXTAL on with external crystal, RTC on, Lower driving	—	1.25	—	µA
		V_{DD} not available, V_{BAT}=2.6 V, LXTAL on with external crystal, RTC on, Lower driving	—	1.05	—	µA

4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the ***Table 4-4. EMS characteristics***, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-4. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C conforms to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	V_{DD} = 3.3 V, T_A = +25 °C conforms to IEC 61000-4-4	4A

EMI (Electromagnetic Interference) emission testing result is given in the ***Table 4-5. EMI characteristics***, compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 4-5. EMI characteristics

Symbol	Parameter	Conditions	Tested frequency band	Conditions		Unit
				24M	48M	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = +25 °C, compliant with IEC 61967-2	0.1 to 2 MHz	<0	<0	dBµV
			2 to 30 MHz	-3.9	-2.8	
			30 to 130 MHz	-7.2	-8	
			130 MHz to 1GHz	-7	-7	

4.5. Power supply supervisor characteristics

Table 4-6. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold	PDR_S=0	2.32	2.40	2.48	V
V_{PDR}	Power down reset threshold		2.27	2.35	2.43	V
V_{HYST}	PDR hysteresis		—	0.05	—	V
$T_{RSTTEMP}$	Reset temporization		—	2	—	ms
V_{POR}	Power on reset threshold	PDR_S=1	2.32	2.40	2.48	V
V_{PDR}	Power down reset threshold		1.72	1.80	1.88	V
V_{HYST}	PDR hysteresis		—	0.6	—	V
$T_{RSTTEMP}$	Reset temporization		—	2	—	ms

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-7. ESD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25 °C; JESD22-A114	—	—	5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=25 °C; JESD22-C101	—	—	500	V

Table 4-8. Static latch-up characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A=25 °C; JESD78	—	—	±100	mA
	V_{supply} over voltage		—	—	5.4	V

4.7. External clock characteristics

Table 4-9. High speed crystal oscillator (HXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	High Speed crystal oscillator (HXTAL) frequency	V_{DD}=3.3V	4	8	32	MHz
C_{HXTAL}	Recommended load capacitance on OSCIN and OSCOUT	—	—	20	30	pF
R_{FHXTAL}	Recommended external feedback resistor between XTALIN and XTALOUT	—	—	200	—	KΩ
D_{HXTAL}	HXTAL oscillator duty cycle	—	48	50	52	%
$I_{DDHXTAL}$	HXTAL oscillator operating current	V_{DD}=3.3V, T_A=25°C	—	1.4	—	μA
$t_{SUHXTAL}$	HXTAL oscillator startup time	V_{DD}=3.3V, T_A=25°C	—	2	—	ms

Table 4-10. Low speed crystal oscillator (LXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Low Speed crystal oscillator (LXTAL) frequency	V_{DD}=V_{BAT}=3.3V	—	32.768	1000	KHz
C_{LXTAL}	Recommended load capacitance on OSC32IN and OSC32OUT	—	—	—	15	pF
D_{LXTAL}	LXTAL oscillator duty cycle	—	48	50	52	%
$I_{DDLXTAL}$	LXTAL oscillator operating current	V_{DD}=V_{BAT}=3.3V	—	1.4	—	µA
$t_{SULXTAL}$	LXTAL oscillator startup time	V_{DD}=V_{BAT}=3.3V	—	3	—	s

4.8. Internal clock characteristics

Table 4-11. Internal 8 MHz RC oscillator (IRC8M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	Internal 8 MHz RC oscillator (IRC8M) frequency	V_{DD}=3.3V	—	8	—	MHz
ACC_{IRC8M}	IRC8M oscillator Frequency accuracy, Factory-trimmed	V_{DD}=3.3V, T_A=-40°C ~+105°C	-2.5	—	+1.5	%
		V_{DD}=3.3V, T_A=0°C ~ +85°C	-1.2	—	+1.2	%
		V_{DD}=3.3V, T_A=25°C	-1	—	+1	%
D_{IRC8M}	IRC8M oscillator duty cycle	V_{DD}=3.3V, f_{IRC8M}=8MHz	48	50	52	%
$I_{DDIRC8M}$	IRC8M oscillator operating current	V_{DD}=3.3V, f_{IRC8M}=8MHz	—	80	100	µA
$t_{SUIRC8M}$	IRC8M oscillator startup time	V_{DD}=3.3V, f_{IRC8M}=8MHz	1	—	2	us

Table 4-12. Internal 40KHz RC oscillator (IRC40K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC40K}	Internal 40KHz RC oscillator (IRC40K) frequency	V_{DD}=V_{BAT}=3.3V, T_A=-40°C ~ +85°C	30	40	60	KHz
$I_{DDIRC40K}$	IRC40K oscillator operating current	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	1	2	µA
$t_{SUIRC40K}$	IRC40K oscillator startup time	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	—	80	µs

4.9. PLL characteristics

Table 4-13. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency		1	8	25	MHz
f_{PLL}	PLL output clock frequency		16	—	72	MHz
t_{LOCK}	PLL lock time		—		200	μs
$Jitter_{PLL}$	Cycle to cycle Jitter				300	ps

4.10. Memory characteristics

Table 4-14. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A=-40°C ~ +85°C	100	—	—	kcycles
t_{RET}	Data retention time	T_A=125°C	20	—	—	years
t_{PROG}	Word programming time	T_A=-40°C ~ +85°C	200	—	400	us
t_{ERASE}	Page erase time	T_A=-40°C ~ +85°C	60	100	450	ms
t_{MERASE}	Mass erase time	T_A=-40°C ~ +85°C	3.2	—	9.6	s

4.11. GPIO characteristics

Table 4-15. I/O port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage	V_{DD}=2.6V	-0.3	—	0.95	V
	5V-tolerant IO Low level input voltage	V_{DD}=2.6V	-0.3	—	0.9	V
V_{IH}	Standard IO High level input voltage	V_{DD}=2.6V	1.2	—	4.0	V
	5V-tolerant IO High level input voltage	V_{DD}=2.6V	1.5	—	5.5	V
V_{OL}	Low level output voltage	V_{DD}=2.6V	—	—	0.2	V
V_{OH}	High level output voltage	V_{DD}=2.6V	2.3	—	—	V
R_{PU}	Internal pull-up resistor	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Internal pull-down resistor	V_{IN}=V_{DD}	30	40	50	kΩ

4.12. ADC characteristics

Table 4-16. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage		2.6	3.3	3.6	V
V_{IN}	ADC input voltage range		0	—	V_{DDA}	V
f_{ADC}	ADC clock		0.6	—	14	MHz
f_S	Sampling rate		—	—	1	MHz
$f_{ADCCONV}$	ADC conversion time	f_{ADC} =14MHz	1	—	18	μs
R_{ADC}	Input sampling switch resistance		—	—	0.2	kΩ
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	—	32	—	pF
t_{SU}	Startup time		—	—	1	μs

4.13. SPI characteristics

Table 4-17. Standard SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency		—	—	18	MHz
$t_{SCK(H)}$	SCK clock high time		19	—	—	ns
$t_{SCK(L)}$	SCK clock low time		19	—	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time		—	—	25	ns
$t_{H(MO)}$	Data output hold time		2	—	—	ns
$t_{SU(MI)}$	Data input setup time		5	—	—	ns
$t_{H(MI)}$	Data input hold time		5	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	f_{PCLK}=54MHz	74	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	f_{PCLK}=54MHz	37	—	—	ns
$t_{A(SO)}$	Data output access time	f_{PCLK}=54MHz	0	—	55	ns
$t_{DIS(SO)}$	Data output disable time		3	—	10	ns
$t_{V(SO)}$	Data output valid time		—	—	25	ns
$t_{H(SO)}$	Data output hold time		15	—	—	ns
$t_{SU(SI)}$	Data input setup time		5	—	—	ns
$t_{H(SI)}$	Data input hold time		4	—	—	ns

4.14. I2C characteristics

Table 4-18. I2C characteristics

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	KHz
$t_{SCL(H)}$	SCL clock high time		4.0	—	0.6	—	ns
$t_{SCL(L)}$	SCL clock low time		4.7	—	1.3	—	ns

5. Package information

5.1. TSSOP package outline dimensions

Figure 5-1. TSSOP package outline

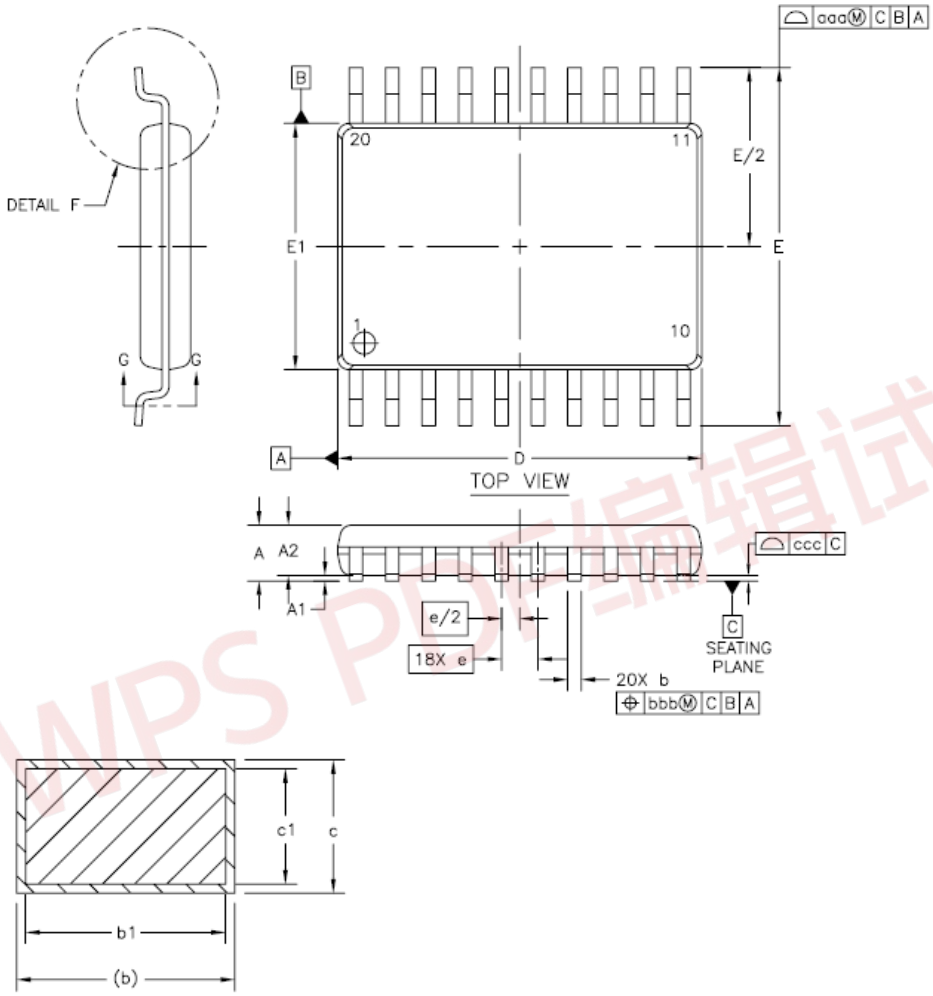


Table 5-1. TSSOP20 package dimensions

Symbol	Dimensions (mm)			Symbol	Dimensions (mm)		
	Min	Typ	Max		Min	Typ	Max
A	-	-	1.2	c1	0.09	-	0.16
A1	0.05	-	1.15	D	6.4	6.5	6.6
A2	0.80	1.00	1.05	E1	4.3	4.4	4.5
b	0.19	-	0.30	E	6.40		
B1	0.19	0.22	0.25	e	0.65		
c	0.09	-	0.20	L	0.45	0.6	0.75

5.2. QFN package outline dimensions

Figure 5-2. QFN package outline

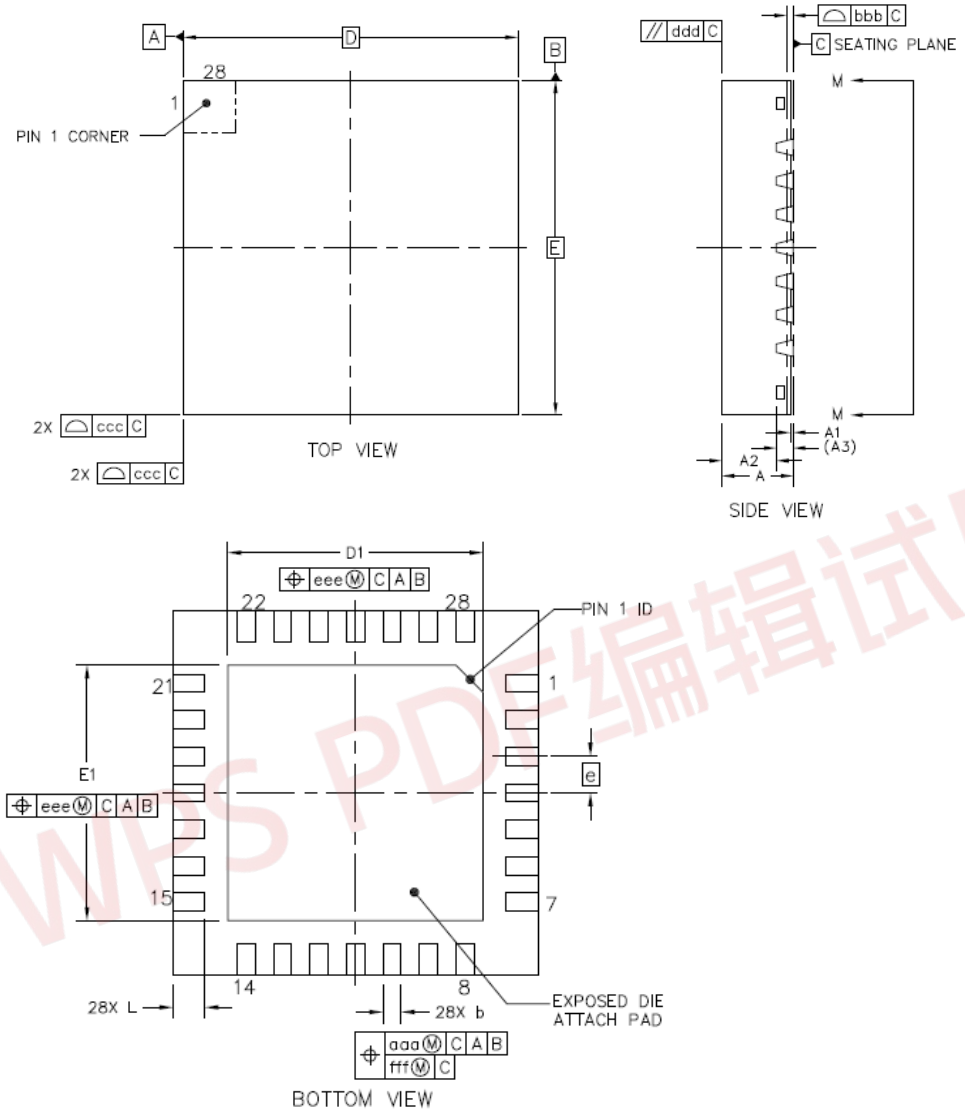


Table 5-2. QFN package dimensions

Symbol	QFN28			QFN32		
	Min	Typ	Max	Min	Typ	Max
A	0.8	0.85	0.9	0.8	0.85	0.9
A1	0	0.035	0.05	0	0.035	0.05
A2	-	0.65	0.67	-	0.65	0.67
A3	-	0.203	-	-	0.203	-
D	-	4.0	-	-	5.0	-
E	-	4.0	-	-	5.0	-
D1	2.7	2.8	2.9	3.4	3.5	3.6
E1	2.7	2.8	2.9	3.4	3.5	3.6
L	0.25	0.35	0.45	0.3	0.4	0.5
e	0.4			0.5		
b	0.15	0.2	0.25	0.2	0.25	0.3

(Original dimensions are in millimeters)

5.3. LQFP package outline dimensions

Figure 5-3. LQFP package outline

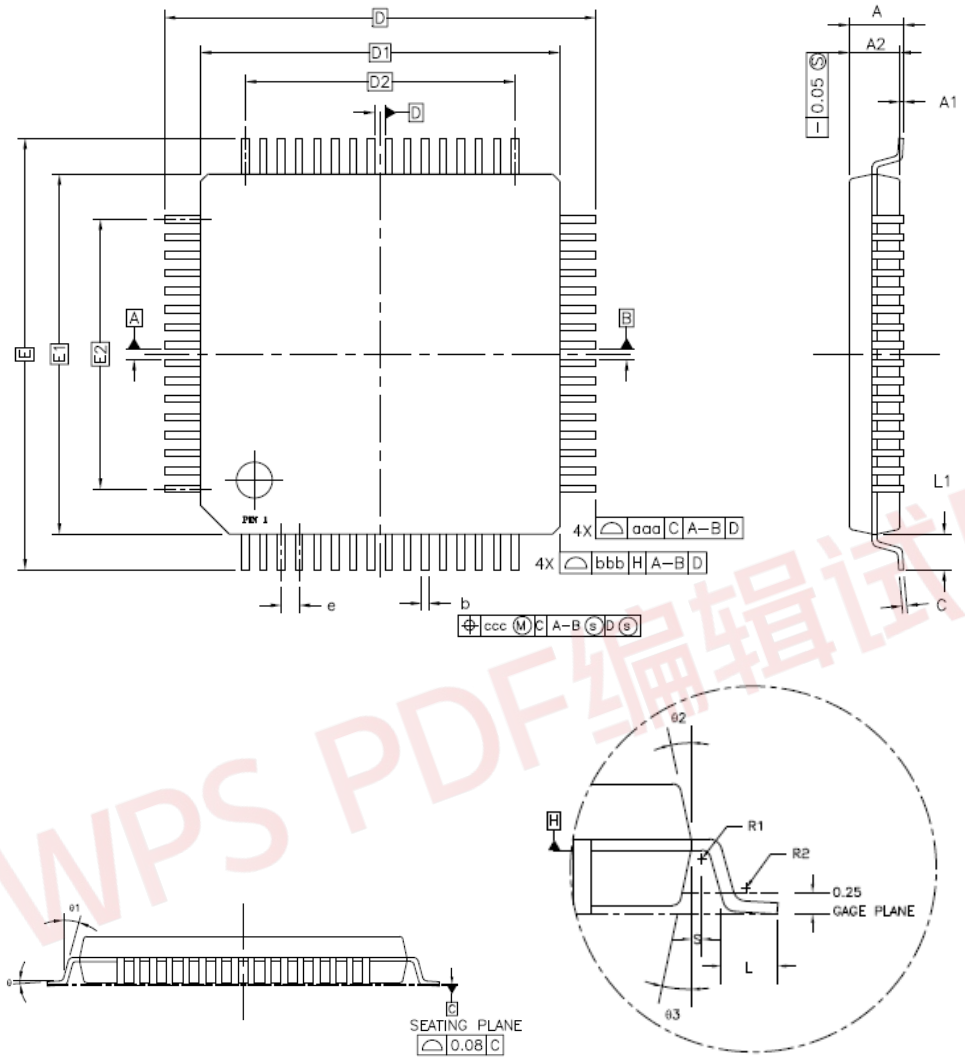


Table 5-3. LQFP package dimensions

Symbol	LQFP32			LQFP48			LQFP64		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	1.50	-	-	1.60
A1	0.05	-	0.25	0.05	-	0.15	0.05	-	0.15
A2	1.35	1.40	1.45	0.95	1.00	1.35	1.35	1.40	1.45
D	-	9.00	-	-	9.00	-	-	12.00	-
D1	-	7.00	-	-	7.00	-	-	10.00	-
E	-	9.00	-	-	9.00	-	-	12.00	-
E1	-	7.00	-	-	7.00	-	-	10.00	-
R1	0.08	-	-	0.08	-	-	0.08	-	-
R2	0.08	-	0.20	0.08	-	0.20	0.08	-	0.20
θ	0°	3.5°	7°	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-	0°	-	-
θ2	11°	12°	13°	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°	11°	12°	13°
c	0.09	-	0.20	0.09	-	0.20	0.09	-	0.20
L	0.45	0.60	0.75	0.45	0.60	0.75	0.45	0.60	0.75
L1	-	1.00	-	-	1.00	-	-	1.00	-
S	0.20	-	-	0.20	-	-	0.20	-	-
b	0.17	0.22	0.27	0.17	0.22	0.27	0.17	0.20	0.27
e	-	0.50	-	-	0.50	-	-	0.50	-
D2	-	5.50	-	-	5.50	-	-	7.50	-
E2	-	5.50	-	-	5.50	-	-	7.50	-
aaa	0.20			0.20			0.20		
bbb	0.20			0.20			0.20		
ccc	0.08			0.08			0.08		

(Original dimensions are in millimeters)

6. Ordering information

Table 6-1. Part ordering code for GD32F130xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F130F4P6	16	TSSOP20	Green	Industrial -40°C to +85°C
GD32F130F6P6	32	TSSOP20	Green	Industrial -40°C to +85°C
GD32F130F8P6	64	TSSOP20	Green	Industrial -40°C to +85°C
GD32F130G4U6	16	QFN28	Green	Industrial -40°C to +85°C
GD32F130G6U6	32	QFN28	Green	Industrial -40°C to +85°C
GD32F130G8U6	64	QFN28	Green	Industrial -40°C to +85°C
GD32F130K4U6	16	QFN32	Green	Industrial -40°C to +85°C
GD32F130K6U6	32	QFN32	Green	Industrial -40°C to +85°C
GD32F130K8U6	64	QFN32	Green	Industrial -40°C to +85°C
GD32F130K4T6	16	LQFP32	Green	Industrial -40°C to +85°C
GD32F130K6T6	32	LQFP32	Green	Industrial -40°C to +85°C
GD32F130K8T6	64	LQFP32	Green	Industrial -40°C to +85°C
GD32F130C4T6	16	LQFP48	Green	Industrial -40°C to +85°C
GD32F130C6T6	32	LQFP48	Green	Industrial -40°C to +85°C
GD32F130C8T6	64	LQFP48	Green	Industrial -40°C to +85°C
GD32F130R8T6	64	LQFP64	Green	Industrial -40°C to +85°C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.8, 2014
1.1	Characteristics values updated in ***Table 4-3. Power consumption characteristics***	Oct.20, 2014
2.0	Characteristics of QFN32 package added in ***Table 2-3. GD32F130R8 LQFP64 pin definitions*** and ***Table 5-2. QFN package dimensions***	Jan 15, 2015
2.1	Characteristics of TSSOP20 package added in ***Table 2-1. GD32F130xx devices features and peripheral list***	Apr 24, 2016
3.0	Adapt To New Name Convention	Jan.24, 2018
3.1	Add LQFP32 Package	Apr.24, 2018

GigaDevice Semiconductor Inc.

GD32F130xx
ARM® Cortex®-M3 32-bit MCU

Datasheet

Table of Contents

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1. General description

The GD32F130xx device belongs to the value line of GD32 MCU family. It is a 32-bit general-purpose microcontroller based on the high performance ARM® Cortex®-M3 RISC core with best ratio in terms of processing power, reduced power consumption and peripheral set. The Cortex®-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The GD32F130xx device incorporates the ARM® Cortex®-M3 32-bit processor core operating at 72 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 64 KB on-chip Flash memory and up to 8 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer one 12-bit ADC, up to five general 16-bit timers, a general 32-bit timer, a PWM advanced timer, as well as standard and advanced communication interfaces: up to two SPIs, two I2Cs and two USARTs.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32F130xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike and so on.

2. Device overview

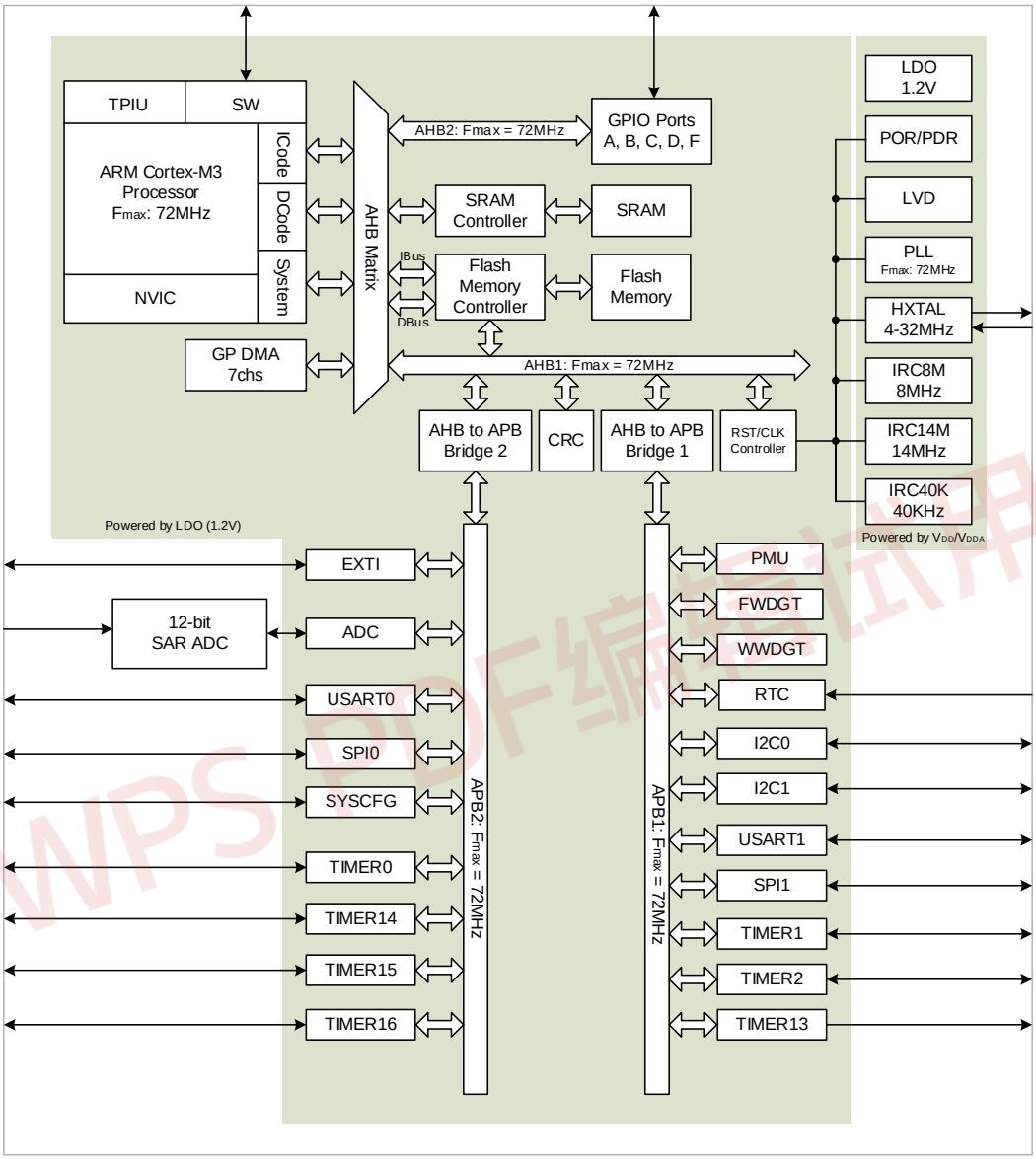
2.1. Device information

Table 2-1. GD32F130xx devices features and peripheral list

Part Number		GD32F130xx												
		F4	F6	F8	G4	G6	G8	K4	K6	K8	C4	C6	C8	R8
Flash (KB)		16	32	64	16	32	64	16	32	64	16	32	64	64
SRAM (KB)		4	4	8	4	4	8	4	4	8	4	4	8	8
Timers	General timer(32-bit)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)
	General timer(16-bit)	4 (2,13,15-16)	4 (2,13,15-16)	4 (2,13,15-16)	4 (2,13,15-16)	4 (2,13,15-16)	5 (2,13-16)	4 (2,13,15-16)	4 (2,13,15-16)	5 (2,13-16)	4 (2,13,15-16)	4 (2,13,15-16)	5 (2,13-16)	5 (2,13-16)
	Advanced timer(16-bit)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
	SysTick	1	1	1	1	1	1	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1	1	1	1	1
Connectivity	USART	1 (0)	2 (0-1)	2 (0-1)	1 (0)	2 (0-1)	2 (0-1)	1 (0)	2 (0-1)	2 (0-1)	1 (0)	2 (0-1)	2 (0-1)	2 (0-1)
	I2C	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	2 (0-1)
	SPI	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	2 (0-1)
GPIO		15	15	15	23	23	23	27	27	27	39	39	39	55
EXTI		16	16	16	16	16	16	16	16	16	16	16	16	16
ADC	Units	1	1	1	1	1	1	1	1	1	1	1	1	1
	Channels (External)	9	9	9	10	10	10	10	10	10	10	10	10	16
	Channels (Internal)	3	3	3	3	3	3	3	3	3	3	3	3	3
Package		TSSOP20			QFN28			QFN32 LQFP32			LQFP48			LQFP 64

2.2. Block diagram

Figure 2-1. GD32F130xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32F130Rx LQFP64 pinouts

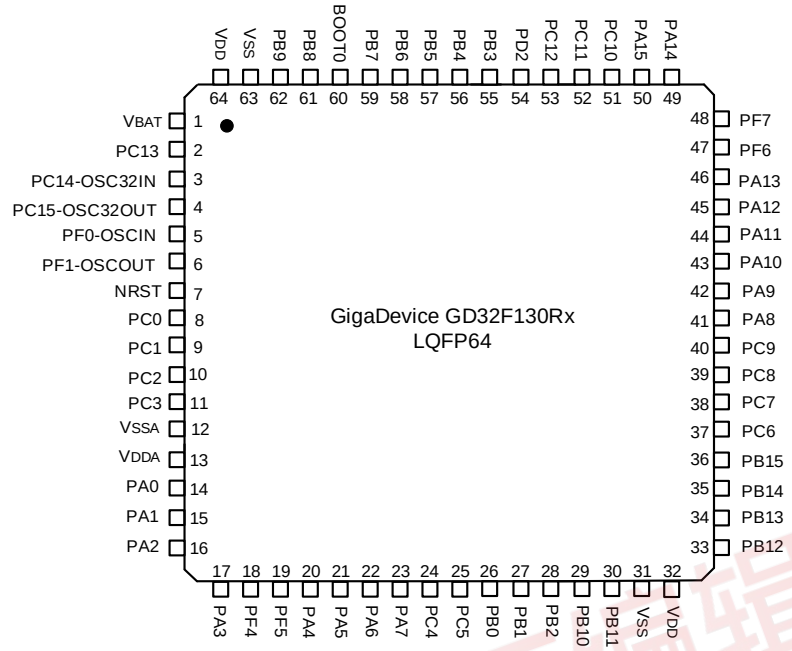


Figure 2-3. GD32F130Cx LQFP48 pinouts

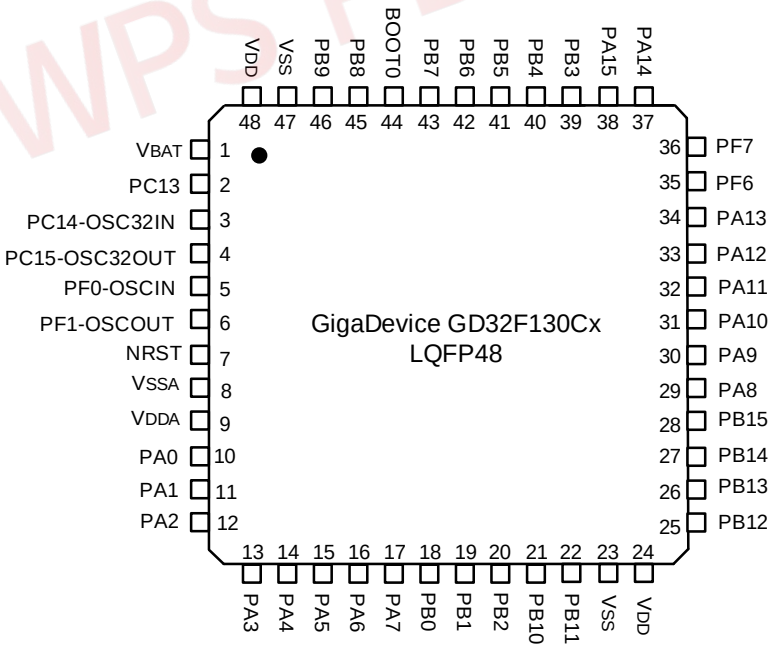


Figure 2-4. GD32F130Cx LQFP32 pinouts

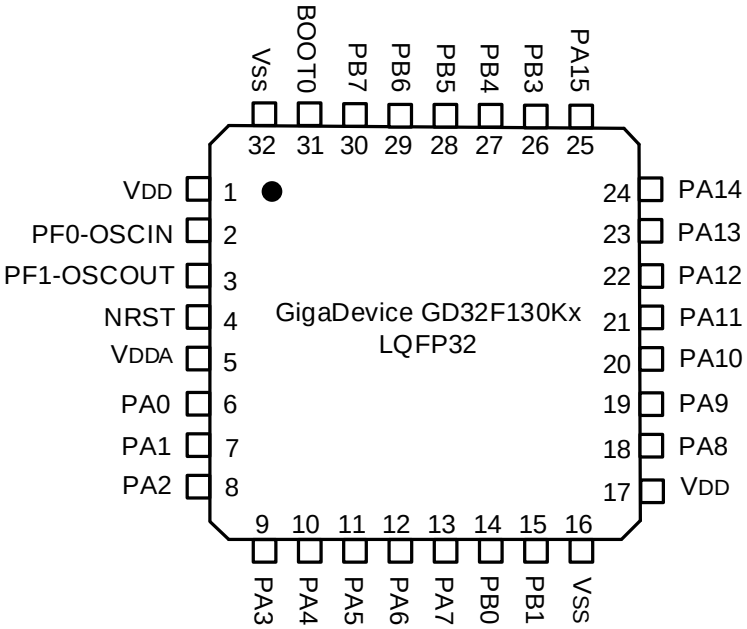


Figure 2-5. GD32F130Kx QFN32 pinouts

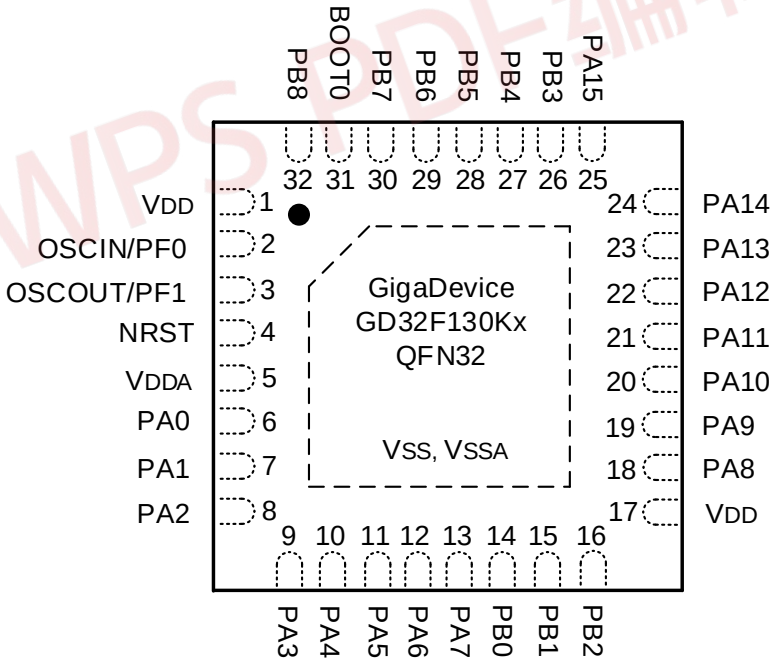


Figure 2-6. GD32F130Gx QFN28 pinouts

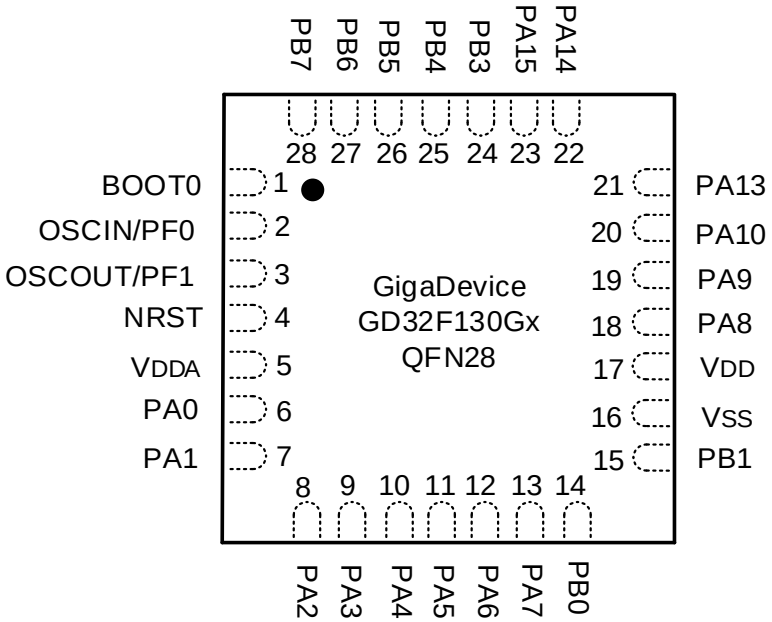
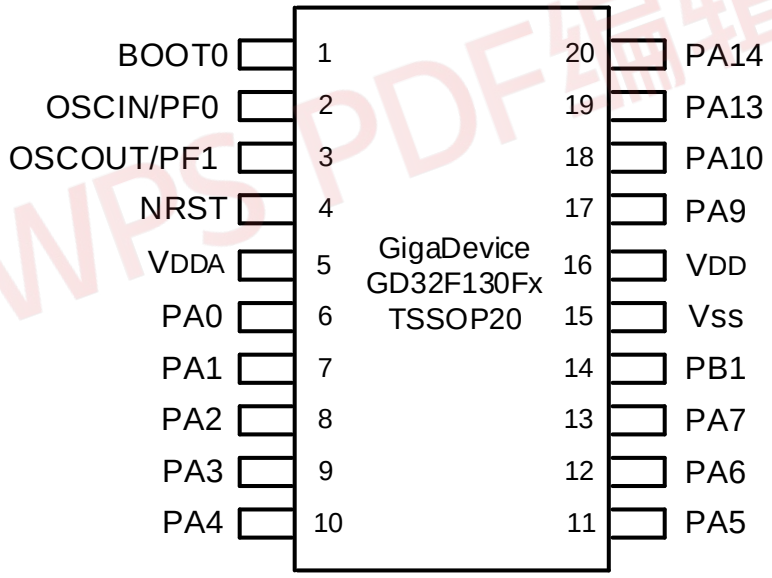


Figure 2-7. GD32F130Fx TSSOP20 pinouts



2.4. Memory map

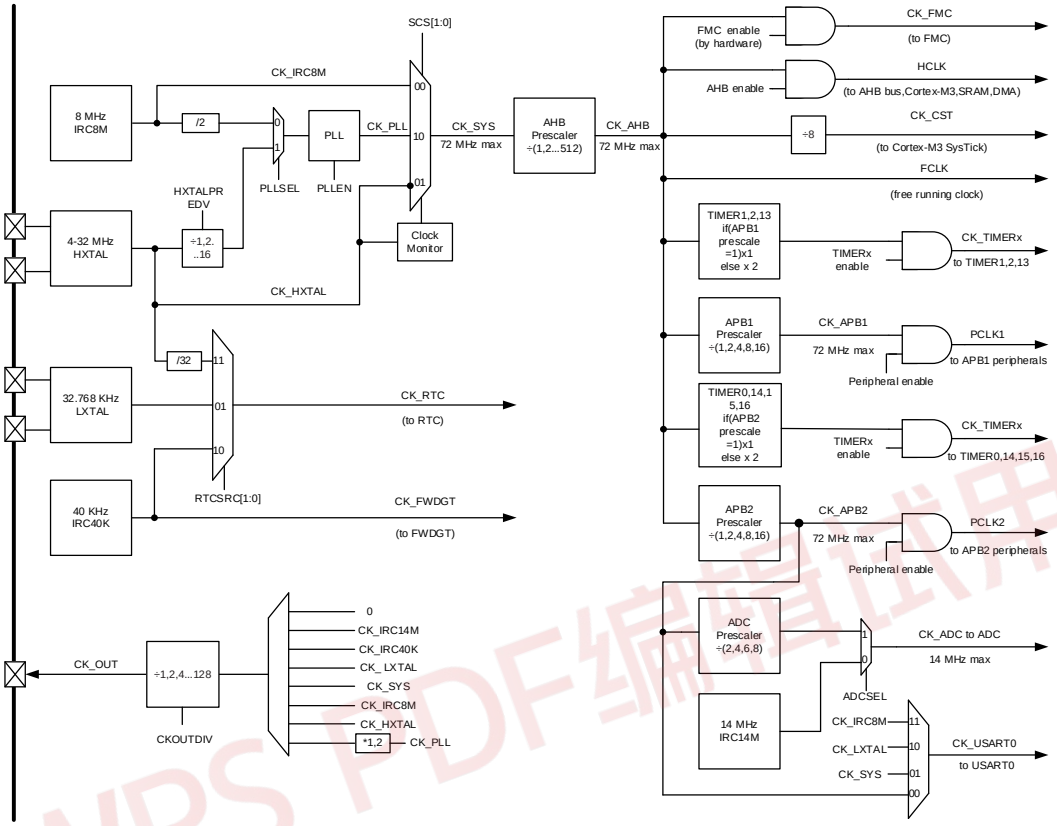
Table 2-2. GD32F130xx memory map

Pre-defined Regions	Bus	Address	Peripherals
		0xE000 0000 - 0xE00F FFFF	Cortex-M3 internal peripherals
External Device		0xA000 0000 - 0xDFFF FFFF	Reserved
External RAM		0x6000 0000 - 0x9FFF FFFF	Reserved
Peripherals	AHB1	0x5000 0000 - 0x5FFF FFFF	Reserved
	AHB2	0x4800 1800 - 0x4FFF FFFF	Reserved
		0x4800 1400 - 0x4800 17FF	GPIOF
		0x4800 1000 - 0x4800 13FF	Reserved
		0x4800 0C00 - 0x4800 0FFF	GPIOD
		0x4800 0800 - 0x4800 0BFF	GPIOC
		0x4800 0400 - 0x4800 07FF	GPIOB
		0x4800 0000 - 0x4800 03FF	GPIOA
	AHB1	0x4002 4400 - 0x47FF FFFF	Reserved
		0x4002 4000 - 0x4002 43FF	Reserved
		0x4002 3400 - 0x4002 3FFF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1400 - 0x4002 1FFF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0400 - 0x4002 0FFF	Reserved
		0x4002 0000 - 0x4002 03FF	DMA
	APB2	0x4001 4C00 - 0x4001 FFFF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER16
		0x4001 4400 - 0x4001 47FF	TIMER15
		0x4001 4000 - 0x4001 43FF	TIMER14
		0x4001 3C00 - 0x4001 3FFF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	Reserved
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	Reserved
		0x4001 2400 - 0x4001 27FF	ADC
		0x4001 0800 - 0x4001 23FF	Reserved
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	SYSCFG
	APB1	0x4000 C400 - 0x4000 FFFF	Reserved
		0x4000 C000 - 0x4000 C3FF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x4000 7C00 - 0x4000 BFFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	Reserved
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6400 - 0x4000 6FFF	Reserved
		0x4000 6000 - 0x4000 63FF	Reserved
		0x4000 5C00 - 0x4000 5FFF	Reserved
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 4800 - 0x4000 53FF	Reserved
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	Reserved
		0x4000 3800 - 0x4000 3BFF	SPI1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 1400 - 0x4000 1FFF	Reserved
		0x4000 1000 - 0x4000 13FF	Reserved
		0x4000 0800 - 0x4000 0FFF	Reserved
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM		0x2000 2000 - 0x3FFF FFFF	Reserved
		0x2000 0000 - 0x2000 1FFF	SRAM
Code		0x1FFF F810 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF F80F	Option bytes
		0x1FFF EC00 - 0x1FFF F7FF	System memory
		0x0801 0000 - 0x1FFF EBFF	Reserved
		0x0800 0000 - 0x0800 FFFF	Main Flash memory
		0x0000 0000 - 0x07FF FFFF	Aliased to Flash or system memory

2.5. Clock tree

Figure 2-8. GD32F130xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillators

IRC40K: Internal 40K RC oscillator

IRC14M: Internal 14M RC oscillators

2.6. Pin definitions

2.6.1. GD32F130R8 LQFP64 pin definitions

Table 2-3. GD32F130R8 LQFP64 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{BAT}	1	P		Default: V_{BAT}
PC13-TAMPER-RTC	2	I/O		Default: PC13 Additional: RTC_TAMP0, RTC_TS, RTC_OUT, WKUP1
PC14-OSC32IN	3	I/O		Default: PC14 Additional: OSC32IN
PC15-OSC32OUT	4	I/O		Default: PC15 Additional: OSC32OUT
PF0-OSCIN	5	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	6	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	7	I/O		Default: NRST
PC0	8	I/O		Default: PC0 Alternate: EVENTOUT Additional: ADC_IN10
PC1	9	I/O		Default: PC1 Alternate: EVENTOUT Additional: ADC_IN11
PC2	10	I/O		Default: PC2 Alternate: EVENTOUT Additional: ADC_IN12
PC3	11	I/O		Default: PC3 Alternate: EVENTOUT Additional: ADC_IN13
V_{SSA}	12	P		Default: V_{SSA}
V_{DDA}	13	P		Default: V_{DDA}
PA0-WKUP	14	I/O		Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, I2C1_SCL Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	15	I/O		Default: PA1 Alternate: USART1_RTS, TIMER1_CH1, I2C1_SDA,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				EVENTOUT Additional: ADC_IN1
PA2	16	I/O		Default: PA2 Alternate: USART1_TX, TIMER1_CH2, TIMER14_CH0 , Additional: ADC_IN2
PA3	17	I/O		Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PF4	18	I/O	5VT	Default: PF4 Alternate: SPI1_NSS, EVENTOUT
PF5	19	I/O	5VT	Default: PF5 Alternate: EVENTOUT
PA4	20	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, TIMER13_CH0, SPI1_NSS Additional: ADC_IN4
PA5	21	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5
PA6	22	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	23	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PC4	24	I/O		Default: PC4 Alternate: EVENTOUT Additional: ADC_IN14
PC5	25	I/O		Default: PC5 Additional: ADC_IN15
PB0	26	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX, EVENTOUT Additional: ADC_IN8
PB1	27	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK Additional: ADC_IN9
PB2	28	I/O	5VT	Default: PB2
PB10	29	I/O	5VT	Default: PB10 Alternate: I2C1_SCL, TIMER1_CH2

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PB11	30	I/O	5VT	Default: PB11 Alternate: I2C1_SDA, TIMER1_CH3, EVENTOUT
V_{SS}	31	P		Default: V_{SS}
V_{DD}	32	P		Default: V_{DD}
PB12	33	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, TIMER0_BRKIN, I2C1_SMBA, EVENTOUT
PB13	34	I/O	5VT	Default: PB13 Alternate: SPI1_SCK, TIMER0_CH0_ON
PB14	35	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, TIMER0_CH1_ON, TIMER14_CH0
PB15	36	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1 Additional: RTC_REFIN
PC6	37	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0
PC7	38	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1
PC8	39	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2
PC9	40	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3
PA8	41	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX, EVENTOUT
PA9	42	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL
PA10	43	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA11	44	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT
PA12	45	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT
PA13	46	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO
PF6	47	I/O	5VT	Default: PF6 Alternate: I2C1_SCL
PF7	48	I/O	5VT	Default: PF7 Alternate: I2C1_SDA

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PA14	49	I/O	5VT	Default: PA14 Alternate: USART1_TX, SWCLK, SPI1_MOSI
PA15	50	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, USART1_RX, TIMER1_CH0, TIMER1_ETI, SPI1_NSS, EVENTOUT
PC10	51	I/O	5VT	Default: PC10
PC11	52	I/O	5VT	Default: PC11
PC12	53	I/O	5VT	Default: PC12
PD2	54	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI
PB3	55	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT
PB4	56	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT
PB5	57	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
PB6	58	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	59	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON
BOOT0	60	I		Default: BOOT0
PB8	61	I/O	5VT	Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0
PB9	62	I/O	5VT	Default: PB9 Alternate: I2C0_SDA, IFRP_OUT, TIMER16_CH0, EVENTOUT
V_{SS}	63	P		Default: V_{SS}
V_{DD}	64	P		Default: V_{DD}

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.2. GD32F130Cx LQFP48 pin definitions

Table 2-4. GD32F130Cx LQFP48 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{BAT}	1	P		Default: V_{BAT}
PC13-TAMPER-RTC	2	I/O		Default: PC13 Additional: RTC_TAMP0, RTC_TS, RTC_OUT, WKUP1
PC14-OSC32IN	3	I/O		Default: PC14 Additional: OSC32IN
PC15-OSC32OUT	4	I/O		Default: PC15 Additional: OSC32OUT
PF0-OSCIN	5	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	6	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	7	I/O		Default: NRST
V_{SSA}	8	P		Default: V_{SSA}
V_{DDA}	9	P		Default: V_{DDA}
PA0-WKUP	10	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	11	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	12	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 Additional: ADC_IN2
PA3	13	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PA4	14	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	15	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PA6	16	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	17	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	18	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT Additional: ADC_IN8
PB1	19	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
PB2	20	I/O	5VT	Default: PB2
PB10	21	I/O	5VT	Default: PB10 Alternate: I2C1_SCL(5), TIMER1_CH2
PB11	22	I/O	5VT	Default: PB11 Alternate: I2C1_SDA(5), TIMER1_CH3, EVENTOUT
V_{SS}	23	P		Default: V_{SS}
V_{DD}	24	P		Default: V_{DD}
PB12	25	I/O	5VT	Default: PB12 Alternate: SPI0_NSS(3), SPI1_NSS(5), TIMER0_BRKIN, I2C1_SMBA(5), EVENTOUT
PB13	26	I/O	5VT	Default: PB13 Alternate: SPI0_SCK(3), SPI1_SCK(5), TIMER0_CH0_ON
PB14	27	I/O	5VT	Default: PB14 Alternate: SPI0_MISO(3), SPI1_MISO(5), TIMER0_CH1_ON, TIMER14_CH0
PB15	28	I/O	5VT	Default: PB15 Alternate: SPI0_MOSI(3), SPI1_MOSI(5), TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1 Additional: RTC_REFIN
PA8	29	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX(4), EVENTOUT
PA9	30	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL
PA10	31	I/O	5VT	Default: PA10

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA11	32	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT
PA12	33	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT
PA13	34	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)
PF6	35	I/O	5VT	Default: PF6 Alternate: I2C1_SCL(5), I2C0_SCL(6)
PF7	36	I/O	5VT	Default: PF7 Alternate: I2C1_SDA(5), I2C0_SCL(6)
PA14	37	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	38	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS(5), EVENTOUT
PB3	39	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT
PB4	40	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT
PB5	41	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
PB6	42	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	43	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON
BOOT0	44	I		Default: BOOT0
PB8	45	I/O	5VT	Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0,
PB9	46	I/O	5VT	Default: PB9 Alternate: I2C0_SDA, IFRP_OUT, TIMER16_CH0, EVENTOUT
V_{SS}	47	P		Default: V_{SS}
V_{DD}	48	P		Default: V_{DD}

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32F130C4 devices only.

(4) Functions are available on GD32F130C8/6 devices.

(5) Functions are available on GD32F130C8 devices.

(6) Functions are available on GD32F130C4/6 devices.

2.6.3. GD32F130Kx LQFP32 pin definitions

Table 2-5. GD32F130Kx LQFP32 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{DD}	1	P		Default: V_{DD}
PF0-OSCIN	2	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 Additional: ADC_IN2
PA3	9	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	14	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT Additional: ADC_IN8
PB1	15	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
Vss	16	P	5VT	Default: Vss
V_{DD}	17	P		Default: V_{DD}
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX(4), EVENTOUT
PA9	19	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA11	21	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT
PA12	22	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT
PA13	23	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)
PA14	24	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	25	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS(5), EVENTOUT
PB3	26	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT
PB4	27	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT
PB5	28	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
PB6	29	I/O	5VT	Default: PB6

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	30	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON
BOOT0	31	I		Default: BOOT0
Vss	32	P		Default: Vss

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32F130K4 devices only.

(4) Functions are available on GD32F130K8/6 devices.

(5) Functions are available on GD32F130K8 devices.

2.6.4. GD32F130Kx QFN32 pin definitions

Table 2-6. GD32F130Kx QFN32 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{DD}	1	P		Default: V_{DD}
PF0-OSCIN	2	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 Additional: ADC_IN2
PA3	9	I/O		Default: PA3

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	14	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT Additional: ADC_IN8
PB1	15	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
PB2	16	I/O	5VT	Default: PB2
V_{DD}	17	P		Default: V_{DD}
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX(4), EVENTOUT
PA9	19	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA11	21	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT
PA12	22	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT
PA13	23	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PA14	24	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	25	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS(5), EVENTOUT
PB3	26	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT
PB4	27	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT
PB5	28	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
PB6	29	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	30	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON
BOOT0	31	I		Default: BOOT0
PB8	32	I/O	5VT	Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0

Notes:

(6) Type: I = input, O = output, P = power.

(7) I/O Level: 5VT = 5 V tolerant.

(8) Functions are available on GD32F130K4 devices only.

(9) Functions are available on GD32F130K8/6 devices.

(10) Functions are available on GD32F130K8 devices.

2.6.5. GD32F130Gx QFN28 pin definitions

Table 2-7. GD32F130Gx QFN28 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
BOOT0	1	I		Default: BOOT0
PF0-OSCIN	2	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 Additional: ADC_IN2
PA3	9	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	14	I/O		Default: PB0

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT Additional: ADC_IN8
PB1	15	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
V_{SS}	16	P		Default: V_{SS}
V_{DD}	17	P		Default: V_{DD}
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX(4), EVENTOUT
PA9	19	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN , I2C0_SCL
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA13	21	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)
PA14	22	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	23	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS(5), EVENTOUT
PB3	24	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT
PB4	25	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT
PB5	26	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
PB6	27	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	28	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32F130G4 devices only.

(4) Functions are available on GD32F130G8/6 devices.

(5) Functions are available on GD32F130G8 devices.

2.6.6. GD32F130Fx TSSOP20 pin definitions

Table 2-8. GD32F130Fx TSSOP20 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
BOOT0	1	I		Default: BOOT0
PF0-OSCIN	2	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 Additional: ADC_IN2
PA3	9	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB1	14	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
V_{SS}	15	P		Default: V_{SS}
V_{DD}	16	P		Default: V_{DD}
PA9	17	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL
PA10	18	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA13	19	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)
PA14	20	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32F130F4 devices only.

(4) Functions are available on GD32F130F8/6 devices.

(5) Functions are available on GD32F130F8 devices.

2.6.7. GD32F130xx pin alternate functions

Table 2-9. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PA0		USART0_CTS(1) USART1_CTS(2)	TIMER1_CH0 TIMER1_ETI		I2C1_SCL(3)		
PA1	EVENTOUT	USART0_RTS(1) USART1_RTS(2)	TIMER1_CH1		I2C1_SDA(3)		
PA2	TIMER14_CH0	USART0_TX(1) USART1_TX(2)	TIMER1_CH2				
PA3	TIMER14_CH1	USART0_RX(1) USART1_RX(2)	TIMER1_CH3				
PA4	SPI0_NSS	USART0_CK(1) USART1_CK(2)			TIMER13_CH0		SPI1_NSS(3)
PA5	SPI0_SCK		TIMER1_CH0 TIMER1_ETI				
PA6	SPI0_MISO	TIMER2_CH0	TIMER0_BRKIN			TIMER15_CH0	EVENTOUT
PA7	SPI0_MOSI	TIMER2_CH1	TIMER0_CH0_ON		TIMER13_CH0	TIMER16_CH0	EVENTOUT
PA8	CK_OUT	USART0_CK	TIMER0_CH0	EVENTOUT	USART1_TX(2)		
PA9	TIMER14_BRKIN	USART0_TX	TIMER0_CH1		I2C0_SCL		
PA10	TIMER16_BRKIN	USART0_RX	TIMER0_CH2		I2C0_SDA		
PA11	EVENTOUT	USART0_CTS	TIMER0_CH3				
PA12	EVENTOUT	USART0_RTS	TIMER0_ETI				
PA13	SWDIO	IFRP_OUT					SPI1_MISO(3)
PA14	SWCLK	USART0_TX(1) USART1_TX(2)					SPI1_MOSI(3)
PA15	SPI0_NSS	USART0_RX(1) USART1_RX(2)	TIMER1_CH0 TIMER1_ETI	EVENTOUT			SPI1_NSS(3)

Notes:

(1) Functions are available on GD32F130x4 devices only.

(2) Functions are available on GD32F130x8/6 devices.

(3) Functions are available on GD32F130x8 devices.

Table 2-10. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PB0	EVENTOUT	TIMER2_CH2	TIMER0_CH1_ON		USART1_RX(2)		
PB1	TIMER13_CH0	TIMER2_CH3	TIMER0_CH2_ON				SPI1_SCK(3)
PB2							
PB3	SPI0_SCK	EVETOUT	TIMER1_CH1				
PB4	SPI0_MISO	TIMER2_CH0	EVENTOUT				
PB5	SPI0_MOSI	TIMER2_CH1	TIMER15_BRKIN	I2C0_SMBA			
PB6	USART0_TX	I2C0_SCL	TIMER15_CH0_ON				
PB7	USART0_RX	I2C0_SDA	TIMER16_CH0_ON				
PB8		I2C0_SCL	TIMER15_CH0				
PB9	IFRP_OUT	I2C0_SDA	TIMER16_CH0	EVENTOUT			
PB10		I2C1_SCL(3)	TIMER1_CH2				
PB11	EVENTOUT	I2C1_SDA(3)	TIMER1_CH3				
PB12	SPI0_NSS(1) SPI1_NSS(3)	EVENTOUT	TIMER0_BRKIN		I2C1_SMBA(3)		
PB13	SPI0_SCK(1) SPI1_SCK(3)		TIMER0_CH0_ON				
PB14	SPI0_MISO(1) SPI1_MISO(3)	TIMER14_CH0	TIMER0_CH1_ON				
PB15	SPI0_MOSI(1) SPI1_MOSI(3)	TIMER14_CH1	TIMER0_CH2_ON	TIMER14_CH0_ON			

Notes:

(1) Functions are available on GD32F130x4 devices only.

(2) Functions are available on GD32F130x8/6 devices.

(3) Functions are available on GD32F130x8 devices.

Table 2-11. Port C & D & F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PC0	EVENTOUT						
PC1	EVENTOUT						
PC2	EVENTOUT						
PC3	EVENTOUT						
PC4	EVENTOUT						
PC6	TIMER2_CH0						
PC7	TIMER2_CH1						
PC8	TIMER2_CH2						
PC9	TIMER2_CH3						
PD2	TIMER2_ETI						
PF4	SPI1_NSS,EVENTOUT						
PF5	EVENTOUT						
PF6	I2C0_SCL(1) I2C1_SCL(2)						
PF7	I2C0_SDA(1) I2C1_SDA(2)						

Notes:

(1) Functions are available on GD32F130x4/6 devices.

(2) Functions are available on GD32F130x8 devices only.

3. Functional description

3.1. ARM® Cortex®-M3 core

The Cortex®-M3 processor is the latest generation of ARM® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

- 32-bit ARM® Cortex®-M3 processor core
- Up to 72 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

3.2. On-chip memory

- Up to 64 Kbytes of Flash memory
- Up to 8 Kbytes of SRAM with hardware parity checking

The ARM® Cortex®-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 64 Kbytes of inner Flash and 8 Kbytes of inner SRAM at most is available for storing programs and data, both accessed (R/W) at CPU clock speed with zero wait states. The ***Table 2-2. GD32F130xx memory map*** shows the memory map of the GD32F130xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator

- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB and two APB domains is 72 MHz. See ***Figure 2-8. GD32F130xx clock tree*** for details on the clock tree.

GD32F1x0 Reset Control includes the control of three kinds of reset: power reset, system reset and backup domain reset. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller and the Backup domain. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.6 V and down to 1.8V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a wake up message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10) or USART1 (PA2 and PA3, PA14 and PA15).

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance

between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, the RTC tamper and Timestamp, the USART0 wakeup and the CEC wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.
- **Standby** mode
  In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except Backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pin.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC engine with up to 1 MSPS conversion rate
- Input voltage range: V_{SSA} to V_{DDA} (2.6 to 3.6 V)
- Temperature sensor

One 12-bit 1 μs multi-channel ADCs are integrated in the device. It is a total of up to 16 multiplexed external channels and 3 internal channels for temperature sensor, voltage reference, V_{BAT} voltage measurement. The conversion range is between 2.6 V < V_{DDA} < 3.6 V. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages. The ADC can be triggered from the events generated by the general timers (TIMERx=1,2,14) and the advanced timers (TIMER0) with internal connection.

The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value. Each device is factory-calibrated to improve the accuracy and the calibration data are stored in the system memory area.

3.7. DMA

- 7 channel DMA controller
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.8. General-purpose inputs/outputs (GPIOs)

- Up to 55 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 55 general purpose I/O pins (GPIO) in GD32F130xx, named PA0 ~ PA15 and PB0 ~ PB15, PC0 ~ PC15, PD2, PF0, PF1, PF4-PF7 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.9. Timers and PWM generation

- One 16-bit advanced timer (TIMER0), one 32-bit general timer (TIMER1), five 16-bit general timers (TIMER2, TIMER13 ~ TIMER16)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, compare match output, generation of PWM waveform (edge-aligned and center-aligned Mode) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other

general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER13 ~ TIMER16 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The GD32F130xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler, It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in stop and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wake up interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.10. Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with five 32-bit backup registers
- Calendar with subsecond, seconds, minutes, hours, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 1 ppm resolution for compensation of quartz crystal inaccuracy

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from

external crystal oscillator.

3.11. Inter-integrated circuit (I2C)

- Up to two I2Cs bus interfaces can support both master and slave mode with a frequency up to 400 KHz
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides transfer rate of up to 100 KHz in standard mode and up to 400 KHz in fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.12. Serial peripheral interface (SPI)

- Up to two SPIs interfaces with a frequency of up to 18 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.13. Universal synchronous asynchronous receiver transmitter (USART)

- Up to two USARTs with operating frequency up to 9 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous

transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.14. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.15. Package and operation temperature

- LQFP64 (GD32F130Rx), LQFP48 (GD32F130Cx), LQFP32 (GD32F130Kx), QFN32 (GD32F130Kx), QFN28 (GD32F130Gx) and TSSOP20 (GD32F130Fx)
- Operation temperature range: -40°C to +85°C (industrial level)

4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin	V_{SS} - 0.3	V_{DD} + 4.0	V
	Input voltage on other I/O	V_{SS} - 0.3	4.0	V
I_{IO}	Maximum current for GPIO pins	—	25	mA
T_A	Operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C

4.2. Recommended DC characteristics

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	—	2.6	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.6	3.3	3.6	V
V_{BAT}	Battery supply voltage	—	1.8	—	3.6	V

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-3. Power consumption characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current (Run mode)	V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, System clock=48 MHz, All peripherals enabled	—	17.26	—	mA
		V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, System clock =48 MHz, All peripherals disabled	—	12.23	—	mA
		V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, System clock =24 MHz, All peripherals enabled	-—	9.26	—	mA
		V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, System Clock =24 MHz, All peripherals disabled	—	6.75	—	mA
	Supply current (Sleep mode)	V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, CPU clock off, System clock =48 MHz, All peripherals enabled	—	9.76	—	mA
		V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, CPU clock off, System clock =48 MHz, All peripherals disabled	—	3.89	—	mA
	Supply current (Deep-Sleep mode)	V_{DD}=V_{BAT}=3.3V, Regulator in run mode, IRC40K on, RTC on, All GPIOs analog mode	—	155.14	—	µA
		V_{DD}=V_{BAT}=3.3V, Regulator in low power mode, IRC40K on, RTC on, All GPIOs analog mode	—	143.17	—	µA
	Supply current (Standby mode)	V_{DD}=V_{BAT}=3.3V, LXTAL off, IRC40K on, RTC on	—	7.38	—	µA
		V_{DD}=V_{BAT}=3.3V, LXTAL off, IRC40K on, RTC off	—	6.94	—	µA
		V_{DD}=V_{BAT}=3.3V, LXTAL off, IRC40K off, RTC off	—	5.74	—	µA
I_{BAT}	Battery supply current	V_{DD} not available, V_{BAT}=3.6 V, LXTAL on with external crystal, RTC on, Higher driving	—	3.08	—	µA
		V_{DD} not available, V_{BAT}=3.3 V, LXTAL on with external crystal, RTC on, Higher driving	—	2.78	—	µA
		V_{DD} not available, V_{BAT}=2.6 V, LXTAL on with external crystal, RTC on, Higher driving	—	2.12	—	µA
		V_{DD} not available, V_{BAT}=3.6 V, LXTAL on with external crystal, RTC on, Lower driving	—	1.37	—	µA
		V_{DD} not available, V_{BAT}=3.3 V, LXTAL on with external crystal, RTC on, Lower driving	—	1.25	—	µA
		V_{DD} not available, V_{BAT}=2.6 V, LXTAL on with external crystal, RTC on, Lower driving	—	1.05	—	µA

4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the ***Table 4-4. EMS characteristics***, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-4. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C conforms to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	V_{DD} = 3.3 V, T_A = +25 °C conforms to IEC 61000-4-4	4A

EMI (Electromagnetic Interference) emission testing result is given in the ***Table 4-5. EMI characteristics***, compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 4-5. EMI characteristics

Symbol	Parameter	Conditions	Tested frequency band	Conditions		Unit
				24M	48M	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = +25 °C, compliant with IEC 61967-2	0.1 to 2 MHz	<0	<0	dBµV
			2 to 30 MHz	-3.9	-2.8	
			30 to 130 MHz	-7.2	-8	
			130 MHz to 1GHz	-7	-7	

4.5. Power supply supervisor characteristics

Table 4-6. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold	PDR_S=0	2.32	2.40	2.48	V
V_{PDR}	Power down reset threshold		2.27	2.35	2.43	V
V_{HYST}	PDR hysteresis		—	0.05	—	V
$T_{RSTTEMP}$	Reset temporization		—	2	—	ms
V_{POR}	Power on reset threshold	PDR_S=1	2.32	2.40	2.48	V
V_{PDR}	Power down reset threshold		1.72	1.80	1.88	V
V_{HYST}	PDR hysteresis		—	0.6	—	V
$T_{RSTTEMP}$	Reset temporization		—	2	—	ms

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-7. ESD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25 °C; JESD22-A114	—	—	5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=25 °C; JESD22-C101	—	—	500	V

Table 4-8. Static latch-up characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A=25 °C; JESD78	—	—	±100	mA
	V_{supply} over voltage		—	—	5.4	V

4.7. External clock characteristics

Table 4-9. High speed crystal oscillator (HXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	High Speed crystal oscillator (HXTAL) frequency	V_{DD}=3.3V	4	8	32	MHz
C_{HXTAL}	Recommended load capacitance on OSCIN and OSCOUT	—	—	20	30	pF
R_{FHXTAL}	Recommended external feedback resistor between XTALIN and XTALOUT	—	—	200	—	KΩ
D_{HXTAL}	HXTAL oscillator duty cycle	—	48	50	52	%
$I_{DDHXTAL}$	HXTAL oscillator operating current	V_{DD}=3.3V, T_A=25°C	—	1.4	—	μA
$t_{SUHXTAL}$	HXTAL oscillator startup time	V_{DD}=3.3V, T_A=25°C	—	2	—	ms

Table 4-10. Low speed crystal oscillator (LXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Low Speed crystal oscillator (LXTAL) frequency	V_{DD}=V_{BAT}=3.3V	—	32.768	1000	KHz
C_{LXTAL}	Recommended load capacitance on OSC32IN and OSC32OUT	—	—	—	15	pF
D_{LXTAL}	LXTAL oscillator duty cycle	—	48	50	52	%
$I_{DDLXTAL}$	LXTAL oscillator operating current	V_{DD}=V_{BAT}=3.3V	—	1.4	—	µA
$t_{SULXTAL}$	LXTAL oscillator startup time	V_{DD}=V_{BAT}=3.3V	—	3	—	s

4.8. Internal clock characteristics

Table 4-11. Internal 8 MHz RC oscillator (IRC8M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	Internal 8 MHz RC oscillator (IRC8M) frequency	V_{DD}=3.3V	—	8	—	MHz
ACC_{IRC8M}	IRC8M oscillator Frequency accuracy, Factory-trimmed	V_{DD}=3.3V, T_A=-40°C ~+105°C	-2.5	—	+1.5	%
		V_{DD}=3.3V, T_A=0°C ~ +85°C	-1.2	—	+1.2	%
		V_{DD}=3.3V, T_A=25°C	-1	—	+1	%
D_{IRC8M}	IRC8M oscillator duty cycle	V_{DD}=3.3V, f_{IRC8M}=8MHz	48	50	52	%
$I_{DDIRC8M}$	IRC8M oscillator operating current	V_{DD}=3.3V, f_{IRC8M}=8MHz	—	80	100	µA
$t_{SUIRC8M}$	IRC8M oscillator startup time	V_{DD}=3.3V, f_{IRC8M}=8MHz	1	—	2	us

Table 4-12. Internal 40KHz RC oscillator (IRC40K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC40K}	Internal 40KHz RC oscillator (IRC40K) frequency	V_{DD}=V_{BAT}=3.3V, T_A=-40°C ~ +85°C	30	40	60	KHz
$I_{DDIRC40K}$	IRC40K oscillator operating current	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	1	2	µA
$t_{SUIRC40K}$	IRC40K oscillator startup time	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	—	80	µs

4.9. PLL characteristics

Table 4-13. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency		1	8	25	MHz
f_{PLL}	PLL output clock frequency		16	—	72	MHz
t_{LOCK}	PLL lock time		—		200	μs
$Jitter_{PLL}$	Cycle to cycle Jitter				300	ps

4.10. Memory characteristics

Table 4-14. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A=-40°C ~ +85°C	100	—	—	kcycles
t_{RET}	Data retention time	T_A=125°C	20	—	—	years
t_{PROG}	Word programming time	T_A=-40°C ~ +85°C	200	—	400	us
t_{ERASE}	Page erase time	T_A=-40°C ~ +85°C	60	100	450	ms
t_{MERASE}	Mass erase time	T_A=-40°C ~ +85°C	3.2	—	9.6	s

4.11. GPIO characteristics

Table 4-15. I/O port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage	V_{DD}=2.6V	-0.3	—	0.95	V
	5V-tolerant IO Low level input voltage	V_{DD}=2.6V	-0.3	—	0.9	V
V_{IH}	Standard IO High level input voltage	V_{DD}=2.6V	1.2	—	4.0	V
	5V-tolerant IO High level input voltage	V_{DD}=2.6V	1.5	—	5.5	V
V_{OL}	Low level output voltage	V_{DD}=2.6V	—	—	0.2	V
V_{OH}	High level output voltage	V_{DD}=2.6V	2.3	—	—	V
R_{PU}	Internal pull-up resistor	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Internal pull-down resistor	V_{IN}=V_{DD}	30	40	50	kΩ

4.12. ADC characteristics

Table 4-16. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage		2.6	3.3	3.6	V
V_{IN}	ADC input voltage range		0	—	V_{DDA}	V
f_{ADC}	ADC clock		0.6	—	14	MHz
f_S	Sampling rate		—	—	1	MHz
$f_{ADCCONV}$	ADC conversion time	f_{ADC} =14MHz	1	—	18	μs
R_{ADC}	Input sampling switch resistance		—	—	0.2	kΩ
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	—	32	—	pF
t_{SU}	Startup time		—	—	1	μs

4.13. SPI characteristics

Table 4-17. Standard SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency		—	—	18	MHz
$t_{SCK(H)}$	SCK clock high time		19	—	—	ns
$t_{SCK(L)}$	SCK clock low time		19	—	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time		—	—	25	ns
$t_{H(MO)}$	Data output hold time		2	—	—	ns
$t_{SU(MI)}$	Data input setup time		5	—	—	ns
$t_{H(MI)}$	Data input hold time		5	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	f_{PCLK}=54MHz	74	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	f_{PCLK}=54MHz	37	—	—	ns
$t_{A(SO)}$	Data output access time	f_{PCLK}=54MHz	0	—	55	ns
$t_{DIS(SO)}$	Data output disable time		3	—	10	ns
$t_{V(SO)}$	Data output valid time		—	—	25	ns
$t_{H(SO)}$	Data output hold time		15	—	—	ns
$t_{SU(SI)}$	Data input setup time		5	—	—	ns
$t_{H(SI)}$	Data input hold time		4	—	—	ns

4.14. I2C characteristics

Table 4-18. I2C characteristics

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	KHz
$t_{SCL(H)}$	SCL clock high time		4.0	—	0.6	—	ns
$t_{SCL(L)}$	SCL clock low time		4.7	—	1.3	—	ns

5. Package information

5.1. TSSOP package outline dimensions

Figure 5-1. TSSOP package outline

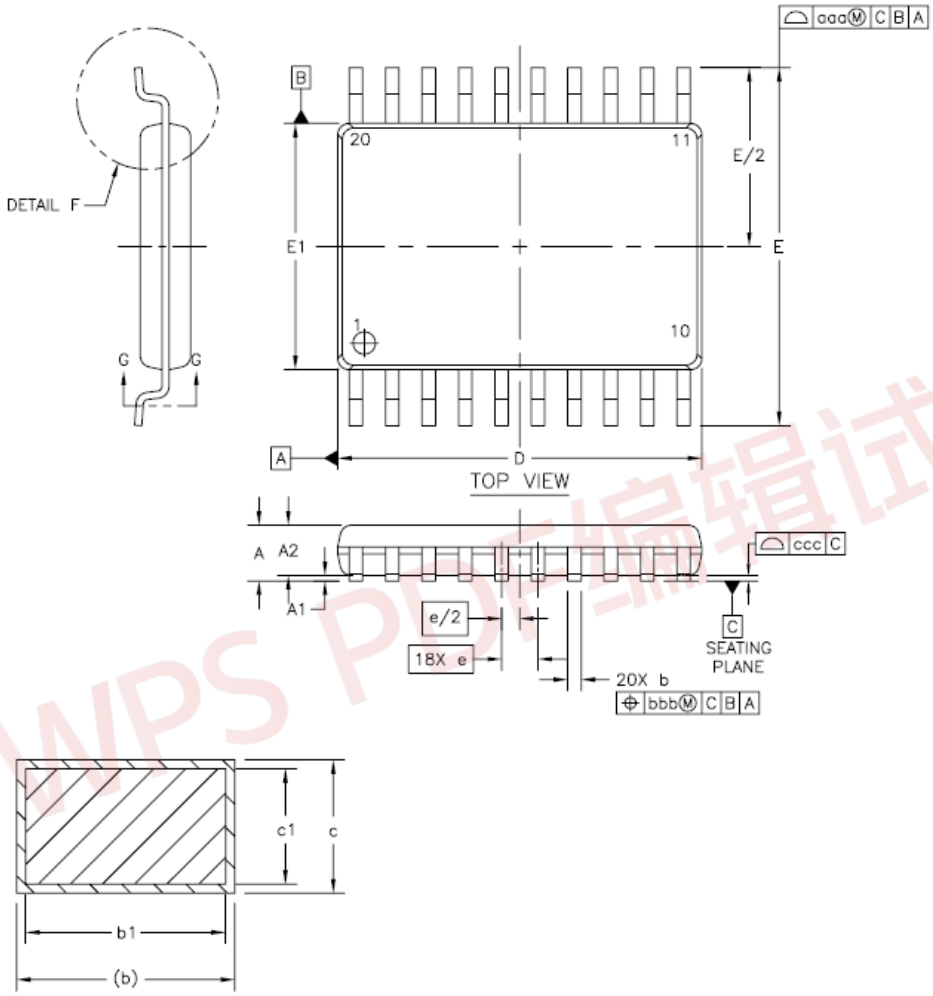


Table 5-1. TSSOP20 package dimensions

Symbol	Dimensions (mm)			Symbol	Dimensions (mm)		
	Min	Typ	Max		Min	Typ	Max
A	-	-	1.2	c1	0.09	-	0.16
A1	0.05	-	1.15	D	6.4	6.5	6.6
A2	0.80	1.00	1.05	E1	4.3	4.4	4.5
b	0.19	-	0.30	E	6.40		
B1	0.19	0.22	0.25	e	0.65		
c	0.09	-	0.20	L	0.45	0.6	0.75

5.2. QFN package outline dimensions

Figure 5-2. QFN package outline

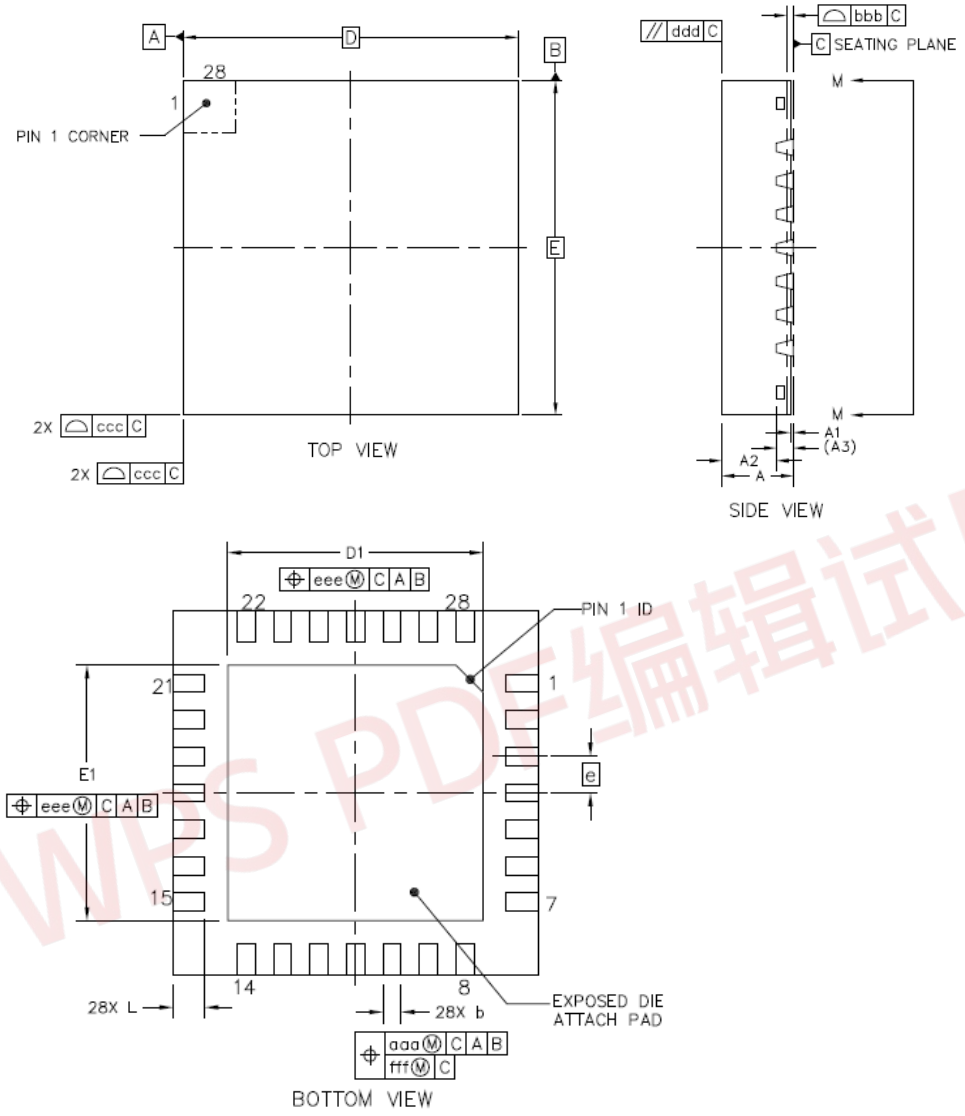


Table 5-2. QFN package dimensions

Symbol	QFN28			QFN32		
	Min	Typ	Max	Min	Typ	Max
A	0.8	0.85	0.9	0.8	0.85	0.9
A1	0	0.035	0.05	0	0.035	0.05
A2	-	0.65	0.67	-	0.65	0.67
A3	-	0.203	-	-	0.203	-
D	-	4.0	-	-	5.0	-
E	-	4.0	-	-	5.0	-
D1	2.7	2.8	2.9	3.4	3.5	3.6
E1	2.7	2.8	2.9	3.4	3.5	3.6
L	0.25	0.35	0.45	0.3	0.4	0.5
e	0.4			0.5		
b	0.15	0.2	0.25	0.2	0.25	0.3

(Original dimensions are in millimeters)

5.3. LQFP package outline dimensions

Figure 5-3. LQFP package outline

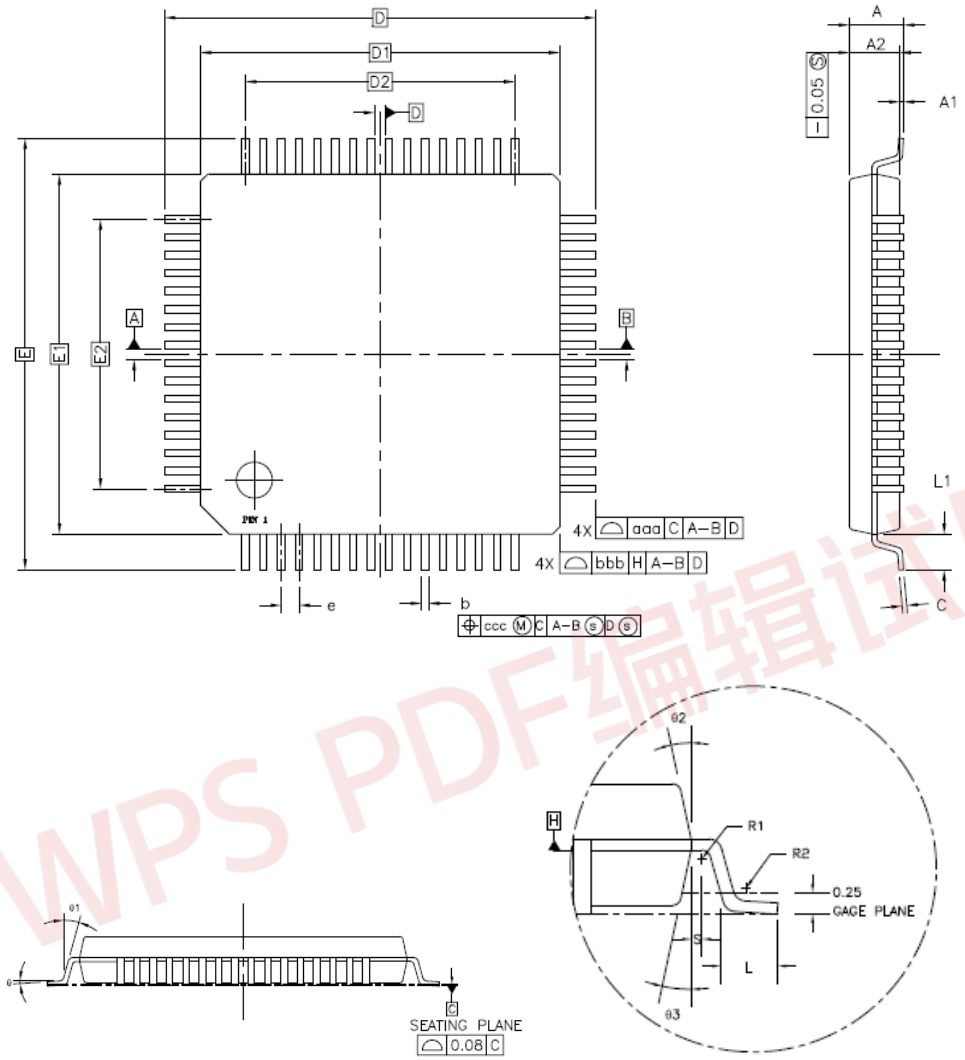


Table 5-3. LQFP package dimensions

Symbol	LQFP32			LQFP48			LQFP64		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	1.50	-	-	1.60
A1	0.05	-	0.25	0.05	-	0.15	0.05	-	0.15
A2	1.35	1.40	1.45	0.95	1.00	1.35	1.35	1.40	1.45
D	-	9.00	-	-	9.00	-	-	12.00	-
D1	-	7.00	-	-	7.00	-	-	10.00	-
E	-	9.00	-	-	9.00	-	-	12.00	-
E1	-	7.00	-	-	7.00	-	-	10.00	-
R1	0.08	-	-	0.08	-	-	0.08	-	-
R2	0.08	-	0.20	0.08	-	0.20	0.08	-	0.20
θ	0°	3.5°	7°	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-	0°	-	-
θ2	11°	12°	13°	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°	11°	12°	13°
c	0.09	-	0.20	0.09	-	0.20	0.09	-	0.20
L	0.45	0.60	0.75	0.45	0.60	0.75	0.45	0.60	0.75
L1	-	1.00	-	-	1.00	-	-	1.00	-
S	0.20	-	-	0.20	-	-	0.20	-	-
b	0.17	0.22	0.27	0.17	0.22	0.27	0.17	0.20	0.27
e	-	0.50	-	-	0.50	-	-	0.50	-
D2	-	5.50	-	-	5.50	-	-	7.50	-
E2	-	5.50	-	-	5.50	-	-	7.50	-
aaa	0.20			0.20			0.20		
bbb	0.20			0.20			0.20		
ccc	0.08			0.08			0.08		

(Original dimensions are in millimeters)

6. Ordering information

Table 6-1. Part ordering code for GD32F130xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F130F4P6	16	TSSOP20	Green	Industrial -40°C to +85°C
GD32F130F6P6	32	TSSOP20	Green	Industrial -40°C to +85°C
GD32F130F8P6	64	TSSOP20	Green	Industrial -40°C to +85°C
GD32F130G4U6	16	QFN28	Green	Industrial -40°C to +85°C
GD32F130G6U6	32	QFN28	Green	Industrial -40°C to +85°C
GD32F130G8U6	64	QFN28	Green	Industrial -40°C to +85°C
GD32F130K4U6	16	QFN32	Green	Industrial -40°C to +85°C
GD32F130K6U6	32	QFN32	Green	Industrial -40°C to +85°C
GD32F130K8U6	64	QFN32	Green	Industrial -40°C to +85°C
GD32F130K4T6	16	LQFP32	Green	Industrial -40°C to +85°C
GD32F130K6T6	32	LQFP32	Green	Industrial -40°C to +85°C
GD32F130K8T6	64	LQFP32	Green	Industrial -40°C to +85°C
GD32F130C4T6	16	LQFP48	Green	Industrial -40°C to +85°C
GD32F130C6T6	32	LQFP48	Green	Industrial -40°C to +85°C
GD32F130C8T6	64	LQFP48	Green	Industrial -40°C to +85°C
GD32F130R8T6	64	LQFP64	Green	Industrial -40°C to +85°C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.8, 2014
1.1	Characteristics values updated in ***Table 4-3. Power consumption characteristics***	Oct.20, 2014
2.0	Characteristics of QFN32 package added in ***Table 2-3. GD32F130R8 LQFP64 pin definitions*** and ***Table 5-2. QFN package dimensions***	Jan 15, 2015
2.1	Characteristics of TSSOP20 package added in ***Table 2-1. GD32F130xx devices features and peripheral list***	Apr 24, 2016
3.0	Adapt To New Name Convention	Jan.24, 2018
3.1	Add LQFP32 Package	Apr.24, 2018

General Description

The DS28E07 is a 1024-bit, 1-Wire® EEPROM chip organized as four memory pages of 256 bits each. Data is written to an 8-byte scratchpad, verified, and then copied to the EEPROM memory. As a special feature, the four user memory pages can individually be write protected or put in EPROM-emulation mode, where bits can only be changed from a 1 to a 0 state. Each device has its own guaranteed unique 64-bit ROM identification number (ROM ID) that is factory programmed into the chip. The communication follows the 1-Wire protocol with the ROM ID acting as node address in the case of a multiple-device 1-Wire network.

Applications

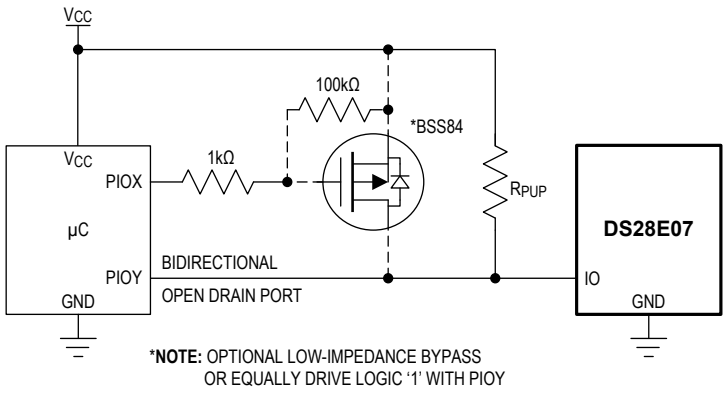
- Accessory/PCB Identification
- Medical Sensor Calibration Data Storage
- Analog Sensor Calibration Including IEEE P1451.4 Smart Sensors
- Ink and Toner Print Cartridge Identification
- After-Market Management of Consumables

Benefits and Features

- Partitioning of Memory Provides Greater Flexibility in Programming User Data
  - 1024 Bits of EEPROM Memory Organized as Four Pages of 256 Bits
  - Individual Memory Pages Can Be Permanently Write Protected or Put in EPROM-Emulation Mode (Write to 0)
- Advanced 1-Wire Protocol Minimizes Interface to Just Single IO Reducing Required Pin Count and Enhancing Reliability
  - Unique Factory-Programmed, Unalterable 64-Bit Identification Number
  - Switchpoint Hysteresis and Filtering to Optimize Performance in the Presence of Noise
  - Communicates to Host with a Single Digital Signal at 15.4kbps or 125kbps Using 1-Wire Protocol
  - Reads and Writes over a Wide Voltage Range from 3.0V to 5.25V from -40°C to +85°C
  - ±8kV HBM ESD Protection (typ) for IO Pin

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit



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Absolute Maximum Ratings

IO Voltage Range to GND.....-0.5V to +6V
IO Sink Current.....±10mA
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Lead Temperature (reflow) TO-92 .....+250°C
Lead Temperature (reflow) TDFN, TSOC.....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TSOC
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....127°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....37°C/W
TO-92
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....132°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....4°C/W
TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....55°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....9°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: GENERAL DATA						
1-Wire Pullup Voltage	V_{PUP}	(Note 3)	3.0		5.25	V
1-Wire Pullup Resistance	R_{PUP}	(Note 3, 4)	300		2200	Ω
Input Capacitance	C_{IO}	(Notes 4, 5)		1000		pF
Input Load Current	I_L	IO pin at V_{PUP}	0.05	1.75	6.7	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 6, 7, 8)		0.65 x V_{PUP}		V
Input Low Voltage	V_{IL}	(Notes 3, 9)			0.5	V
Low-to-High Switching Threshold	V_{TH}	(Notes 6, 7, 10)		0.75 x V_{PUP}		V
Switching Hysteresis	V_{HY}	(Notes 6, 7, 11)		0.3		V
Output Low Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 10mA, 4.75V ≤ V_{PUP} ≤ 5.25V			0.5	
Recovery Time (Notes 3, 13)	t_{REC}	Standard speed, R_{PUP} = 2200Ω	5			µs
		Overdrive speed, R_{PUP} = 2200Ω	3			
		Overdrive speed, directly prior to reset pulse, R_{PUP} = 2200Ω	5			
Rising-Edge Hold-off Time (Notes 6, 14)	t_{REH}	Standard speed		1.3		µs
		Overdrive speed		N/A (0)		
Time Slot Duration (Notes 3, 15)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed	9			

Electrical Characteristics (continued)

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

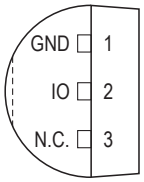
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: 1-Wire RESET, PRESENSE-DETECT CYCLE						
Reset Low Time (Note 3)	t_{RSTL}	Standard speed	480		640	µs
		Overdrive speed	48		80	
Presence Detect High Time	t_{PDH}	Standard speed	15		60	µs
		Overdrive speed	2		6	
Presence Detect Low Time	t_{PDL}	Standard speed	60		240	µs
		Overdrive speed	8		24	
Presence-Detect Sample Time (Notes 3, 16)	t_{MSP}	Standard speed	60		75	µs
		Overdrive speed	6		10	
IO PIN: 1-Wire WRITE						
Write-Zero Low Time (Notes 3, 17)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed	6		15.5	
Write-One Low Time (Notes 3, 17)	t_{W1L}	Standard speed	1		15	µs
		Overdrive speed	0.25		2	
IO PIN: 1-Wire READ						
Read Low Time (Notes 3, 18)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	0.25		2 - δ	
Read Sample Time (Notes 3, 18)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL} + δ		2	
EEPROM						
Programming Current	I_{PROG}	(Notes 6, 19)			1.2	mA
Programming Time	t_{PROG}	(Note 20)			12	ms
Write/Erase Cycles (Endurance)	N_{CY}	T_A = +85°C (Notes 21, 22)	1000			—
Data Retention	t_{DR}	T_A = +85°C (Notes 23, 24, 25)	10			Years

Note 2: Limits are 100% production tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are at T_A = +25°C.
Note 3: System requirement.
Note 4: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times.
Note 5: Maximum value represents the internal parasite capacitance when V_{PUP} is first applied. Once the parasite capacitance is charged, it does not affect normal communication.
Note 6: Guaranteed by design and/or characterization only. Not production tested.
Note 7: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage, which is a function of V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on IO. Lower V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.
Note 8: Voltage below which, during a falling edge on IO, a logic-zero is detected.
Note 9: The voltage on IO must be less than or equal to V_{ILMAX} at all times the master is driving IO to a logic-zero level.
Note 10: Voltage above which, during a rising edge on IO, a logic-one is detected.
Note 11: After V_{TH} is crossed during a rising edge on IO, the voltage on IO must drop by at least V_{HY} to be detected as logic-zero.

Note 13: Applies to a single device attached to a 1-Wire line.
Note 14: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been previously reached.
Note 15: Defines maximum possible bit rate. Equal to $1/(t_{W0LMIN} + t_{RECMIN})$.
Note 16: Interval after t_{RSTL} during which a bus master can read a logic 0 on IO if there is a DS28E07 present. The power-up presence detect pulse could be outside this interval but will be complete within 2ms after power-up.
Note 17: ε in Figure 11 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F - \varepsilon$ and $t_{W0LMAX} + t_F - \varepsilon$, respectively.
Note 18: δ in Figure 11 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input-high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.
Note 19: Current drawn from IO during the EEPROM programming interval. The pullup circuit on IO during the programming interval should be such that the voltage at IO is greater than or equal to V_{PUPMIN}. If V_{PUP} in the system is close to V_{PUPMIN}, a low impedance bypass of R_{PUP}, which can be activated during programming, may need to be added.
Note 20: Interval begins t_{REHMAX} after the trailing rising edge on IO for the last time slot of the E/S byte for a valid Copy Scratchpad sequence. Interval ends once the device's self-timed EEPROM programming cycle is complete and the current drawn by the device has returned from I_{PROG} to I_L.
Note 21: Write-cycle endurance is tested in compliance with JESD47G.
Note 22: Not 100% production tested; guaranteed by reliability monitor sampling.
Note 23: Data retention is tested in compliance with JESD47G.
Note 24: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to the data sheet limit at operating temperature range is established by reliability testing.
Note 25: EEPROM writes can become nonfunctional after the data-retention time is exceeded. Long-term storage at elevated temperatures is not recommended.

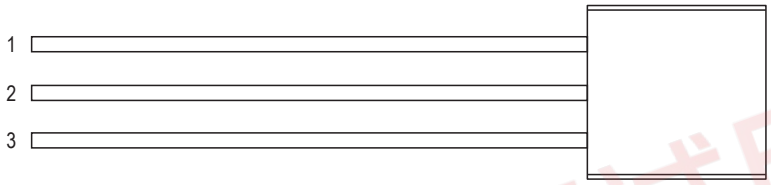
Pin Configurations

SIDE VIEW

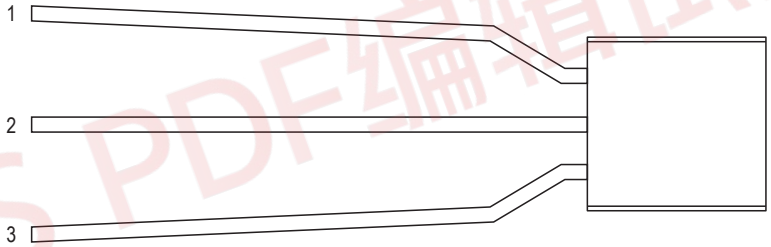


TO-92

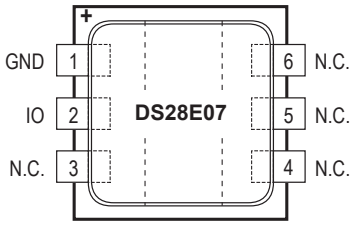
FRONT VIEW



FRONT VIEW (T&R VERSION)

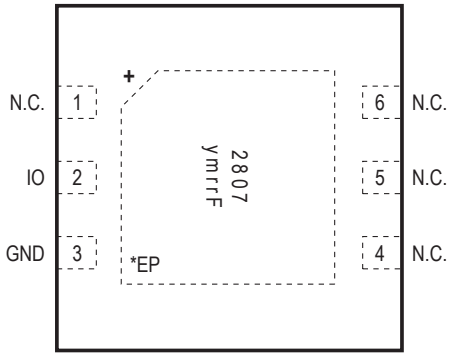


TOP VIEW



TSOC

TOP VIEW



TDFN
(3mm x 3mm)

*EXPOSED PAD

Pin Description

PIN			NAME	FUNCTION
TSOC	TO-92	TDFN-EP		
3, 4, 5, 6	3	1, 4, 5, 6	N.C.	Not Connected
2	2	2	IO	1-Wire Bus Interface. Open-drain signal requires an external pullup resistor.
1	1	3	GND	Ground
—	—	—	EP	Exposed Pad (TDFN Only). Solder evenly to the board's ground plane for proper operation. Refer to Application Note 3273: *Exposed Pads: A Brief Introduction* for additional information.

Detailed Description

The DS28E07 combines 1024 bits of user EEPROM, 64 bits of administrative data memory, and a 64-bit ROM ID in a single chip. Data is transferred serially through the 1-Wire protocol that requires only a single data lead and a ground return. The DS28E07 has an additional memory area called the scratchpad that acts as a buffer when writing to the main memory or the administrative data memory. Data is first written to the scratchpad from which it can be read back. After the data has been verified, a Copy Scratchpad command transfers the data to its final memory location. The user memory can have unrestricted write access (factory default), or can be write protected or put in EPROM emulation mode. Write protection prevents changes to the memory data. EPROM emulation mode logically ANDs memory data with incoming new data, which allows changing bits from 1 to 0, but not vice versa. By changing one bit at a time this mode could be used to create nonvolatile nonresettable counters. For more details, refer to Application Note 5042: *Implementing Nonvolatile*, *Nonresettable Counters for Embedded Systems*. The device's 64-bit ROM ID electronically identifies the equipment in which the DS28E07 is used. The ROM ID guarantees unique identification and is also used to address the device in a multidrop 1-Wire network environment, where multiple devices reside on a common 1-Wire bus and operate independently of each other. DS28E07 applications include accessory/PCB identification, medical sensor calibration data storage, analog sensor calibration including IEEE P1451.4 smart sensors, ink and toner print cartridge identification, and after-market management of consumables.

Overview

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS28E07. The DS28E07 has four main data components: four 32-byte pages of user EEPROM, a 64-bit scratchpad, 64 bit of administrative data memory, and a 64-bit ROM ID.

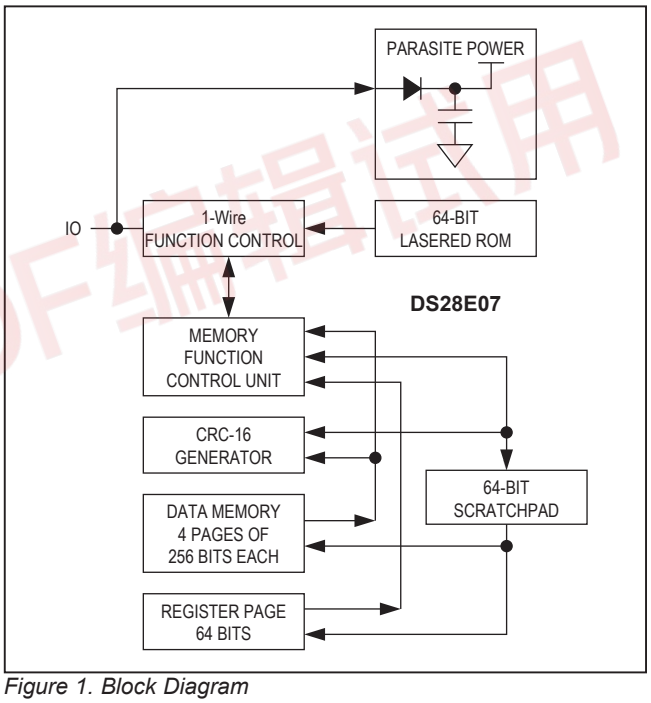


Figure 1. Block Diagram

Figure 2 shows the hierarchical structure of the 1-Wire protocol. The bus master must first provide one of the seven ROM function commands: Read ROM, Match ROM, Search ROM, Skip ROM, Resume, Overdrive-Skip ROM, or Overdrive-Match ROM. Upon completion of an Overdrive-Skip ROM or Overdrive-Match ROM command byte executed at standard speed, the device enters overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 9. After a ROM function command is successfully executed, the memory functions become accessible and the master can provide any one of the four memory function commands. The protocol for these memory function commands is described in Figure 7. **All data is read and written least significant bit first**.

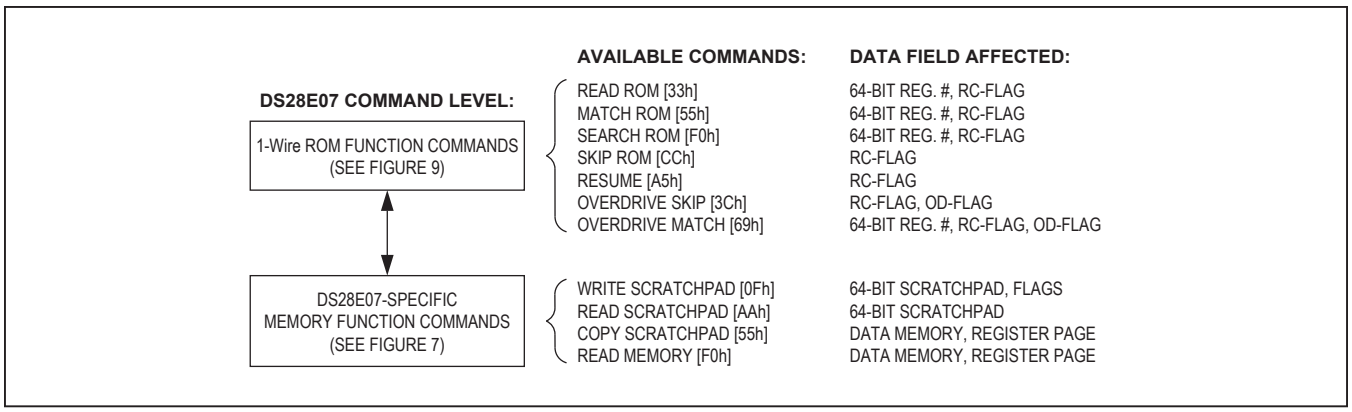


Figure 2. Hierarchical Structure for 1-Wire Protocol

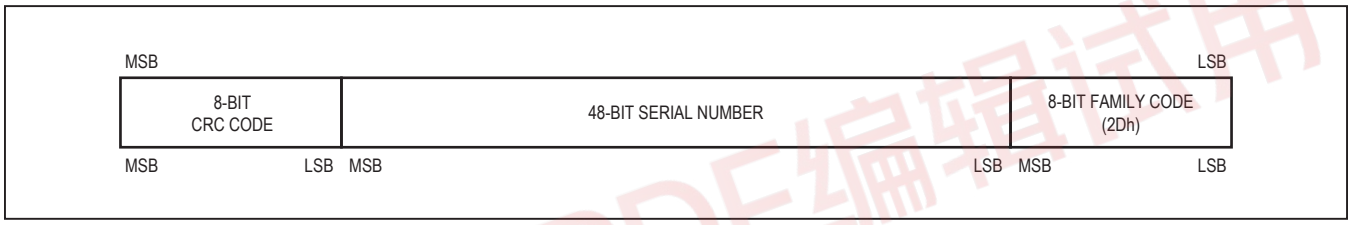


Figure 3. 64-Bit ROM ID

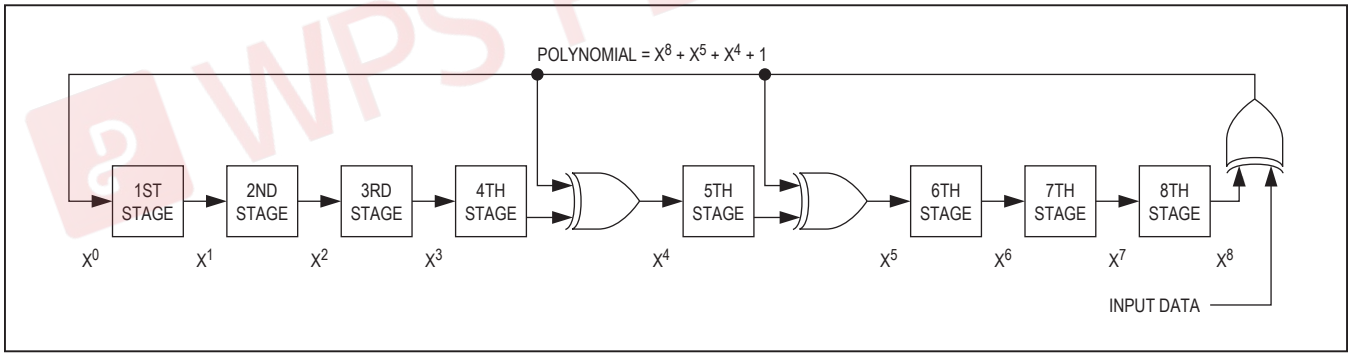


Figure 4. 1-Wire CRC Generator

64-Bit ROM ID

Each DS28E07 contains a unique ROM ID that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a cyclic redundancy check (CRC) of the first 56 bits. See Figure 3 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 1-Wire CRC is available in Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton® Products.*

The shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, the serial number is entered. After the last bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of the CRC returns the shift register to all 0s.

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Memory Resources

The memory of the DS28E07 consists of user memory, administrative data, scratchpad, and a ROM ID. Table 1 shows the size, access mode, and purpose of the various memory areas. Brackets around an access mode indicate possible restrictions, such as write protection or read protection. User memory and administrative data are located in a linear address space, as shown in Figure 5. The user memory and the administrative data have unrestricted read access. Each user memory page can be individually set to open (unprotected), write protected, or EPROM mode by setting the associated protection byte in the administrative data. As a factory default, the entire user memory is unprotected and its contents are undefined. The administrative data consists of 4 protection control bytes, a copy-protection byte, the factory byte, and 2 user byte/manufacture ID bytes. The manufacturer ID can be a customer-supplied identification code that assists the application software in identifying the product the DS28E07 is associated with. Contact the factory to set up and register a custom manufacturer ID. Any data read from addresses 0088 to 00FEh is undefined. Address 00FFh provides read access to a byte that tells the chip revision in hexadecimal notation, e.g., A1h.

Table 1. Memory Resources

NAME	SIZE(BYTES)	ACCESS MODE	PURPOSE
User memory (EEPROM)	128	Read, (write)	Application-specific data storage
Administrative data	8	Read, (write), Internal read	Page protection settings, factory bytes, user bytes/manufacturer ID
Scratchpad	8	Read, write, internal read	Intermediate data storage
ROM ID	8	Read, internal read	1-Wire network device address

ADDRESS RANGE	TYPE	DESCRIPTION	PROTECTION CODES
0000h to 001Fh	R/(W)	User memory Page 0	
0020h to 003Fh	R/(W)	User memory Page 1	
0040h to 005Fh	R/(W)	User memory Page 2	
0060h to 007Fh	R/(W)	User memory Page 3	
0080h*	R/(W)	Protection Control Byte Page 0	55h: Write Protect P0; AAh: EPROM mode P0; 55h or AAh: Write Protect 80h
0081h*	R/(W)	Protection Control Byte Page 1	55h: Write Protect P1; AAh: EPROM mode P1; 55h or AAh: Write Protect 81h
0082h*	R/(W)	Protection Control Byte Page 2	55h: Write Protect P2; AAh: EPROM mode P2; 55h or AAh: Write Protect 82h
0083h*	R/(W)	Protection Control Byte Page 3	55h: Write Protect P3; AAh: EPROM mode P3; 55h or AAh: Write Protect 83h
0084h*	R/(W)	Copy Protection Byte	55h or AAh: Copy Protect 0080:008Fh, and any write-protected Pages
0085h	R	Factory byte. Set at Factory.	AAh:Write Protect 85h, 86h, 87h; 55h: Write Protect 85h, unprotect 86h, 87h
0086h	R/(W)	User Byte/Manufacturer ID	—
0087h	R/(W)	User Byte/Manufacturer ID	—
0088h to 00FEh	R	Reserved	—
00FFh	R	Chip Revision Code	—

**Once programmed to AAh or 55h this address becomes read-only. All other codes can be stored but will neither write protect the address nor activate any function.*

Figure 5. Memory Map

In addition to the main EEPROM array, an 8-byte volatile scratchpad is included. Writes to the EEPROM array are a two-step process. First, data is written to the scratchpad and then copied into the main array. This allows the user to first verify the data written to the scratchpad prior to copying into the main array. The device supports only 8-byte copy operations. For data in the scratchpad to be valid for a copy operation, the address supplied with a Write Scratchpad command must start on an 8-byte boundary, i.e., the three LS-bits of the address must be 000b, and 8 full bytes must be written into the scratchpad.

The protection control bytes determine how incoming data on a Write Scratchpad command is loaded into the scratchpad. A protection setting of 55h (write protect) causes the incoming data to be ignored and the target address main memory data to be loaded into the scratchpad. A protection setting of AAh (EPROM mode) causes the logical AND of incoming data and target address user memory data to be loaded into the scratchpad. Any other protection control byte setting leaves the associated user memory page open for unrestricted write access. Note: For the EPROM mode to function, the entire affected memory page must first be programmed to FFh. Protection-control byte settings of 55h or AAh also write protect the protection-control byte. The protection-control byte setting of 55h does not block the copy. This allows write-protected data to be refreshed (i.e., reprogrammed with the current data) in the device.

The copy-protection byte is used for a higher level of security and should only be used after all other protection control bytes, user bytes, and write-protected pages are set to their final value. If the copy-protection byte is set to 55h or AAh, all copy attempts to the administrative data are blocked. In addition, all copy attempts to write-protected user memory pages (i.e., refresh) are blocked.

Address Registers and Transfer Status

The DS28E07 employs three address registers: TA1, TA2, and E/S (Figure 6). These registers are common to many other 1-Wire devices, but operate slightly differently with the DS28E07. Registers TA1 and TA2 must be loaded with the target address to which the data is written or from which data is read. Register E/S is a read only transfer-status register used to verify data integrity with write commands. E/S bits E[2:0] are loaded with the incoming T[2:0] on a Write Scratchpad command and increment on each subsequent data byte. This is, in effect, a byte-ending offset counter within the 8-byte scratchpad. Bit 5 of the E/S register, called PF, is a logic 1 if the data in the scratchpad is not valid due to a loss of power or if the master sends fewer bytes than needed to reach the end of the scratchpad. For a valid write to the scratchpad, T[2:0] must be 0 and the master must have sent 8 data bytes. Bits 3, 4, and 6 have no function; they always read 0. The highest valued bit of the E/S register, called authorization accepted (AA), acts as a flag to indicate that the data stored in the scratchpad has already been copied to the target memory address. Writing data to the scratchpad clears this flag.

BIT #	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	0	PF	0	0	E2	E1	E0

Figure 6. Address Registers

Writing with Verification

To write data to the DS28E07, the scratchpad must be used as intermediate storage. First, the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. Note that Copy Scratchpad commands must be performed on 8-byte boundaries, i.e., the three LSBs of the target address (T2, T1, T0) must be equal to 000b. If T[2:0] are sent with nonzero values, the copy function is blocked. Under certain conditions (see the Write Scratchpad [0Fh] section) the master receives an inverted CRC-16 of the command, address (actual address sent), and data at the end of the Write Scratchpad command sequence. Knowing this CRC value, the master can compare it to the value it has calculated to decide if the communication was successful and proceed to the Copy Scratchpad command. If the master could not receive the CRC-16, it should send the Read Scratchpad command to verify data integrity. As a preamble to the scratchpad data, the DS28E07 repeats the target address TA1 and TA2 and sends the contents of the E/S register. If the PF flag is set, data did not arrive correctly in the scratchpad, or there was a loss of power since data was last written to the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag together with a cleared PF flag indicates that the device did not recognize the Write command.

If everything went correctly, both flags are cleared. Now the master can continue reading and verifying every data byte. After the master has verified the data, it can send the Copy Scratchpad command, for example. This command must be followed exactly by the data of the three address registers, TA1, TA2, and E/S. The master should obtain the contents of these registers by reading the scratchpad. As well, a strong pullup (i.e., low impedance bypass) turns on after the Copy Scratchpad sequence for the duration of t_{PROG} to enhance power delivery. The strong pullup can comprise an external FET circuitry or by driving logic 1 on the PIO of a host system with a good low-impedance drive strength. If neither option is available then the designer can size R_{PUP} accordingly for proper power delivery as to not violate V_{PUP} minimum.

Memory Function Commands

Figure 7 describes the protocols necessary for accessing the memory of the DS28E07. An example on how to use these functions to write to and read from the device is in the *Memory Function Example* section. The communication between the master and the DS28E07 takes place either at standard speed (default, OD = 0) or at overdrive speed (OD = 1). If not explicitly set into overdrive mode, the DS28E07 assumes standard speed.

Write Scratchpad [0Fh]

The Write Scratchpad command applies to the user memory and the writable addresses of the administrative data. For the scratchpad data to be valid for copying to the array, the user must perform a Write Scratchpad command of 8 bytes starting at a valid row boundary. The Write Scratchpad command accepts invalid addresses and partial rows, but subsequent Copy Scratchpad commands are blocked.

After issuing the Write Scratchpad command, the master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data is written to the scratchpad starting at the byte offset of T[2:0]. The E/S bits E[2:0] are loaded with the starting byte offset and increment with each subsequent byte. Effectively, E[2:0] is the byte offset of the last full byte written to the scratchpad. Only full data bytes are accepted.

When executing the Write Scratchpad command, the CRC generator inside the DS28E07 (Figure 13) calculates a CRC of the entire data stream, starting at the command code and ending at the last data byte as sent by the master. This CRC is generated using the CRC-16 polynomial by first clearing the CRC generator and then shifting in the command code (0Fh) of the Write Scratchpad command, the target addresses (TA1 and TA2), and all the data bytes. Note that the CRC-16 calculation is performed with the actual TA1 and TA2 and data sent by the master. The master can end the Write Scratchpad command at any time. However, if the end of the scratchpad is reached (E[2:0] = 111b), the master can send 16 read time slots and receive the CRC generated by the DS28E07.

If a Write Scratchpad command is attempted to a write-protected location, the scratchpad is loaded with the data already existing in memory rather than the data transmitted. Similarly, if the target address page is in EPROM mode, the scratchpad is loaded with the bitwise logical AND of the transmitted data and data already existing in memory.

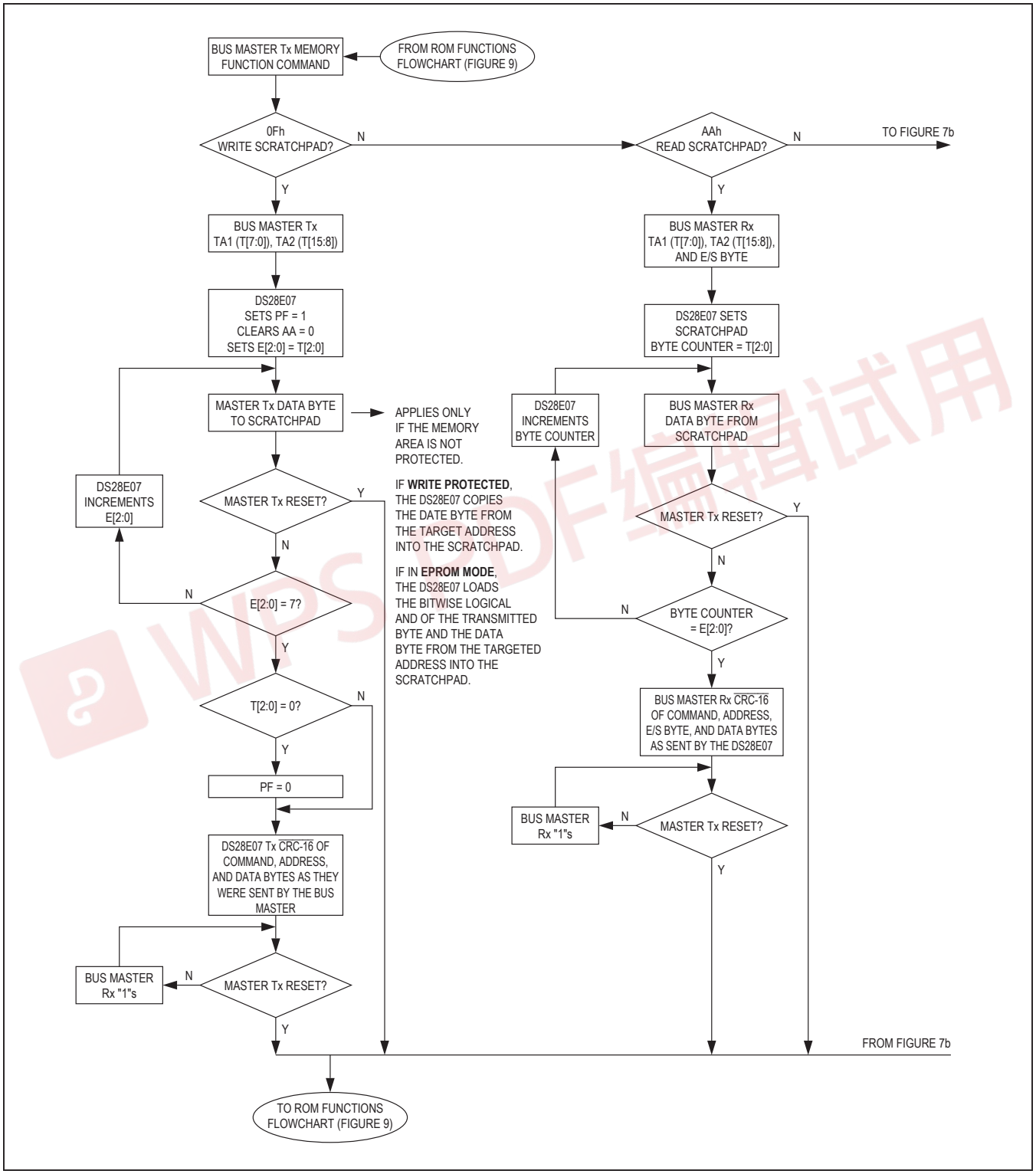


Figure 7a. Memory Function Flowchart

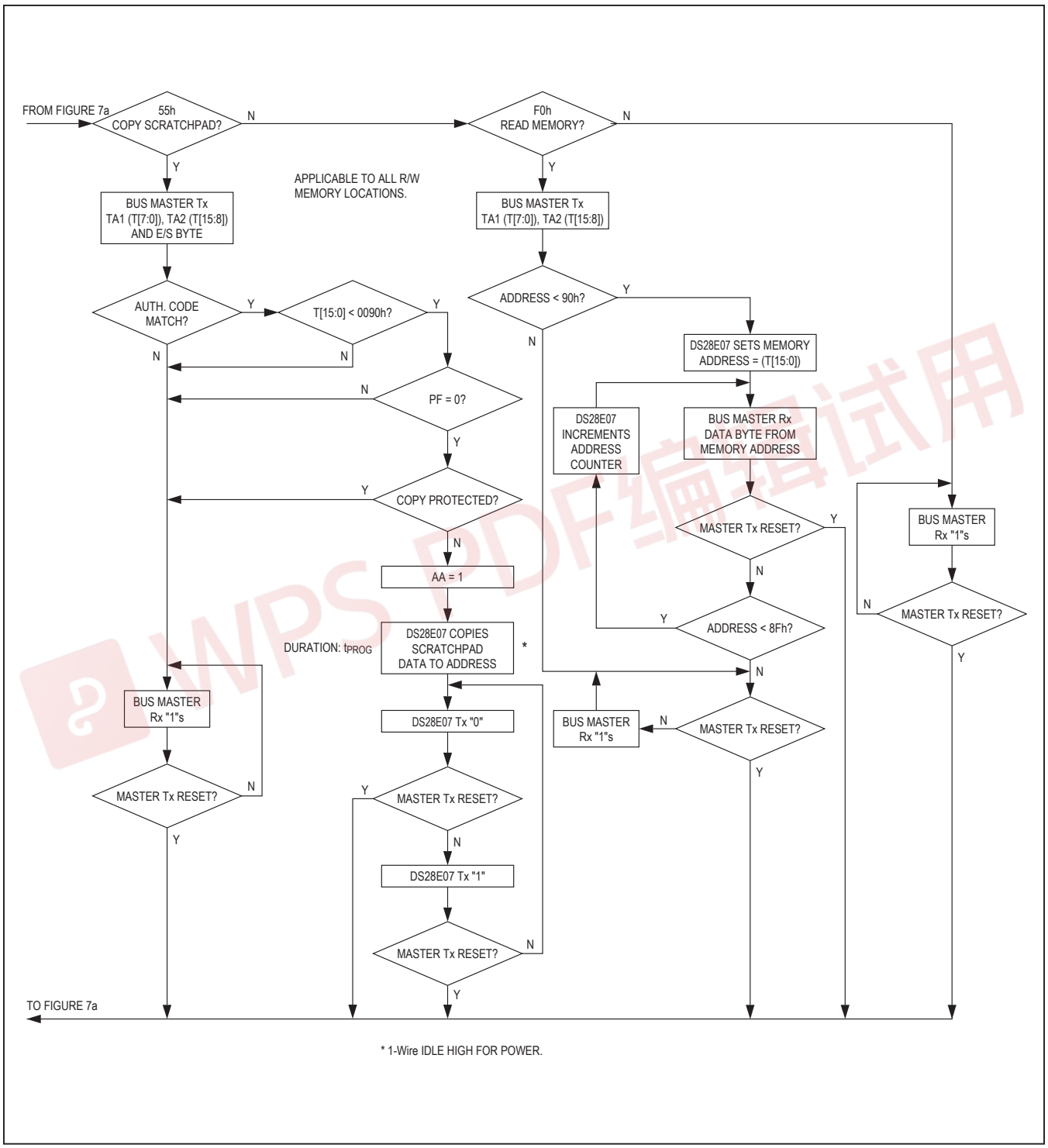


Figure 7b. Memory Function Flowchart (continued)

Read Scratchpad [AAh]

The Read Scratchpad command allows verifying the target address and the integrity of the scratchpad data. After issuing the command code, the master begins reading. The first two bytes are the target address. The next byte is the ending offset/data status byte (E/S) followed by the scratchpad data, which may be different from what the master originally sent. This is of particular importance if the target address is within the administrative data section or a page in either write-protection mode or EPROM mode. See the Write Scratchpad [0Fh] section for details. The master should read through the scratchpad (E[2:0] - T[2:0] + 1 bytes), after which it receives the inverted CRC based on data as it was sent by the DS28E07. If the master continues reading after the CRC, all data is logic 1.

Copy Scratchpad [55h]

The Copy Scratchpad command is used to copy data from the scratchpad to writable memory sections. After issuing the Copy Scratchpad command, the master must provide a 3-byte authorization pattern, which should have been obtained by an immediately preceding Read Scratchpad command. This 3-byte pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the target address is valid, the PF flag is not set, and the target memory is not copy protected, then the AA flag is set and the copy begins. All 8 bytes of scratchpad contents are copied to the target memory location. The duration of the device's internal data transfer is t_{PROG} during which the voltage on the 1-Wire bus must not fall below V_{PUP} minimum. Best practice is to generate a strong pullup that turns on after the Copy Scratchpad sequence for the duration of t_{PROG} to enhance power delivery. A pattern of alternating 0s and 1s are transmitted after the data has been copied until the master issues a reset pulse. If the PF flag is set or the target memory is copy protected, the copy does not begin and the AA flag is not set.

Read Memory [F0h]

The Read Memory command is the general function to read data from the DS28E07. After issuing the command, the master must provide the 2-byte target address. After these 2 bytes, the master reads data beginning from the target address and can continue until address 00FFh. If the master continues reading, the result is logic 1s. The device's internal TA1, TA2, E/S, and scratchpad contents are not affected by a Read Memory command.

1-Wire Bus System

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances, the DS28E07 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots, which are initiated on the falling edge of sync pulses from the bus master.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS28E07 is open drain with an internal circuit equivalent to that shown in Figure 8.

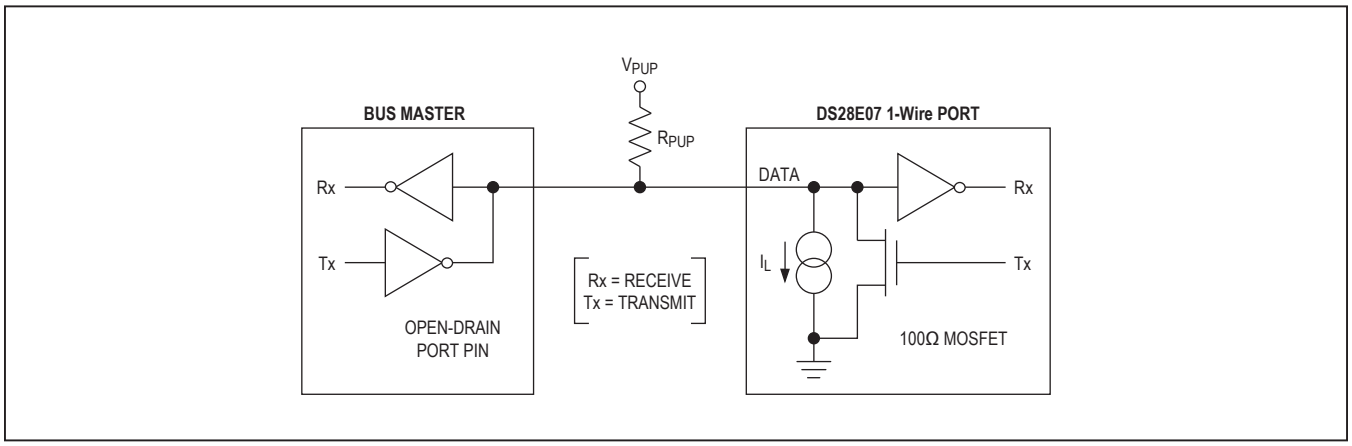


Figure 8. Hardware Configuration

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The DS28E07 supports both a standard and overdrive communication speed of 15.4kbps (max) and 125kbps (max), respectively. The value of the pullup resistor primarily depends on the network size and load conditions. The DS28E07 requires a pullup resistor of 2.2kΩ (max) at any speed.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus must be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 15.5µs (overdrive speed) or more than 120µs (standard speed), one or more devices on the bus could be reset.

Transaction Sequence

The protocol for accessing the DS28E07 through the 1-Wire port is as follows:

- Initialization
- ROM function command
- Memory function command
- Transaction/data

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS28E07 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

1-Wire ROM Function Commands

Once the bus master has detected a presence, it can issue one of the seven ROM function commands that the DS28E07 supports. All ROM function commands are 8 bits long. A list of these commands follows. See Figure 9.

Read ROM [33h]

The Read ROM command allows the bus master to read the DS28E07's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS28E07 on a multidrop bus. Only the DS28E07 that exactly matches the 64-bit ROM sequence responds to the subsequent memory function command. All other slaves wait for a reset pulse. This command can be used with a single device or multiple devices on the bus.

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their ROM ID numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the ID of all slave devices. For each bit in the ID number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its ID number bit. On the second slot, each slave device participating in the search outputs the complemented value of its ID number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the search tree. After one complete pass, the bus master knows the ROM ID number of a single device. Additional passes identify the ID numbers of the remaining devices. Refer to Application Note 187: *1-Wire Search Algorithm* for a detailed discussion, including an example.

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM ID. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

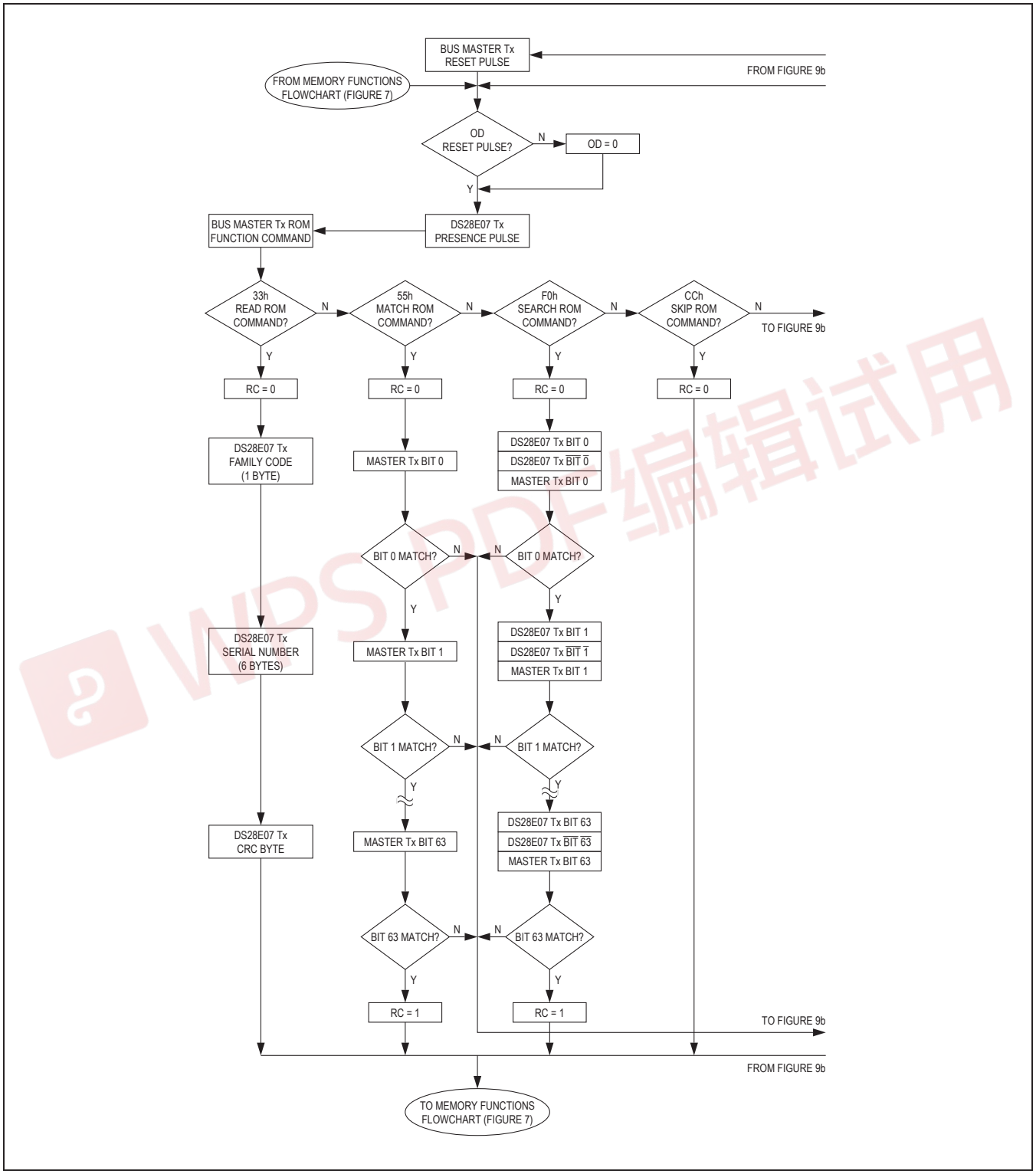


Figure 9a. ROM Functions Flow Chart

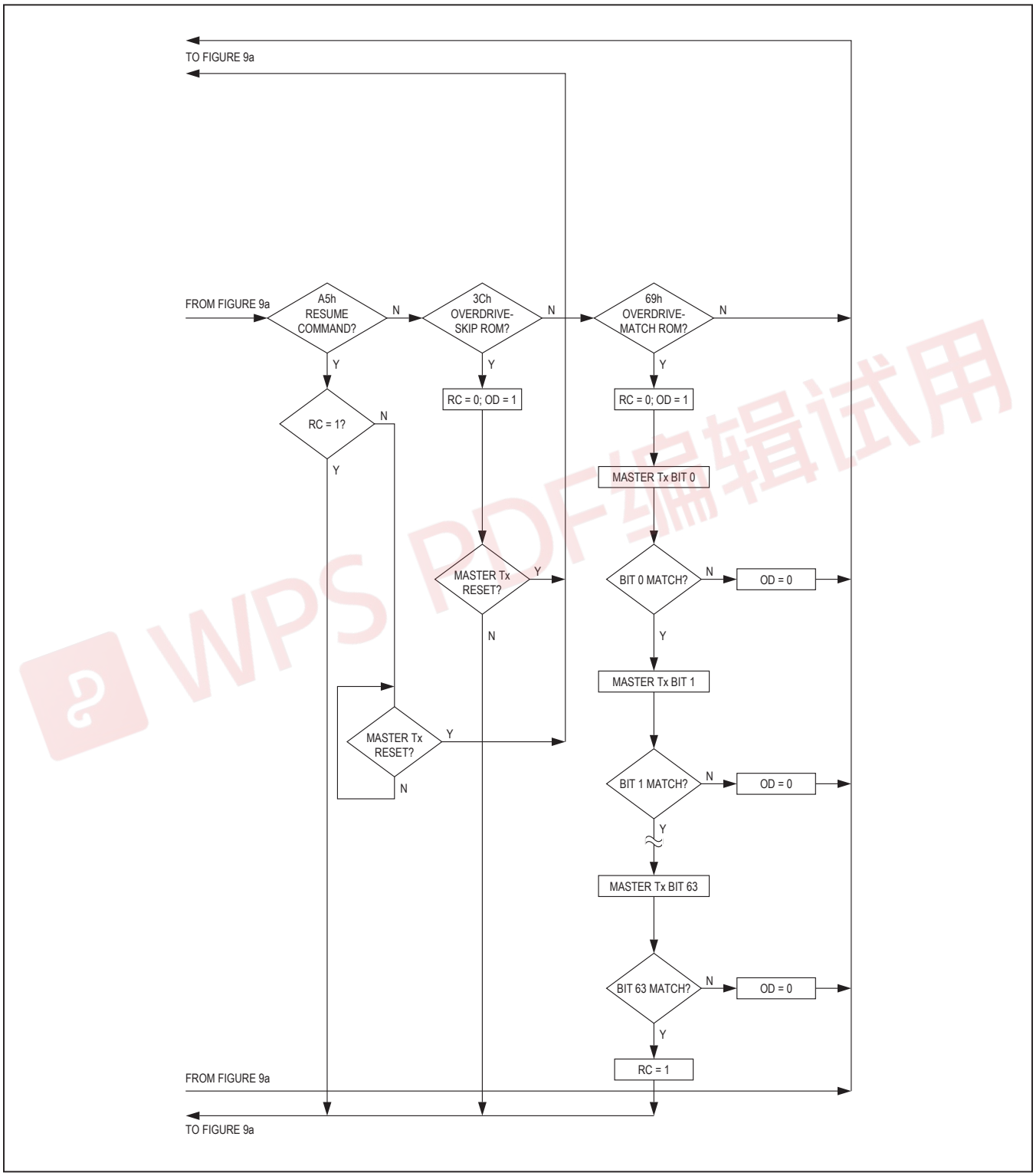


Figure 9b. ROM Functions Flow Chart (continued)

Resume [A5h]

To maximize the data throughput in a multidrop environment, the Resume command is available. This command checks the status of the RC bit and, if it is set, directly transfers control to the memory function commands, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM, or Overdrive-Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command.

Overdrive-Skip ROM [3Ch]

On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit ROM ID. Unlike the normal Skip ROM command, the Overdrive-Skip ROM command sets the DS28E07 into the overdrive mode (OD = 1). All communication following this command must occur at overdrive speed until a reset pulse of minimum 480µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all overdrive-supporting devices into overdrive mode. To subsequently address a specific overdrive-supporting device, a reset pulse at overdrive speed must be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave supporting overdrive is present on the bus and the Overdrive-Skip ROM command is followed by a read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Overdrive-Match ROM [69h]

The Overdrive-Match ROM command followed by a 64-bit ROM sequence transmitted at overdrive speed allows the bus master to address a specific DS28E07 on a multidrop bus and to simultaneously set it in overdrive mode. Only the DS28E07 that exactly matches the 64-bit ROM sequence responds to the subsequent memory function command. Slaves already in overdrive mode from a previous Overdrive-Skip ROM or successful Overdrive-Match ROM command remain in overdrive mode. All overdrive-capable slaves return to standard speed at the next reset pulse of minimum 480µs duration. The Overdrive-Match ROM command can be used with a single device or multiple devices on the bus.

1-Wire Signaling

The DS28E07 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus master initiates all falling edges. The DS28E07 can communicate at two different speeds: standard speed and overdrive speed. If not explicitly set into the overdrive mode, the DS28E07 communicates at standard speed. While in overdrive mode, the fast timing applies to all waveforms.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 10 as ε, and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS28E07 when determining a logical level, not triggering any events.

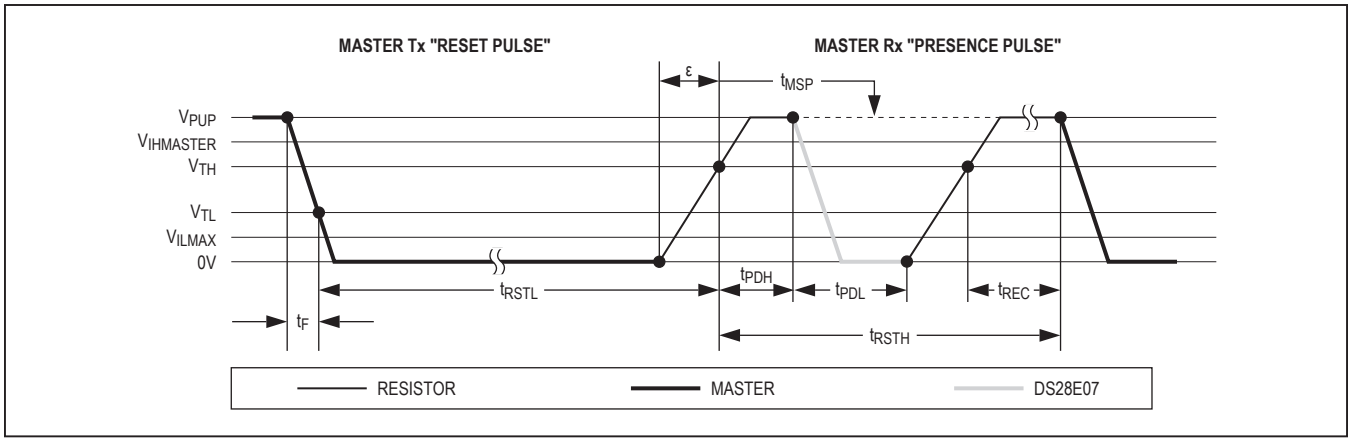


Figure 10. Initialization Procedure: Reset and Presence Pulse

Figure 10 shows the initialization sequence required to begin any communication with the DS28E07. A reset pulse followed by a presence pulse indicates that the DS28E07 is ready to receive data, given the correct ROM and memory function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge. A t_{RSTL} duration of 480µs or longer exits the overdrive mode, returning the device to standard speed. If the DS28E07 is in overdrive mode and t_{RSTL} is no longer than 80µs, the device remains in overdrive mode. If the device is in overdrive mode and t_{RSTL} is between 80µs and 480µs, the device resets, but the communication speed is undetermined.

After the bus master has released the line it goes into receive mode. Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor or, in the case of a special driver chip, through the active circuitry. When the threshold V_{TH} is crossed, the DS28E07 waits for t_{PDH} and then transmits a presence pulse by pulling the line low for t_{PDL}. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

The t_{RSTH} window must be at least the sum of t_{PDHMAX}, t_{PDLMAX}, and t_{RECMIN}. Immediately after t_{RSTH} is expired, the DS28E07 is ready for data communication. In a mixed population network, t_{RSTH} should be extended to minimum 480µs at standard speed and 48µs at overdrive speed to accommodate other 1-Wire devices.

Read/Write Time Slots

Data communication with the DS28E07 takes place in time slots that carry a single bit each. Write time slots transport data from bus master to slave. Read time slots transfer data from slave to master. Figure 11 illustrates the definitions of the write and read time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS28E07 starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

Master-to-Slave

For a **write-one** time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a **write-zero** time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS28E07 needs a recovery time t_{REC} before it is ready for the next time slot.

Slave-to-Master

A **read-data** time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS28E07 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS28E07 does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of $t_{RL} + \delta$ (rise time) on one side and the internal timing generator of the DS28E07 on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}), in which the master must perform a read from the data line. For the most reliable communication, t_{RL} should be as short as permissible, and the master should read close to but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS28E07 to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS28E07 attached to a 1-Wire line. For multidevice configurations, t_{REC} must be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time such as the special 1-Wire line drivers can be used.

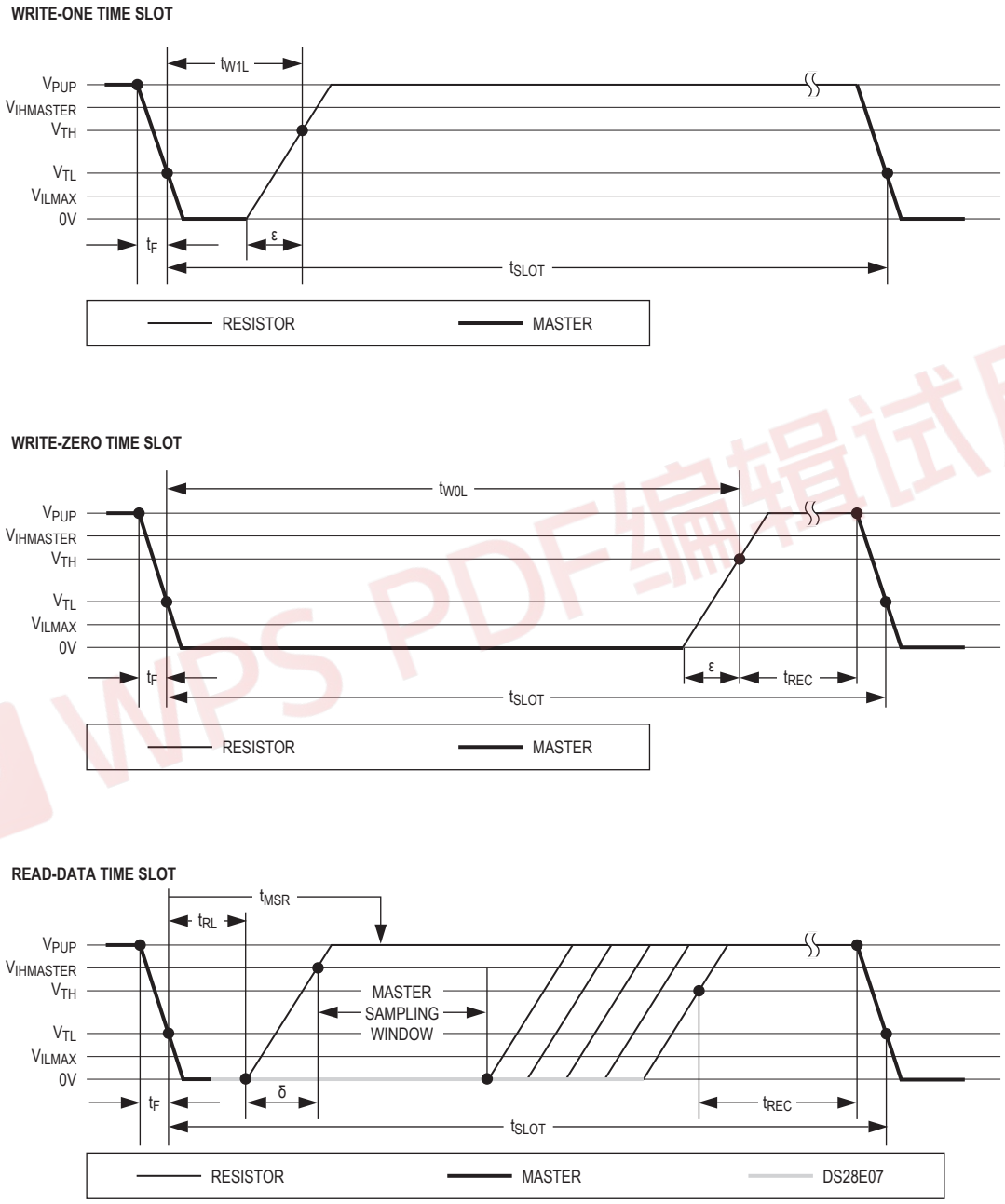


Figure 11. Read/Write Timing Diagrams

Improved Network Behavior (Switchpoint Hysteresis)

In a 1-Wire environment, line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, consequently, result in a Search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS28E07 uses a 1-Wire front-end that is less sensitive to noise.

The DS28E07's 1-Wire front-end has the following features:

1) There is additional lowpass filtering in the circuit that detects the falling edge at the beginning of a time slot. This reduces the sensitivity to high-frequency noise. This additional filtering does not apply at overdrive speed.
2) There is a hysteresis at the low-to-high switching threshold V_{TH}. If a negative glitch crosses V_{TH} but does not go below V_{TH} - V_{HY}, it is not recognized (Figure 12, Case A). The hysteresis is effective at any 1-Wire speed.
3) There is a time window specified by the rising edge hold-off time t_{REH} during which glitches are ignored, even if they extend below the V_{TH} - V_{HY} threshold (Figure 12, Case B, $t_{GL} < t_{REH}$). Deep voltage drops or glitches that appear late after crossing the V_{TH} threshold and extend beyond the t_{REH} window cannot be filtered out and are taken as the beginning of a new time slot (Figure 12, Case C, $t_{GL} \geq t_{REH}$).

CRC Generation

The DS28E07 uses two different types of CRCs. One CRC is an 8-bit type and is stored in the most significant byte of the 64-bit ROM ID. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM ID and compare it to the value stored within the DS28E07 to determine if the ROM data has been received error-free. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (non-inverted) form.

The other CRC is a 16-bit type, generated according to the standardized CRC-16 polynomial function $X^{16} + X^{15} + X^2 + 1$. This CRC is used for fast verification of a data transfer when writing to or reading from the scratchpad. In contrast to the 8-bit CRC, the 16-bit CRC is always communicated in the inverted form. A CRC generator inside the DS28E07 chip (Figure 13) calculates a new 16- bit CRC, as shown in the command flowchart (Figure 7). The bus master compares the CRC value read from the device to the one it calculates from the data and decides whether to continue with an operation or to reread the portion of the data with the CRC error.

With the Write Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, and all the data bytes as they were sent by the bus master. The DS28E07 transmits this CRC only if E[2:0] = 111b.

With the Read Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, the E/S byte, and the scratchpad data as they were sent by the DS28E07. The DS28E07 transmits this CRC only if the reading continues through the end of the scratchpad. For more information on generating CRC values, refer to Application Note 27.

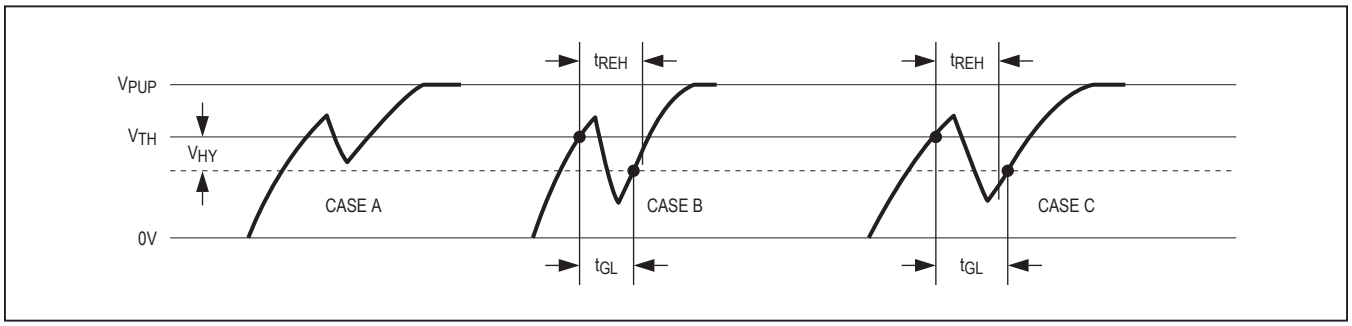


Figure 12. Noise Suppression Scheme

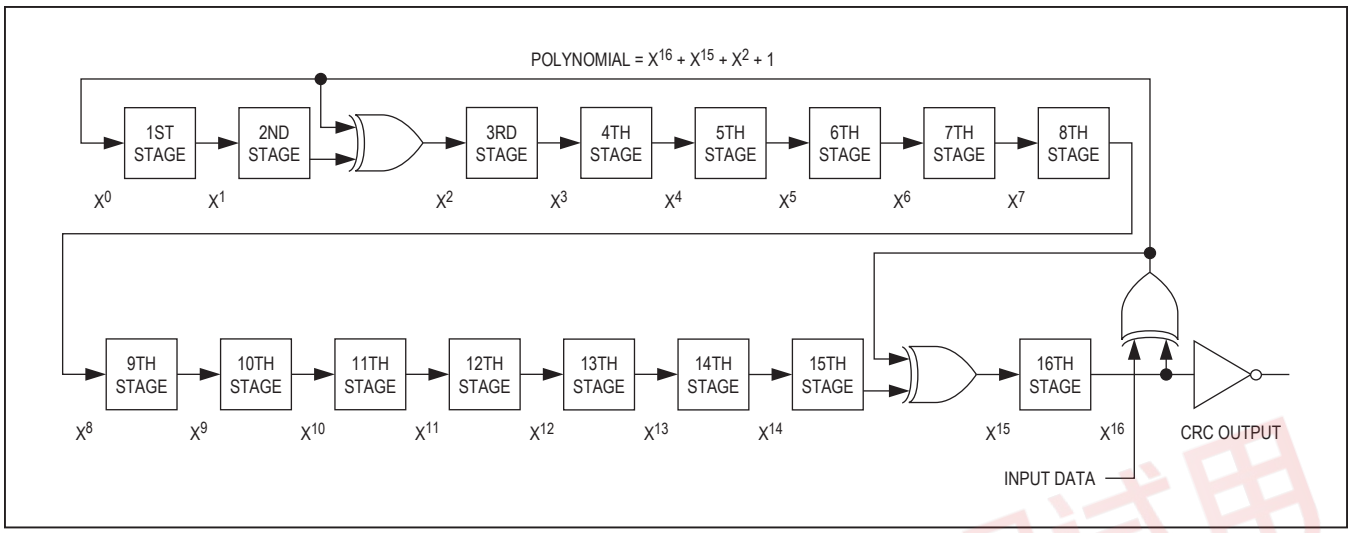


Figure 13. CRC-16 Hardware Description and Polynomial

Command-Specific 1-Wire Communication Protocol—Color Codes

Master to Slave	Slave to Master	Programming

Command-Specific 1-Wire Communication Protocol—Legend

SYMBOL	DESCRIPTION
RST	1-Wire Reset Pulse generated by master.
PD	1-Wire Presence Pulse generated by slave.
Select	Command and data to satisfy the ROM function protocol (e.g. Skip ROM [CCh], etc…).
WS	Command “Write Scratchpad [0Fh]”.
RS	Command “Read Scratchpad [AAh]”.
CPS	Command “Copy Scratchpad [55h]”.
RM	Command “Read Memory [F0h]”.
TA	Target Address TA1, TA2.
TA-E/S	Target Address TA1, TA2 with E/S byte.
<8 – T2:T0 bytes>	Transfer of as many bytes as needed to reach the end of the scratchpad for a given target address.
<data to EOM>	Transfer of as many data bytes as are needed to reach the end of the memory.
$\overline{\text{CRC16}}$	Transfer of an inverted $\overline{\text{CRC16}}$.
FF loop	Indefinite loop where the master reads FF bytes.
AA loop	Indefinite loop where the master reads AA bytes.
Programming	Data transfer to EEPROM; no activity on the 1-Wire bus permitted during this time.

1-Wire Communication Examples

Write Scratchpad (CANNOT FAIL)

RST	PD	Select	WS	TA	<8 – T2:T0 bytes>	$\overline{\text{CRC16}}$	FF loop

Read Scratchpad (CANNOT FAIL)

RST	PD	Select	RS	TA-E/S	<8 – T2:T0 bytes>	$\overline{\text{CRC16}}$	FF loop

Copy Scratchpad (success)

RST	PD	Select	CPS	TA-E/S	Programming	AA loop

Copy Scratchpad (invalid ADDRESS or PF = 1 or COPY protected)

RST	PD	Select	CPS	TA-E/S	FF loop

Read Memory (success)

RST	PD	Select	RM	TA	<data to EOM>	FF loop

Read Memory (invalid address)

RST	PD	Select	RM	TA	FF loop

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS28E07+	-40°C to +85°C	3 TO-92
DS28E07+T	-40°C to +85°C	3 TO-92 (2k pcs)
DS28E07P+	-40°C to +85°C	6 TSOC
DS28E07P+T	-40°C to +85°C	6 TSOC (4k pcs)
DS28E07Q+T	-40°C to +85°C	6 TDFN-EP* (2.5k pcs)

+Denotes a lead-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
3 TO-92 (Bulk)	Q3+1	**21-0248**	—
3 TO-92 (T&R)	Q3+4	**21-0250**	—
6 TSOC	D6+1	**21-0382**	**90-0321**
6 TDFN-EP	T633+2	**21-0137**	**90-0058**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/15	Initial release	—
1	5/16	Removed future product references	22
2	1/17	Added row to Output Low Voltage parameter and removed Note 12 (remaining Notes were not renumbered per request)	2, 4

DS28EC20
20Kb 1-Wire EEPROM

GENERAL DESCRIPTION

The DS28EC20 is a 20480-bit, 1-Wire® EEPROM organized as 80 memory pages of 256 bits each. An additional page is set aside for control functions. Data is written to a 32-byte scratchpad, verified, and then copied to the EEPROM memory. As a special feature, blocks of eight memory pages can be write protected or put in EPROM-Emulation mode, where bits can only be changed from a 1 to a 0 state. The DS28EC20 communicates over the single-conductor 1-Wire bus. The communication follows the standard 1-Wire protocol. Each device has its own unalterable and unique 64-bit ROM registration number. The registration number is used to address the device in a multidrop 1-Wire net environment.

APPLICATIONS

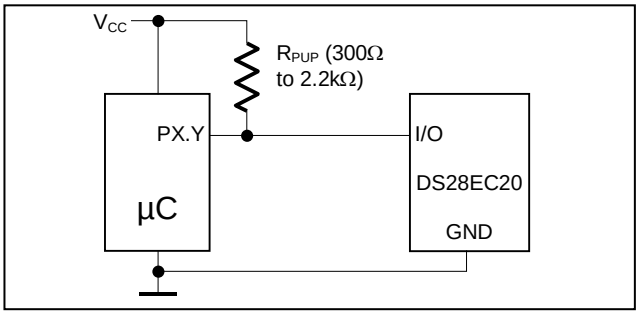
Device Authentication
IEEE 1451.4 Sensor TEDS
Ink/Toner Cartridges
Medical Sensors
PCB Identification
Wireless Base Stations

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS28EC20+	-40°C to +85°C	3 TO-92
DS28EC20+T	-40°C to +85°C	3 TO-92, T&R
DS28EC20P+	-40°C to +85°C	6 TSOC
DS28EC20P+T	-40°C to +85°C	6 TSOC, T&R
DS28EC20Q+T	-40°C to +85°C	6 TDFN, T&R

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

TYPICAL OPERATING CIRCUIT



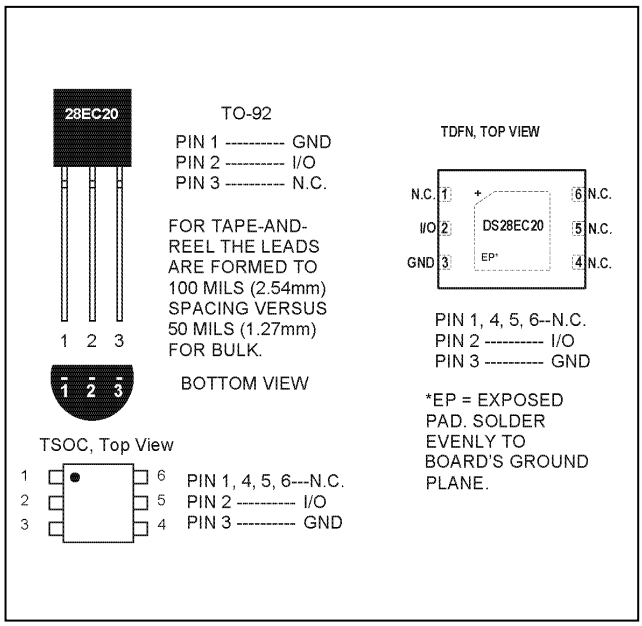
Commands, bytes, and modes are capitalized for clarity.

1-Wire is a registered trademark of Maxim Integrated Products, Inc.

FEATURES

- 20480 Bits of Nonvolatile (NV) EEPROM Partitioned into Eighty 256-Bit Pages
- Individual 8-Page Groups of Memory Pages (Blocks) can be Permanently Write Protected or Put in OTP EPROM-Emulation Mode ("Write to 0")
- Read and Write Access Highly Backward-Compatible to Legacy Devices (e.g., DS2433)
- 256-Bit Scratchpad with Strict Read/Write Protocols Ensures Integrity of Data Transfer
- 200k Write/Erase Cycle Endurance at +25°C
- Unique Factory-Programmed 64-Bit Registration Number Ensures Error-Free Device Selection and Absolute Part Identity
- Switchpoint Hysteresis and Filtering to Optimize Performance in the Presence of Noise
- Communicates to Host at 15.4kbps or 90kbps Using 1-Wire Protocol
- Low-Cost TO-92 Package
- Operating Range: 4V to 5.25V, -40°C to +85°C
- Operating Range: 3.135V to3.465V, 0°C to +70°C (Standard Speed only)
- IEC 1000-4-2 Level 4 ESD Protection (±8kV Contact, ±15kV Air, Typical) for I/O Pin

PIN CONFIGURATION



19-6067; Rev 7; 9/17

ABSOLUTE MAXIMUM RATINGS

I/O Voltage to GND	-0.5V, +6V
I/O Sink Current	20mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	
TO-92	+250°C
TSOC, TDFN	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.0V SUPPLY ELECTRICAL CHARACTERISTICS

(V_{PUP} = 4V to 5.25, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O PIN GENERAL DATA						
1-Wire Pullup Resistance	R_{PUP}	(Notes 2, 3)	0.3		2.2	kΩ
Input Capacitance	C_{IO}	(Notes 4, 5)		2000		pF
Input Load Current	I_L	I/O pin at V_{PUP}	0.05		3.5	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 5, 6, 7)	1.6		V_{PUP} - 1.8	V
Input Low Voltage	V_{IL}	(Notes 2, 8)			0.5	V
Low-to-High Switching Threshold	V_{TH}	(Notes 5, 6, 9)	2.5		V_{PUP} - 1.1	V
Switching Hysteresis	V_{HY}	(Notes 5, 6, 10)	0.30		1.30	V
Output Low Voltage	V_{OL}	At 4mA (Note 11)			0.20	V
Recovery Time (Notes 2, 12)	t_{REC}	Standard speed	5			µs
		Overdrive speed	5			
Rising-Edge Hold-off Time (Notes 5, 13)	t_{REH}	Standard speed	0.5		5.0	µs
		Overdrive speed	Not applicable (0)			
Timeslot Duration (Notes 2, 14)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed	11			
I/O PIN, 1-Wire RESET, PRESENCE DETECT CYCLE						
Reset-Low Time (Note 2)	t_{RSTL}	Standard speed	480		640	µs
		Overdrive speed	48		80	
Presence-Detect High Time	t_{PDH}	Standard speed	15		60	µs
		Overdrive speed	2		6	
Presence-Detect Low Time	t_{PDL}	Standard speed	60		240	µs
		Overdrive speed	8		24	
Presence-Detect Sample Time (Notes 2, 15)	t_{MSP}	Standard speed	60		75	µs
		Overdrive speed	6		10	
I/O PIN, 1-Wire WRITE						
Write-0 Low Time (Notes 2, 16, 17)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed	6		15.5	
Write-1 Low Time (Notes 2, 17)	t_{W1L}	Standard speed	1		15	µs
		Overdrive speed	1		2	
I/O PIN, 1-Wire READ						
Read-Low Time (Notes 2, 18)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	0.800		2 - δ	
Read-Sample Time (Notes 2, 18)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL} + δ		2.27	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM						
Programming Current	I_{PROG}	(Note 19)			0.9	mA
Programming Time	t_{PROG}	(Note 20)			10	ms
Write/Erase Cycles (Endurance) (Notes 21, 22)	N_{CY}	At +25°C	200k			—
		At +85°C (worst case)	50k			
Data Retention (Notes 23, 24, 25)	t_{DR}	At +85°C (worst case)	40			years

Note 1: Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.
Note 2: System requirement.
Note 3: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system, 1-Wire recovery times, and current requirements during EEPROM programming. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2482-x00, DS2480B, or DS2490 may be required.
Note 4: Typical value represents the internal parasite capacitance when V_{PUP} is first applied. Once the parasite capacitance is charged, it does not affect normal communication.
Note 5: Guaranteed by design, characterization and/or simulation only. Not production tested.
Note 6: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage which is itself a function of V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on I/O. Lower V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.
Note 7: Voltage below which, during a falling edge on I/O, a logic 0 is detected.
Note 8: The voltage on I/O needs to be less or equal to V_{ILMAX} at all times the master is driving I/O to a logic 0 level.
Note 9: Voltage above which, during a rising edge on I/O, a logic 1 is detected.
Note 10: After V_{TH} is crossed during a rising edge on I/O, the voltage on I/O has to drop by at least V_{HY} to be detected as logic 0.
Note 11: The I-V characteristic is approximately linear for voltages less than 1V.
Note 12: Applies to a single device attached to a 1-Wire line.
Note 13: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been reached on the preceding rising edge.
Note 14: Defines maximum possible bit rate. Equal to $1/(t_{W0LMIN} + t_{RECMIN})$.
Note 15: Interval after t_{RSTL} during which a bus master can read a logic 0 on I/O if there is a DS28EC20 present. The power-up presence detect pulse could be outside this interval but will be complete within 2ms after power-up.
Note 16: Highlighted numbers are NOT in compliance with legacy 1-Wire product standards. See comparison table below.
Note 17: ε in Figure 11 represents the time required for the pullup circuitry to pull the voltage on I/O up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F - \varepsilon$ and $t_{W0LMAX} + t_F - \varepsilon$, respectively.
Note 18: δ in Figure 11 represents the time required for the pullup circuitry to pull the voltage on I/O up from V_{IL} to the input high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.
Note 19: Current drawn from I/O during the EEPROM programming interval. During a programming cycle the voltage at I/O drops by $I_{PROG} \times R_{PUP}$ below V_{PUP}. If V_{PUP} and R_{PUP} are within their EC table limits, the residual I/O voltage meets the guaranteed-by-design minimum voltage requirements for programming.
Note 20: The t_{PROG} interval begins t_{REHMAX} after the trailing rising edge on I/O for the last time slot of the E/S byte for a valid copy scratchpad sequence. Interval ends once the device's self-timed EEPROM programming cycle is complete and the current drawn by the device has returned from I_{PROG} to I_L.
Note 21: Write-cycle endurance is degraded as T_A increases.
Note 22: Not 100% production-tested; guaranteed by reliability monitor sampling.
Note 23: Data retention is degraded as T_A increases.
Note 24: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to data sheet limit at operating temperature range is established by reliability testing.
Note 25: EEPROM writes may become nonfunctional after the data retention time is exceeded. Long-time storage at elevated temperatures is not recommended; the device may lose its write capability after 10 years at +125°C or 40 years at +85°C.

PARAMETER	LEGACY VALUES				DS28EC20 VALUES			
	STANDARD SPEED		OVERDRIVE SPEED#		STANDARD SPEED		OVERDRIVE SPEED#	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
t_{SLOT} (incl. t_{REC})	61µs	(undefined)	7µs	(undefined)	65µs*	(undefined)	11µs	(undefined)
t_{RSTL}	480µs	(undefined)	48µs	80µs	480µs	640µs	48µs	80µs
t_{PDH}	15µs	60µs	2µs	6µs	15µs	60µs	2µs	6µs
t_{PDL}	60µs	240µs	8µs	24µs	60µs	240µs	8µs	24µs
t_{W0L}	60µs	120µs	6µs	16µs	60µs	120µs	6µs	15.5µs

**Intentional change, longer recovery time requirement due to modified 1-Wire front-end.*
#For operation at overdrive speed, the DS28EC20 requires V_{PUP} to be between 4V and 5.25V.

3.3V SUPPLY ELECTRICAL CHARACTERISTICS

(V_{PUP} = 3.3V ±5%, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O PIN GENERAL DATA						
1-Wire Pullup Resistance	R_{PUP}	(Notes 1, 2)	0.3		2.2	kΩ
Input Capacitance	C_{IO}	(Notes 3, 4)		2000		pF
Input Load Current	I_L	I/O pin at V_{PUP}	0.05		3.5	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 4, 5, 6)	0.49		V_{PUP} - 1.9	V
Input Low Voltage	V_{IL}	(Notes 1, 7)			0.5	V
Low-to-High Switching Threshold	V_{TH}	(Notes 4, 5, 8)	1.09		V_{PUP} - 1.1	V
Switching Hysteresis	V_{HY}	(Notes 4, 5, 9)	0.33		0.70	V
Output Low Voltage	V_{OL}	At 4mA (Note 10)			0.30	V
Recovery Time	t_{REC}	Standard speed (Notes 1, 11)	5			µs
Rising-Edge Hold-off Time	t_{REH}	Standard speed (Notes 4, 12)	0.5		5.0	µs
Timeslot Duration	t_{SLOT}	Standard speed (Notes 1, 13)	65			µs
I/O PIN, 1-Wire RESET, PRESENCE DETECT CYCLE						
Reset-Low Time	t_{RSTL}	Standard speed (Note 1)	480		640	µs
Presence-Detect High Time	t_{PDH}	Standard speed	15		60	µs
Presence-Detect Low Time	t_{PDL}	Standard speed	60		240	µs
Presence-Detect Sample Time	t_{MSP}	Standard speed (Notes 1, 14)	60		75	µs
I/O PIN, 1-Wire WRITE						
Write-0 Low Time	t_{W0L}	Standard speed (Notes 1, 15)	60		120	µs
Write-1 Low Time	t_{W1L}	Standard speed (Notes 1, 15)	1		15	µs
I/O PIN, 1-Wire READ						
Read-Low Time	t_{RL}	Standard speed (Notes 1, 16)	5		15 - δ	µs
Read-Sample Time	t_{MSR}	Standard speed (Notes 1, 16)	t_{RL} + δ		15	µs
EEPROM						
Programming Current	I_{PROG}	(Note 17)			0.9	mA
Programming Time	t_{PROG}	(Note 18)			10	ms
Write/Erase Cycles (Endurance) (Notes 19, 20)	N_{CY}	At +25°C	200k			—
		At +70°C	50k			
Data Retention	t_{DR}	(Notes 21, 22, 23)	40			years

Note 1: System requirement.

Note 2: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system, 1-Wire recovery times, and current requirements during EEPROM programming. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2482-x00, DS2480B, or DS2490 may be required.

Note 3: Typical value represents the internal parasite capacitance when V_{PUP} is first applied. Once the parasite capacitance is charged, it does not affect normal communication.

Note 4: Guaranteed by design, characterization and/or simulation only. Not production tested.

Note 5: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage which is itself a function of V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on I/O. Lower V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.

Note 6: Voltage below which, during a falling edge on I/O, a logic 0 is detected.

Note 7: The voltage on I/O needs to be less or equal to V_{ILMAX} at all times the master is driving I/O to a logic 0 level.

Note 8: Voltage above which, during a rising edge on I/O, a logic 1 is detected.

Note 9: After V_{TH} is crossed during a rising edge on I/O, the voltage on I/O has to drop by at least V_{HY} to be detected as logic 0.

Note 10: The I-V characteristic is approximately linear for voltages less than 1V.

Note 11: Applies to a single device attached to a 1-Wire line.

Note 12: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been reached on the preceding rising edge.

Note 13: Defines maximum possible bit rate. Equal to $1/(t_{W0LMIN} + t_{RECMIN})$.

Note 14: Interval after t_{RSTL} during which a bus master can read a logic 0 on I/O if there is a DS28EC20 present. The power-up presence detect pulse could be outside this interval but will be complete within 2ms after power-up.

Note 15: ε in Figure 11 represents the time required for the pullup circuitry to pull the voltage on I/O up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F - \varepsilon$ and $t_{W0LMAX} + t_F - \varepsilon$, respectively.

Note 16: δ in Figure 11 represents the time required for the pullup circuitry to pull the voltage on I/O up from V_{IL} to the input high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.

Note 17: Current drawn from I/O during the EEPROM programming interval. The pullup circuit on I/O during the programming interval should be such that the voltage at I/O is greater than or equal to 3.0V. For 3.3V±5% V_{PUP} operation of the DS28EC20, a low-impedance bypass of R_{PUP}, which can be activated during programming, is required.

Note 18: The t_{PROG} interval begins t_{REHMAX} after the trailing rising edge on I/O for the last time slot of the E/S byte for a valid copy scratchpad sequence. Interval ends once the device's self-timed EEPROM programming cycle is complete and the current drawn by the device has returned from I_{PROG} to I_L.

Note 19: Write-cycle endurance is degraded as T_A increases.

Note 20: Not 100% production-tested; guaranteed by reliability monitor sampling.

Note 21: Data retention is degraded as T_A increases.

Note 22: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to data sheet limit at operating temperature range is established by reliability testing.

Note 23: EEPROM writes may become nonfunctional after the data retention time is exceeded. Long-time storage at elevated temperatures is not recommended; the device may lose its write capability after 10 years at +125°C or 40 years at +85°C.

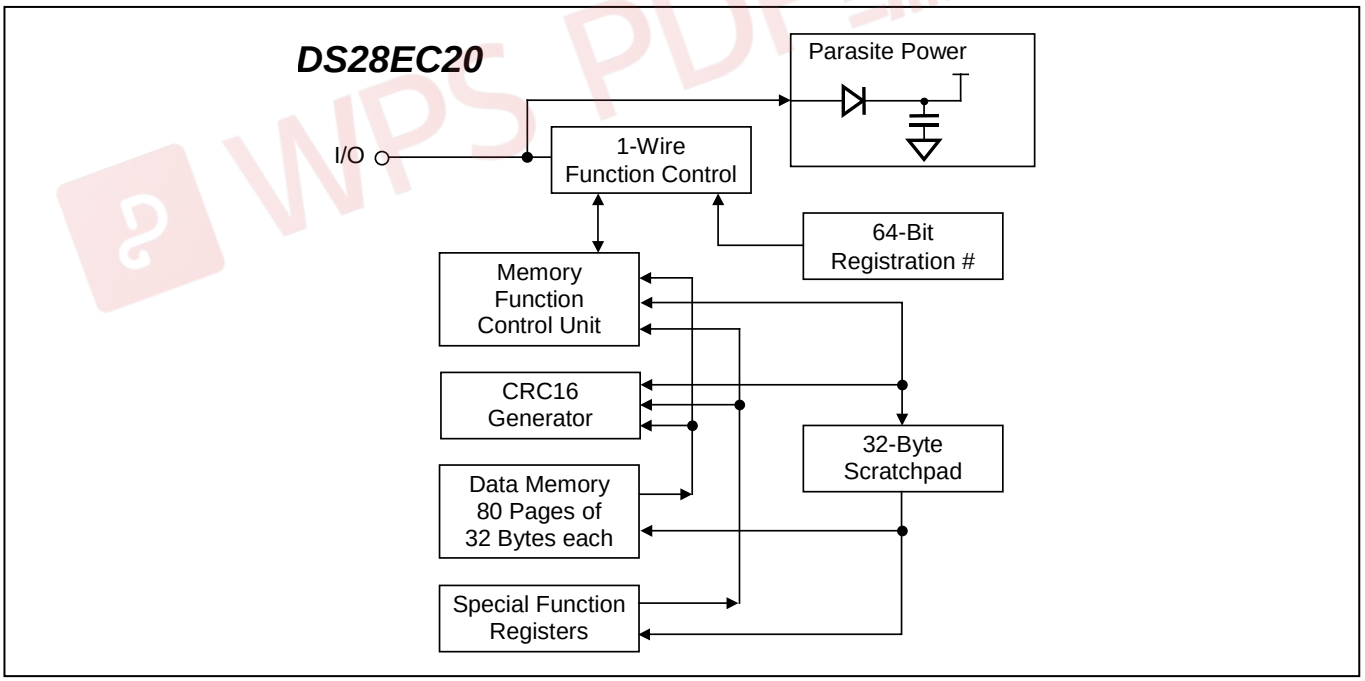
PIN DESCRIPTION

NAME	FUNCTION
I/O	1-Wire Bus Interface. Open drain, requires external pullup resistor.
GND	Ground Reference
N.C.	Not Connected

DESCRIPTION

The DS28EC20 combines 20Kb of data EEPROM with a fully featured 1-Wire interface in a single chip. The memory is organized as 80 pages of 256 bits each. In addition, the device has one page for control functions such as permanent write protection and EPROM-Emulation mode for individual 2048-bit (8-page) memory blocks. A volatile 256-bit memory page called the scratchpad acts as a buffer when writing data to the EEPROM to ensure data integrity. Data is first written to the scratchpad, from which it can be read back for verification before transferring it to the EEPROM. The operation of the DS28EC20 is controlled over the single-conductor 1-Wire bus. Device communication follows the standard 1-Wire protocol. The energy required to read and write the DS28EC20 is derived entirely from the 1-Wire communication line. Each DS28EC20 has its own unalterable and unique 64-bit registration number. The registration number guarantees unique identification and is used to address the device in a multidrop 1-Wire net environment. Multiple DS28EC20 devices can reside on a common 1-Wire bus and be operated independently of each other. Applications of the DS28EC20 include device authentication, analog-sensor calibration such as IEEE-P1451.4 Smart Sensors TEDS, ink and toner print cartridge identification, medical-sensor calibration data storage, PC board identification, and data for self-configuration of central office switches, wireless base stations, PBXs, or other modular-based rack systems. The DS28EC20 provides a high degree of backward compatibility with the DS2433. Besides the different family codes, the only protocol change that is required on an existing DS2433 implementation is a lengthening of the programming duration (t_{PROG}) from 5ms to 10ms.

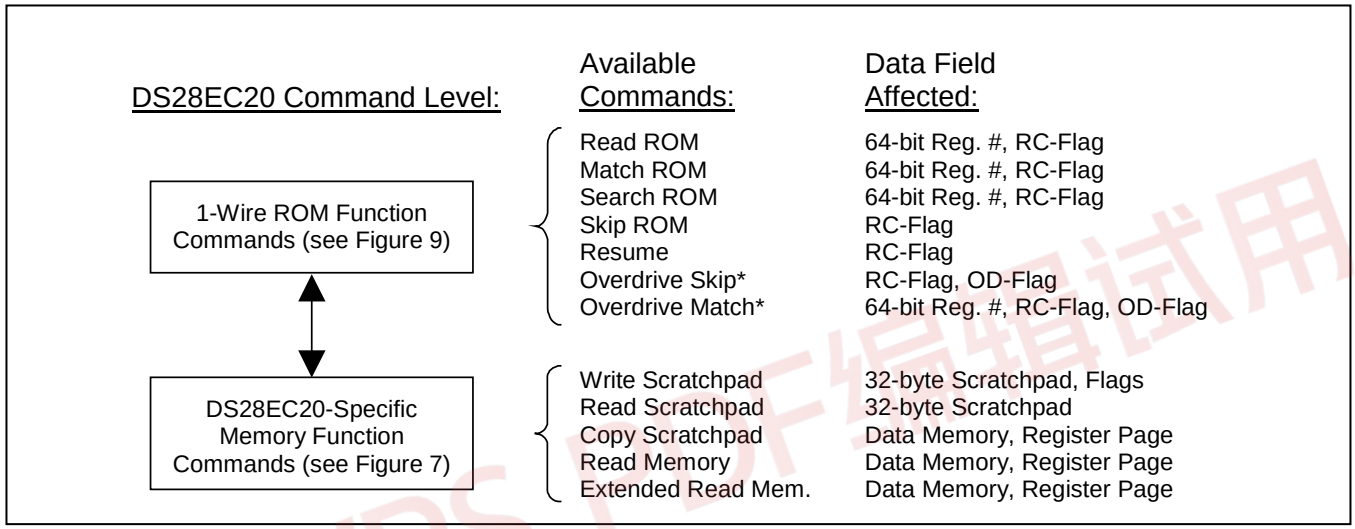
Figure 1. Block Diagram



OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS28EC20. The DS28EC20 has four main data components: 1) 64-bit registration number, 2) 32-byte scratchpad, 3) eighty 32-byte pages of EEPROM, and 4) special function registers. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the seven ROM (network) function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, 5) Resume, 6) Overdrive Skip ROM, or 7) Overdrive Match ROM. Upon completion of an Overdrive ROM command byte executed at standard speed, the device enters Overdrive mode where all subsequent communication occurs at a higher speed. For operation at overdrive speed, the DS28EC20 requires V_{PUP} to be between 4V and 5.25V. The protocol required for these ROM function commands is described in Figure 9. After a ROM function command is successfully executed, the memory functions become accessible and the master may provide any one of the five memory function commands. The protocol for these commands is described in Figure 7. All data is read and written least significant bit first.

Figure 2. Hierarchical Structure for 1-Wire Protocol



* For operation at overdrive speed, the DS28EC20 requires V_{PUP} to be between 4V and 5.25V.

64-BIT ROM

Each DS28EC20 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a cyclic redundancy check (CRC) of the first 56 bits. See Figure 3 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 1-Wire CRC is available in *Application Note 27*: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton® Products* (**www.maximintegrated.com/AN27**).

The shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, the serial number is entered. After the last bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of the CRC returns the shift register to all 0s.

Figure 3. 64-Bit ROM

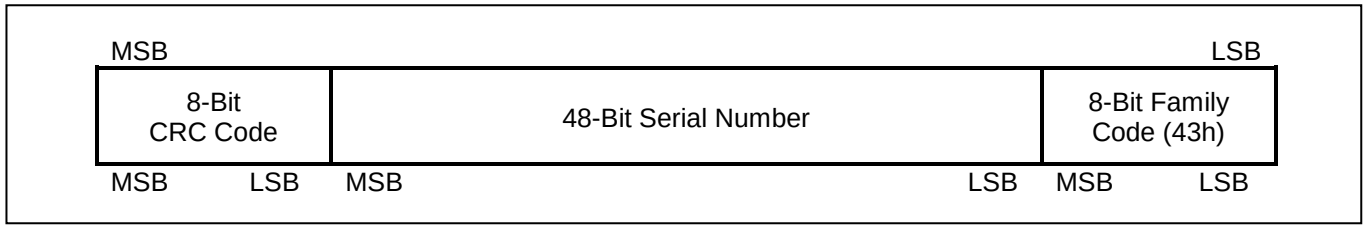


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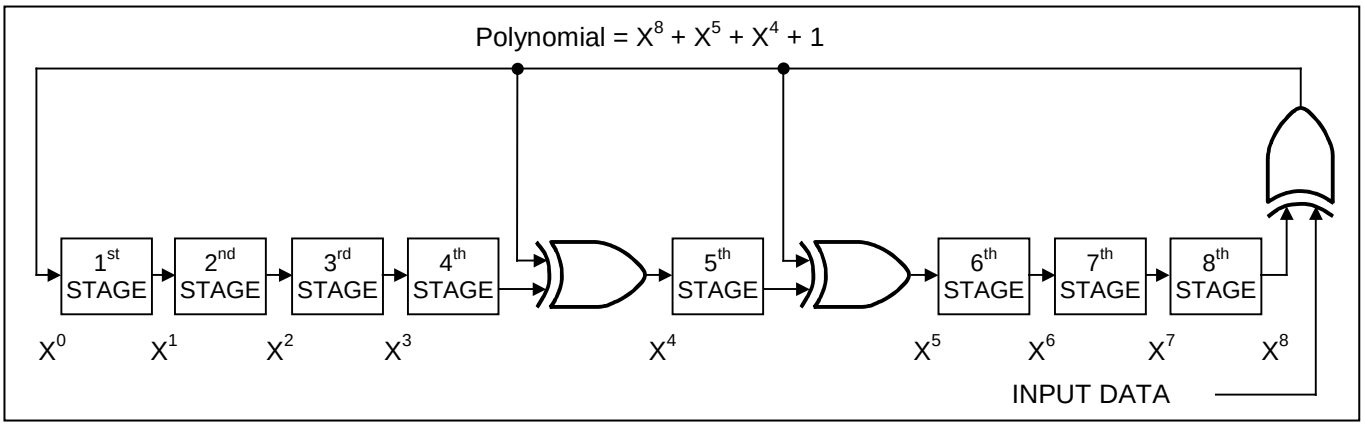
Figure 4. 1-Wire CRC Generator



MEMORY

Data memory and special function registers are located in a linear address space, as shown in Figure 5. The data memory and the registers have unrestricted read access. The data memory consists of 80 pages of 32 bytes each. Eight adjacent pages form one 2Kb block. Each block can be individually set to open (default), write protected, or EPROM mode by setting the associated protection byte in the register page, which starts at address 0A00h. Besides the 10 block protection control bytes (one for each 2Kb data memory block) the register page contains 20 bytes of user EEPROM plus a memory block lock byte and a register page lock byte. Starting at address 0A20h, the DS28EC20 has a read-only memory page that stores a factory byte and a 2-byte field reserved for a factory-administered service to program manufacturer identification. All other bytes of that page are reserved. The manufacturer ID can be a customer-supplied identification code that assists the application software in identifying the product the DS28EC20 is associated with. Contact the factory to set up and register a custom manufacturer ID. In addition to the EEPROM, the device has a 32-byte volatile scratchpad. Writes to the EEPROM array are a two-step process. First, data is written to the scratchpad, and then copied into the main array. The user can verify the data in the scratchpad prior to copying.

The protection control registers, along with the Memory Block Lock byte, determine whether write protection, EPROM mode, or copy protection is enabled for each of the 10 data memory blocks. A value of 55h sets write protection for the associated memory block. A value of Aah sets EPROM mode. The Memory Block Lock byte, if programmed to either 55h or Aah, sets copy protection for all write-protected data memory blocks. Blocks in EPROM mode are not affected. Programming the Register Page Lock byte to either 55h or Aah copy protects the entire register page. The protection control registers and the Lock bytes write protect themselves if set to 55h or Aah. Any other setting leaves them open for unrestricted write access. See the *Copy Protection* section for explanation of copy protect vs. write protect.

Write Protection: Write protection prevents data from being changed, but does not block the copy-scratchpad function; this allows the memory to be reprogrammed with the same data. In EEPROM devices digital information is stored as electrical charge (electrons) on floating gates. Quantum mechanical effects allow electrons to be transported in large numbers to and from the floating gate for programming and erasing memory cells. Electrons leave the floating gate at a temperature-dependent rate. The higher the temperature, the faster is the rate at which electrons escape. This rate is expressed as *Data Retention* in the EC table. Reprogramming the memory returns the charge to the original value for a full data retention time. This is particularly useful in applications where data retention is a concern, e.g., at high temperatures.

Copy Protection: Copy protection blocks the execution of the copy-scratchpad function. This feature achieves a higher level of security, and should only be used after all write-protected locations and their associated protection control bytes are set to their final values. Copy protection does not prevent copying data from one device to another.

Figure 5. Memory Map

ADDRESS RANGE	TYPE	DESCRIPTION	PROTECTION CODES (NOTES)
0000h to 00FFh	R/(W)	Data Memory Pages 0 to 7 (Block 0)	(Protection controlled by address 0A00h)
0100h to 01FFh	R/(W)	Data Memory Pages 8 to 15 (Block 1)	(Protection controlled by address 0A01h)
0200h to 02FFh	R/(W)	Data Memory Pages 16 to 23 (Block 2)	(Protection controlled by address 0A02h)
0300h to 03FFh	R/(W)	Data Memory Pages 24 to 31 (Block 3)	(Protection controlled by address 0A03h)
0400h to 04FFh	R/(W)	Data Memory Pages 32 to 39 (Block 4)	(Protection controlled by address 0A04h)
0500h to 05FFh	R/(W)	Data Memory Pages 40 to 47 (Block 5)	(Protection controlled by address 0A05h)
0600h to 06FFh	R/(W)	Data Memory Pages 48 to 55 (Block 6)	(Protection controlled by address 0A06h)
0700h to 07FFh	R/(W)	Data Memory Pages 56 to 63 (Block 7)	(Protection controlled by address 0A07h)
0800h to 08FFh	R/(W)	Data Memory Pages 64 to 71 (Block 8)	(Protection controlled by address 0A08h)
0900h to 09FFh	R/(W)	Data Memory Pages 72 to 79 (Block 9)	(Protection controlled by address 0A09h)
0A00h* to 0A09h*	R/(W)	Protection Control Blocks 0 to 9	55h: Write protected; Aah: EPROM mode. Address 0A00h is associated with Block 0, address 0A01h with Block 1, etc.
0A0Ah to 0A1Dh	R/(W)	User EEPROM	(Protection controlled by address 0A1Fh)
0A1Eh*	R/(W)	Memory Block Lock	(See text)
0A1Fh*	R/(W)	Register Page Lock	(See text)
0A20h	R	Factory Byte	(55h ➔ no valid manufacturer ID, Aah ➔ 0A23h to 0A24h are a valid Manufacturer ID)
0A21h to 0A22h	R	Factory Trim Bytes	(Unspecified value)
0A23h to 0A24h	R	Manufacturer ID	Validity depends on factory byte
0A25h to 0A3Fh	R	Reserved	(Unspecified value)

** Once programmed to Aah or 55h this address becomes read-only. All other codes can be stored but neither write-protect the address nor activate any function.*

ADDRESS REGISTERS AND TRANSFER STATUS

The DS28EC20 employs three address registers: TA1, TA2, and E/S (Figure 6). Registers TA1 and TA2 must be loaded with the target address to which the data is written or from which data is read. Register E/S is a read-only transfer status register used to verify data integrity with write commands. E/S bits E[4:0] are loaded with the incoming T[4:0] on a Write Scratchpad command and increment on each subsequent data byte. This is, in effect, a byte-ending offset counter within the 32-byte scratchpad. Bit 5 of the E/S register, called PF, is set if the number of data bits sent by the master is not an integer multiple of 8 or if the data in the scratchpad is not valid due to a loss of power. A valid write to the scratchpad clears the PF bit. Bit 6 has no function; it always reads 0. The highest valued bit of the E/S register, called authorization accepted (AA), is valid only if the PF flag reads 0. If PF is 0 and AA is 1, the data stored in the scratchpad has already been copied to the target memory address. Writing data to the scratchpad clears this flag.

Figure 6. Address Registers

Bit #	7	6	5	4	3	2	1	0
Target Address (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
Target Address (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
Ending Address with Data Status (E/S) (Read Only)	AA	0	PF	E4	E3	E2	E1	E0

WRITING WITH VERIFICATION

To write data to the DS28EC20, the scratchpad must be used as intermediate storage. First, the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. Under certain conditions (see the *Write Scratchpad Command* section) the master receives an inverted CRC16 of the command, address (actual address sent), and data at the end of the Write Scratchpad command sequence. Knowing this CRC value, the master can compare it to the value it has calculated itself to decide if the communication was successful and precede to the Copy Scratchpad command. If the master could not receive the CRC16, it should send the Read Scratchpad command to verify data integrity. As a preamble to the scratchpad data, the DS28EC20 repeats the target address TA1 and TA2 and sends the contents of the E/S register. If the PF flag is set, data did not arrive correctly in the scratchpad or there was a loss of power since data was last written to the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag together with a cleared PF flag indicates that the device did not recognize the Write command. If everything went correctly, both flags are cleared and the ending offset indicates the address of the last byte written to the scratchpad. Now the master can continue reading and verifying every data byte. After the master has verified the data, it can send the Copy Scratchpad command, for example. This command must be followed exactly by the data of the three address registers TA1, TA2, and E/S. The master should obtain the contents of these registers by reading the scratchpad. As soon as the DS28EC20 has received these bytes correctly, it starts copying the scratchpad data to the requested location, provided that the target memory is not copy protected, the PF flag is cleared, and there was no Read Memory or Extended Read Memory command issued between Write Scratchpad and Copy Scratchpad.

MEMORY FUNCTION COMMANDS

The *Memory Function Flowchart* (Figure 7) describes the protocols necessary for accessing the memory of the DS28EC20. The target address registers TA1 and TA2 are used for both read and write. To prevent accidental changes to the data memory or control registers the device employs a BS-flag indicating a “bad sequence”. The communication between master and DS28EC20 takes place either at standard speed (default, OD = 0) or at overdrive speed (OD = 1). If not explicitly set into the Overdrive mode, the DS28EC20 assumes standard speed. For operation at overdrive speed, the DS28EC20 requires V_{PUP} to be between 4V and 5.25V.

WRITE SCRATCHPAD COMMAND [0Fh]

The Write Scratchpad command applies to the data memory and the writable addresses in the register page. After issuing the Write Scratchpad command, the master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data is written to the scratchpad starting at the byte offset of T[4:0]. The E/S bits E[4:0] are loaded with the starting byte offset, and increment with each subsequent byte. Effectively, E[4:0] is the byte offset of the last full byte written to the scratchpad. Only full bytes are accepted. If the last byte is incomplete its content is ignored and the partial byte flag PF is set. The PF flag is also set if the master ends the command before a complete target address is transmitted. The PF and BS flags are both cleared when a complete target address is received.

When executing the Write Scratchpad command, the CRC generator inside the DS28EC20 (Figure 13) calculates a 16-bit CRC of the entire data stream, starting at the command code and ending at the last data byte as sent by the master. This CRC is generated using the CRC16 polynomial ($X^{16} + X^{15} + X^2 + 1$) by first clearing the CRC generator and then shifting in the command code (0Fh) of the Write Scratchpad command, the target addresses TA1 and TA2 as supplied by the master, and all the data bytes. The master can end the Write Scratchpad command at any time. However, if the end of the scratchpad is reached (E[4:0] = 11111b), the master can send 16 read-time slots to receive the CRC generated by the DS28EC20.

If a Write Scratchpad is attempted to a write-protected location, the scratchpad is loaded with the data already in memory, rather than the data transmitted. Similarly, if the target address page is in EPROM mode, the scratchpad is loaded with the bitwise logical AND of the transmitted data and the data already in memory.

The DS28EC20’s memory address range is 0000h to 0A3Fh. If the bus master sends a target address higher than this, the DS28EC20’s internal circuitry sets the four most significant address bits to zero as they are shifted into the internal address register. The Read Scratchpad command reveals the modified target address. The master identifies such address modifications by comparing the target address read back to the target address transmitted. If the master does not read the scratchpad, a subsequent Copy Scratchpad command does not work since the most significant bits of the target address the master sends do not match the value the DS28EC20 expects.

READ SCRATCHPAD COMMAND [Aah]

The Read Scratchpad command allows verifying the target address and the integrity of the scratchpad data. After issuing the command code, the master begins reading. The first two bytes are the target address. The next byte is the Ending Offset/Data Status byte (E/S) followed by the scratchpad data beginning at the byte offset (T[4:0]). The scratchpad data can be different from what the master originally sent. This is of particular importance if the target address is within the register page or a page in either Write Protection or EPROM modes. See the *Write Scratchpad Command* section for details. The master should read through the end of the scratchpad, after which it receives an inverted CRC16, based on data as it was sent by the DS28EC20. If the master continues reading after the CRC, all data are logic 1s.

Figure 7-1. Memory Function Flowchart

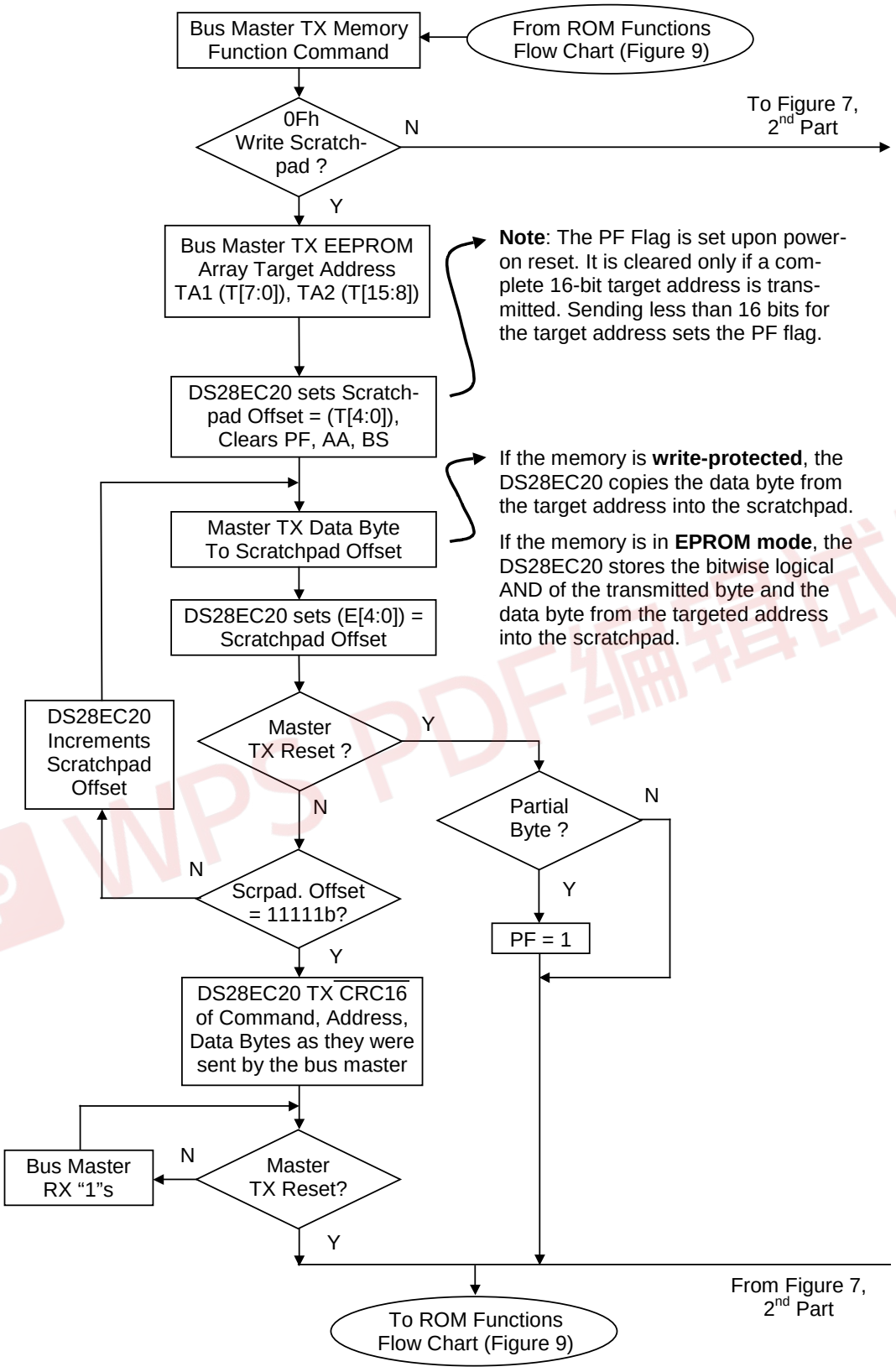


Figure 7-2. Memory Function Flowchart (continued)

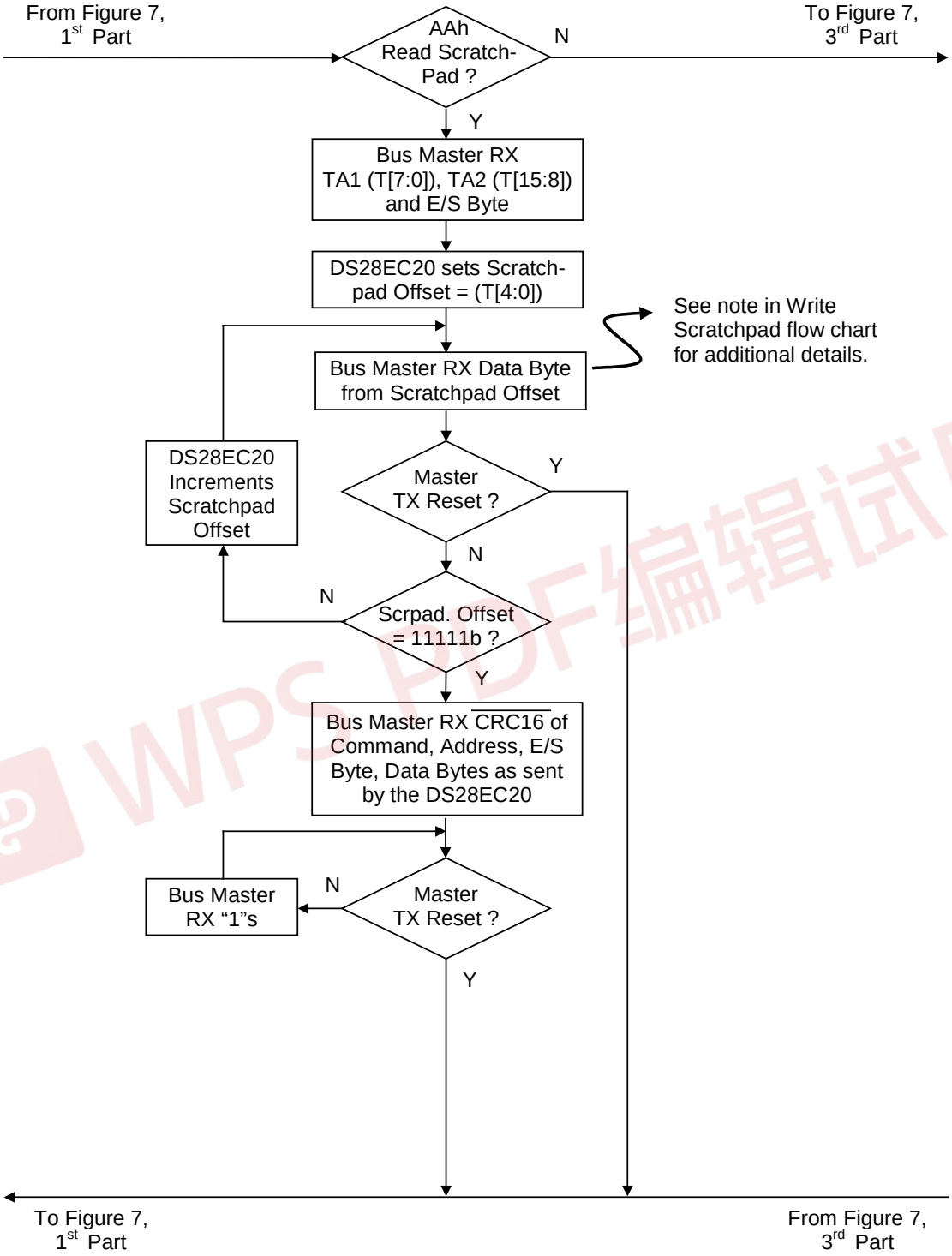


Figure 7-3. Memory Function Flowchart (continued)

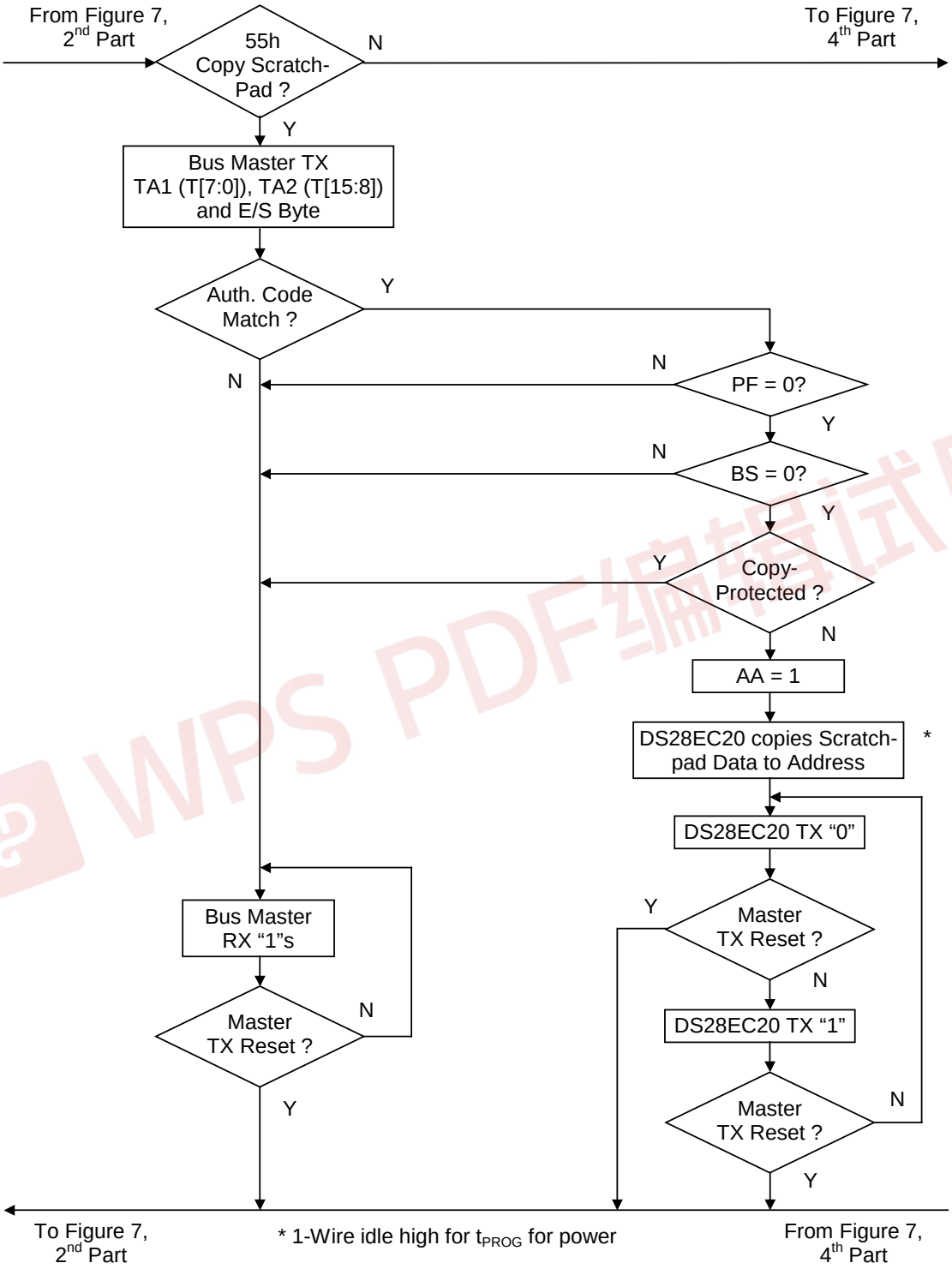
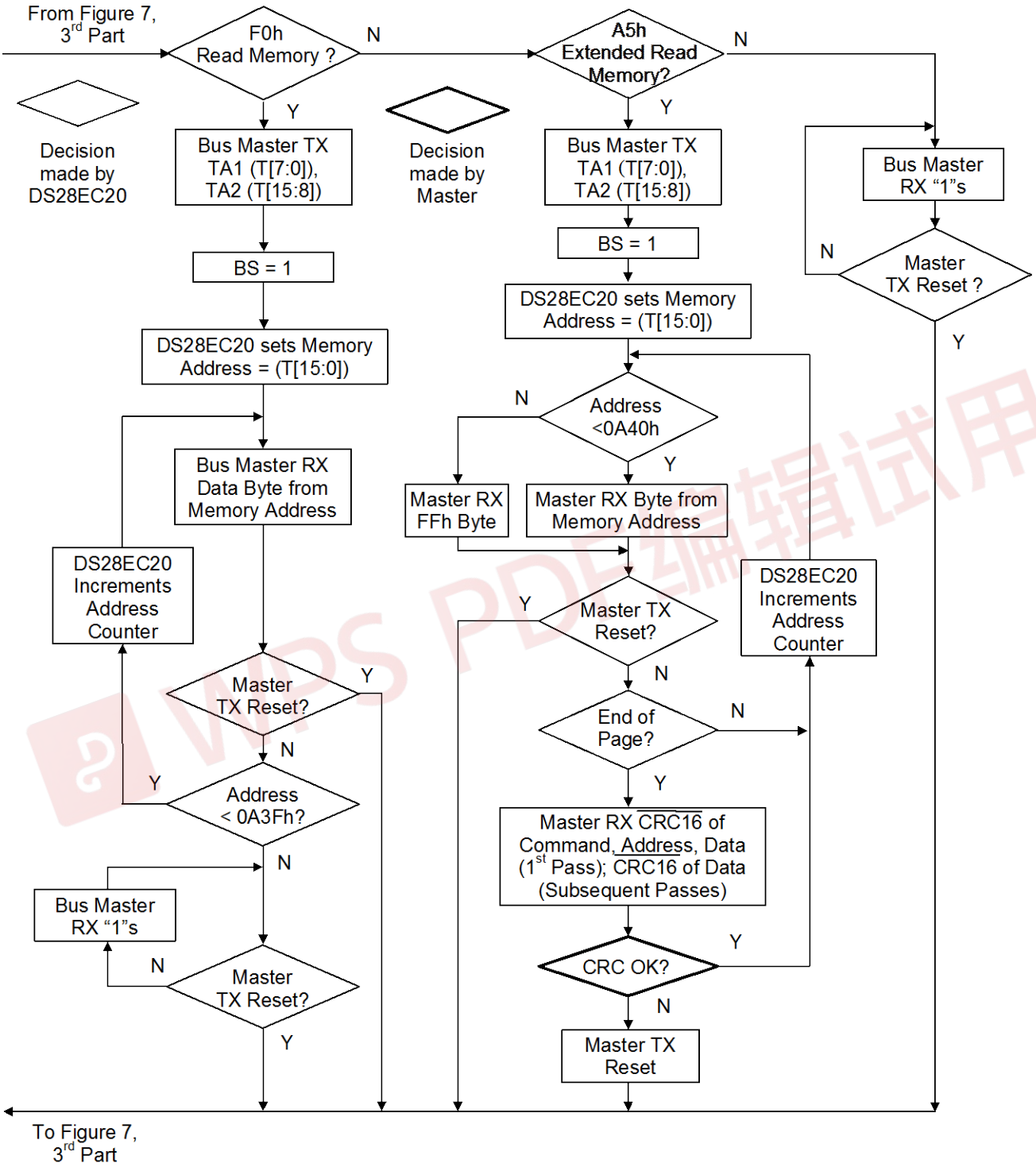


Figure 7-4. Memory Function Flowchart (continued)



COPY SCRATCHPAD [55h]

The Copy Scratchpad command is used to copy data from the scratchpad to the data memory and the writable sections of the register page. After issuing the Copy Scratchpad command, the master must provide a 3-byte authorization pattern, which should have been obtained by an immediately preceding Read Scratchpad command. This 3-byte pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the target address is valid, the PF and BS flag are not set, and the target memory is not copy protected, the AA flag is set and the copy begins. The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset is copied to memory, starting at the target address. Anywhere from 1 to 32 bytes can be copied with this command. The duration of the device's internal data transfer is t_{PROG} during which the 1-Wire bus must be idle or actively pulled high. Active pullup is optional for this device. A pattern of alternating 0s and 1s are transmitted after the data has been copied until the master issues a reset pulse. If the PF flag or BS flag is set or the target memory is copy protected, the copy does not begin and the AA flag is not set. The BS flag ensures that Copy Scratchpad is not executed (blocked) if there was a Read Memory or Extended Read Memory between Write Scratchpad and Copy Scratchpad.

READ MEMORY [F0h]

The Read Memory command is the general function to read from the DS28EC20. After issuing the command, the master must provide a 2-byte target address, which should be in the range of 0000h to 0A3Fh. If the target address is higher than 0A3Fh, the DS28EC20 changes the upper four address bits to 0. After the address is transmitted, the master reads data starting at the (modified) target address and can continue until address 0A3Fh. If the master continues reading, the result is FFh. The Read Memory command sequence can be ended at any point by issuing a reset pulse. Note that this command sets the BS flag. This requires any scratchpad data to be rewritten before it can be used in a Copy Scratchpad sequence.

EXTENDED READ MEMORY [A5h]

This command works essentially the same way as Read Memory, except for the 16-bit CRC that the DS28EC20 generates and transmits following the last data byte of a memory page. The CRC generated by this command uses the same polynomial as the Write Scratchpad command. After issuing the command, the master must provide a 2-byte target address, which should be in the range of 0000h to 0A3Fh. If the target address is higher than 0A3Fh, the DS28EC20 changes the upper four address bits to 0. After the address is transmitted, the master reads data starting at the (modified) target address and continuing until the end of a 32-byte page is reached. At that point the bus master receives an inverted 16-bit CRC. If the master continues reading it receives data starting at the beginning of the next page, followed again by the inverted CRC for that page. Reading beyond the end of the memory is permissible, but the result is FFh. The Extended Read Memory command sequence can be ended at any point by issuing a reset pulse. Note that this command sets the BS flag. This requires any scratchpad data to be rewritten before it can be used in a Copy Scratchpad sequence.

1-Wire BUS SYSTEM

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances the DS28EC20 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots, which are initiated on the falling edge of sync pulses from the bus master.

HARDWARE CONFIGURATION

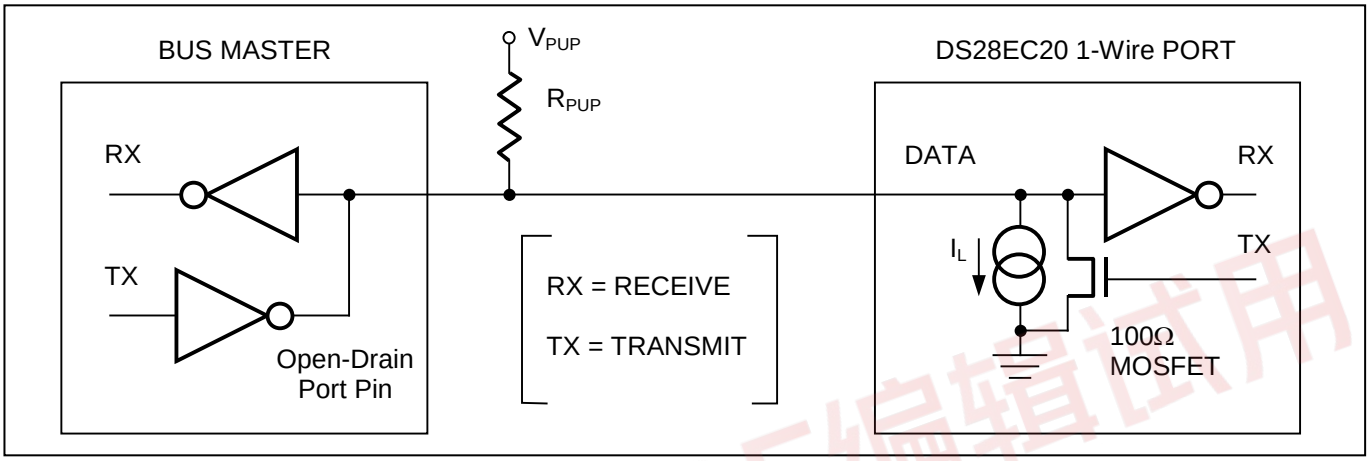
The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or tri-state outputs. The 1-Wire port of the DS28EC20 is open drain with an internal circuit equivalent to that shown in Figure 8.

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The DS28EC20 supports both a standard and overdrive communication speed of 15.4kbps (max) and 90kbps (max), respectively. For operation at overdrive

speed, the DS28EC20 requires V_{PUP} to be between 4V and 5.25V. Note that legacy 1-Wire products support a standard communication speed of 16.3kbps and overdrive of 142kbps. The slightly reduced rates for the DS28EC20 are a result of additional recovery times, which in turn were driven by a 1-Wire physical interface enhancement to improve noise immunity. The value of the pullup resistor primarily depends on the network size and load conditions. The DS28EC20 requires a pullup resistor of 2.2kΩ (max) at any speed.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs (overdrive speed) or more than 120µs (standard speed), one or more devices on the bus can be reset.

Figure 8. Hardware Configuration



TRANSACTION SEQUENCE

The protocol for accessing the DS28EC20 through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS28EC20 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

1-Wire ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the seven ROM function commands that the DS28EC20 supports. All ROM function commands are 8 bits long. See Figure 9 for list of these commands.

READ ROM [33h]

This command allows the bus master to read the DS28EC20's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

MATCH ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS28EC20 on a multidrop bus. Only the DS28EC20 that exactly matches the 64-bit ROM sequence responds to the following memory function command. All other slaves wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

SEARCH ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their registration numbers. By taking advantage of the bus's wired-AND property, the master can use a process of elimination to identify the registration numbers of all slave devices. For each bit of the registration number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its registration number bit. On the second slot, each slave device participating in the search outputs the complemented value of its registration number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the ROM code tree. After one complete pass, the bus master knows the registration number of a single device. Additional passes identify the registration numbers of the remaining devices. Refer to *Application Note 187: 1-Wire Search Algorithm* (**www.maximintegrated.com/AN187**) for a detailed discussion, including an example.

SKIP ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and, for example, a Read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

RESUME [A5h]

To maximize the data throughput in a multidrop environment, the Resume function is available. This function checks the status of the RC bit and, if it is set, directly transfers control to the memory functions, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM, or Overdrive Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command function. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command function.

OVERDRIVE SKIP ROM [3Ch]*

On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command, the Overdrive Skip ROM sets the DS28EC20 in the Overdrive mode (OD = 1). All communication following this command must occur at overdrive speed until a reset pulse of minimum 480µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all overdrive-supporting devices into Overdrive mode. To subsequently address a specific overdrive-supporting device, a reset pulse at overdrive speed must be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave supporting overdrive is present on the bus and the Overdrive Skip ROM command is followed by a Read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

OVERDRIVE MATCH ROM [69h]*

The Overdrive Match ROM command followed by a 64-bit ROM sequence transmitted at overdrive speed allows the bus master to address a specific DS28EC20 on a multidrop bus and to simultaneously set it in Overdrive mode. Only the DS28EC20 that exactly matches the 64-bit ROM sequence responds to the subsequent memory function command. Slaves already in Overdrive mode from a previous Overdrive Skip or successful Overdrive Match command remain in Overdrive mode. All overdrive-capable slaves return to standard speed at the next Reset Pulse of minimum 480µs duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

* For operation at overdrive speed, the DS28EC20 requires V_{PUP} to be between 4V and 5.25V.

Figure 9-1. ROM Functions Flowchart

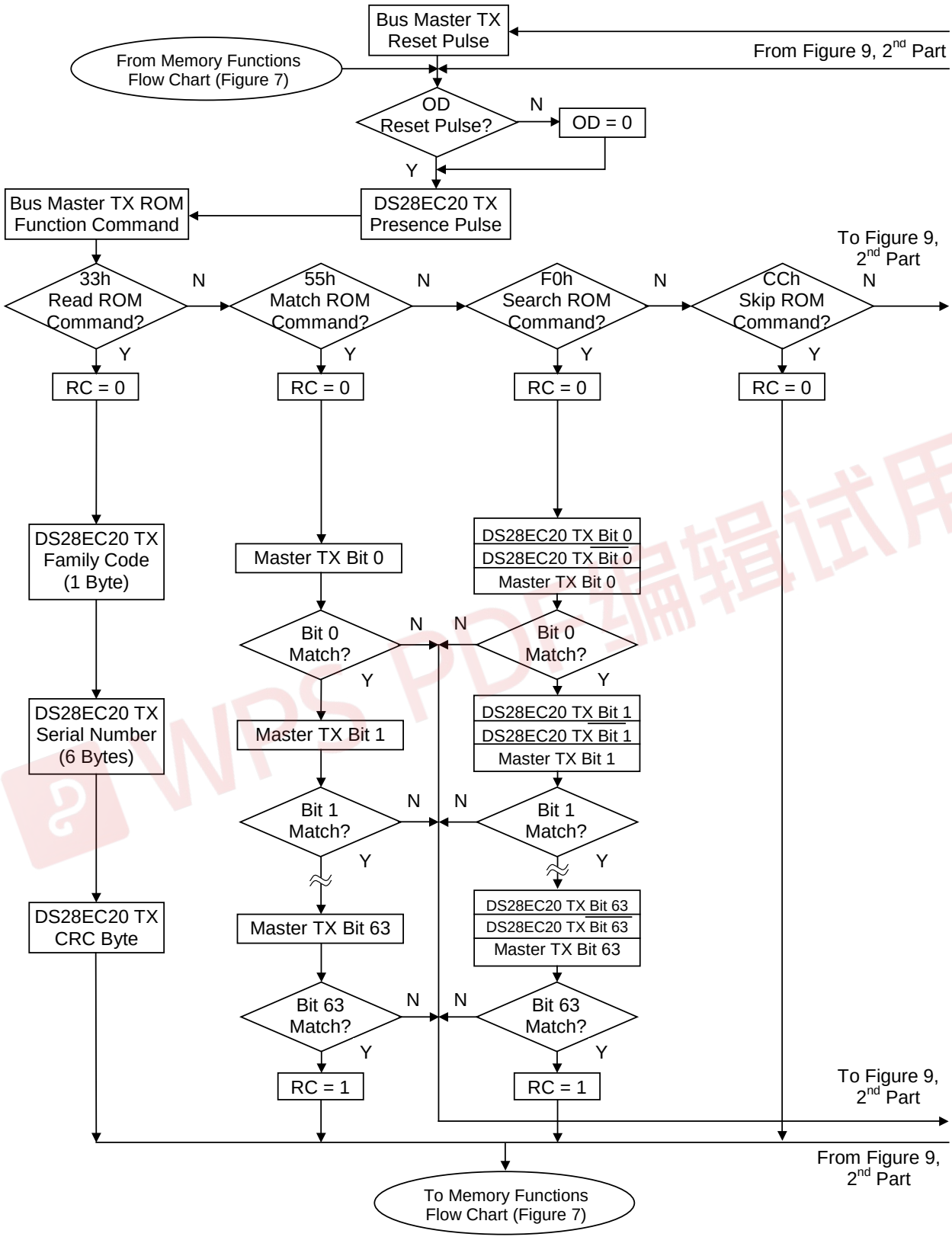
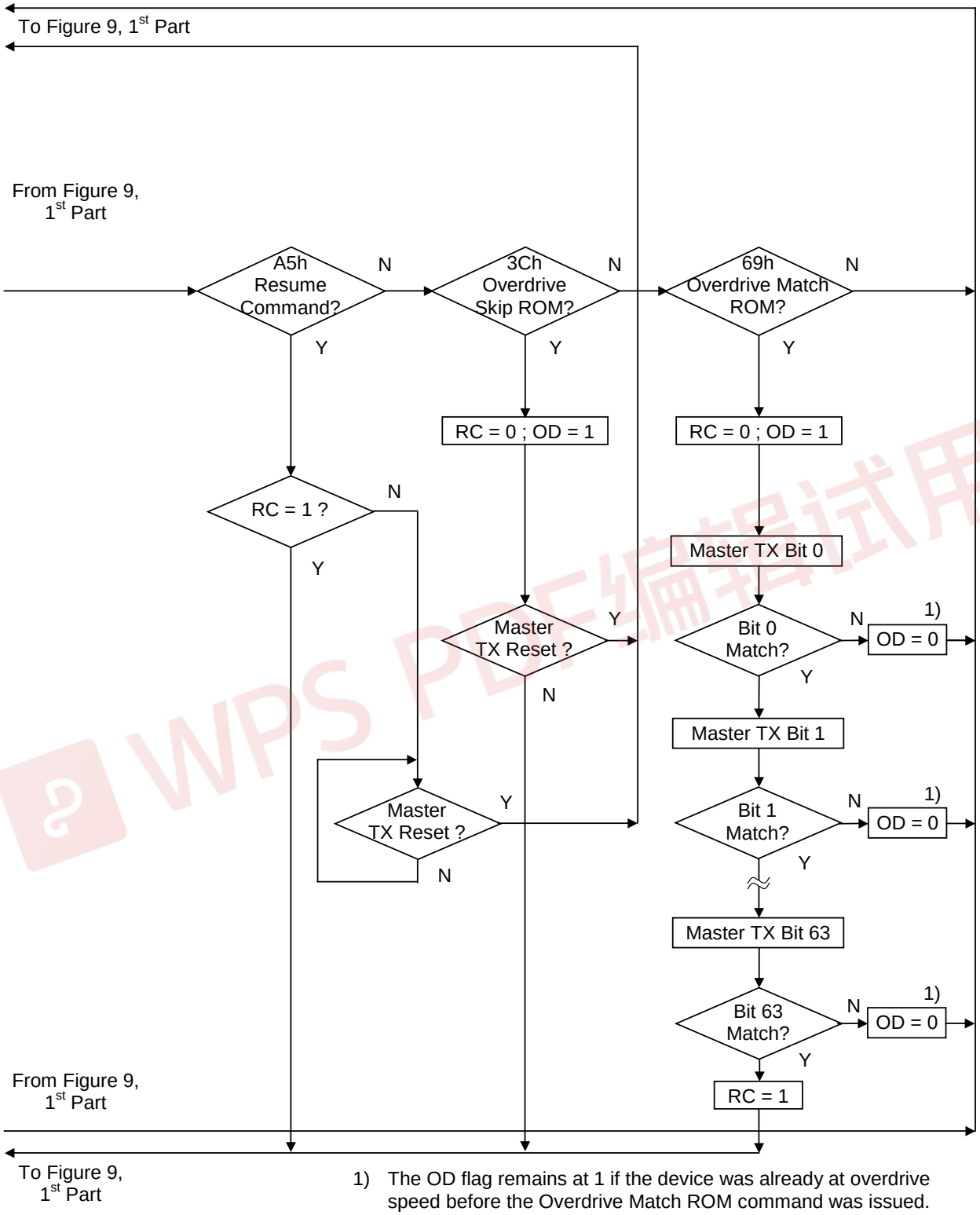


Figure 9-2. ROM Functions Flowchart (continued)



1) The OD flag remains at 1 if the device was already at overdrive speed before the Overdrive Match ROM command was issued.

NOTE: For operation at overdrive speed, the DS28EC20 requires V_{PUP} to be between 4V and 5.25V.

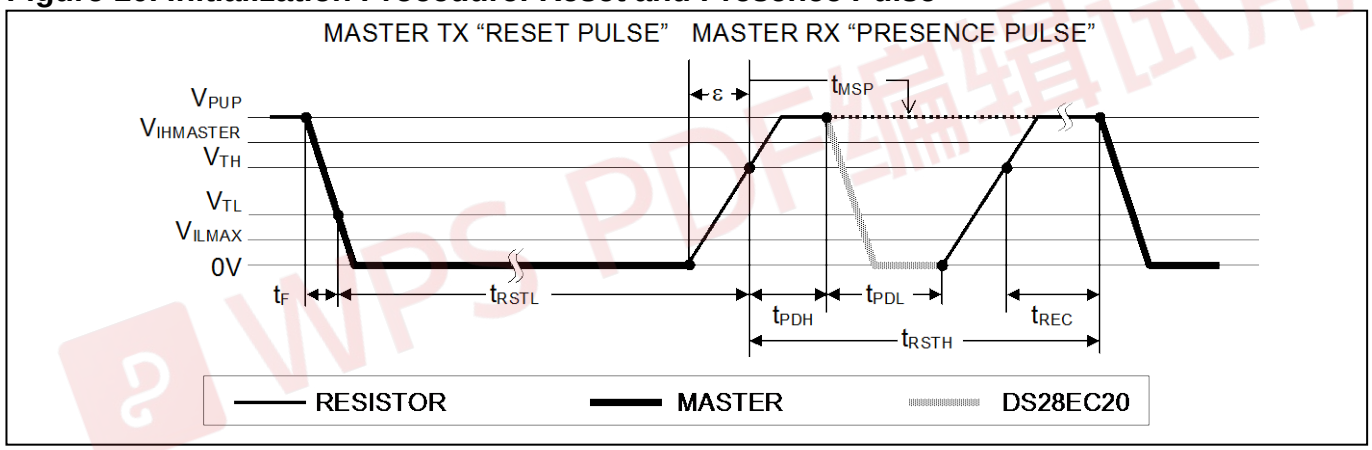
1-Wire SIGNALING

The DS28EC20 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus master initiates all falling edges. The DS28EC20 can communicate at two different speeds: standard speed and overdrive speed. If not explicitly set into the Overdrive mode, the DS28EC20 communicates at standard speed. While in Overdrive mode the fast timing applies to all waveforms. For operation at overdrive speed, the DS28EC20 requires V_{PUP} to be between 4V and 5.25V.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 10 as ε, and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS28EC20 when determining a logical level, not triggering any events.

Figure 10 shows the initialization sequence required to begin any communication with the DS28EC20. A reset pulse followed by a presence pulse indicates that the DS28EC20 is ready to receive data, given the correct ROM and memory function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for t_{RSTL} + t_F to compensate for the edge. A t_{RSTL} duration of 480µs or longer exits the Overdrive mode, returning the device to standard speed. If the DS28EC20 is in Overdrive mode and t_{RSTL} is no longer than 80µs, the device remains in Overdrive mode. If the device is in Overdrive mode and t_{RSTL} is between 80µs and 480µs, the device resets, but the communication speed is undetermined.

Figure 10. Initialization Procedure: Reset and Presence Pulse



After the bus master has released the line it goes into Receive mode. Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor, or in case of a DS2482-x00 or DS2480B driver, by active circuitry. When the threshold V_{TH} is crossed, the DS28EC20 waits for t_{PDH} and then transmits a presence pulse by pulling the line low for t_{PDL}. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

The t_{RSTH} window must be at least the sum of t_{PDHMAX}, t_{PDLMAX}, and t_{RECMIN}. Immediately after t_{RSTH} is expired, the DS28EC20 is ready for data communication. In a mixed population network, t_{RSTH} should be extended to minimum 480µs at standard speed and 48µs at overdrive speed to accommodate other 1-Wire devices.

Read-/Write-Time Slots

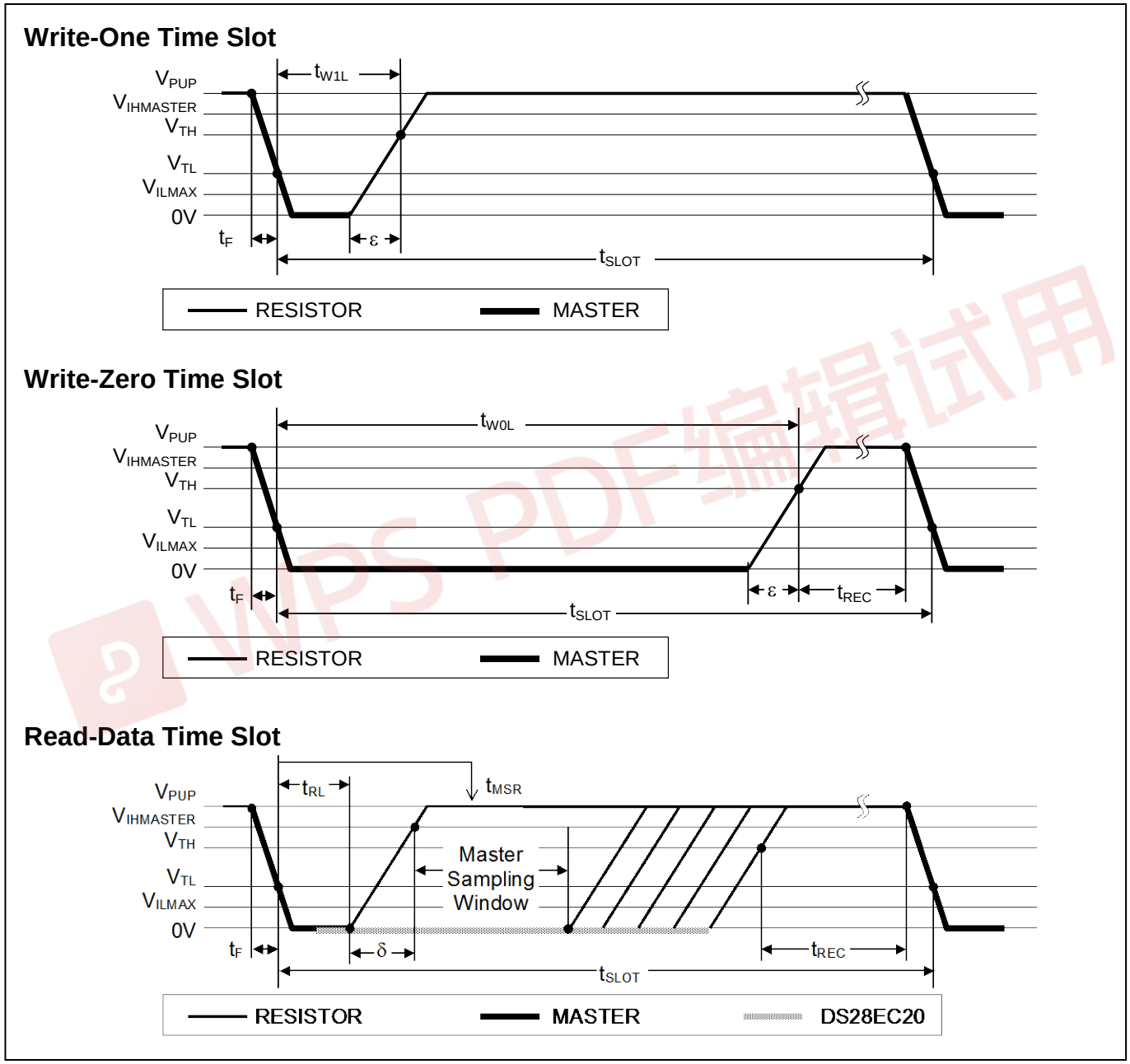
Data communication with the DS28EC20 takes place in time slots, which carry a single bit each. Write-time slots transport data from bus master to slave. Read-time slots transfer data from slave to master. Figure 11 illustrates the definitions of the write– and read-time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS28EC20 starts its internal timing generator that determines when the data line is sampled during a write-time slot and how long data is valid during a read-time slot.

Master-to-Slave

For a write-one time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a write-zero time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS28EC20 needs a recovery time t_{REC} before it is ready for the next time slot.

Figure 11. Read/Write Timing Diagram



Slave-to-Master

A read-data time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS28EC20 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS28EC20 does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of t_{RL} + δ (rise time) on one side and the internal timing generator of the DS28EC20 on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}) in which the master must perform a read from the data line. For the most reliable communication, t_{RL} should be as short as permissible, and the master should read close to but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS28EC20 to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS28EC20 attached to a 1-Wire line. For multidevice configurations, t_{REC} needs to be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time such as the DS2482-x00 or DS2480B 1-Wire line drivers can be used.

IMPROVED NETWORK BEHAVIOR (SWITCHPOINT HYSTERESIS)

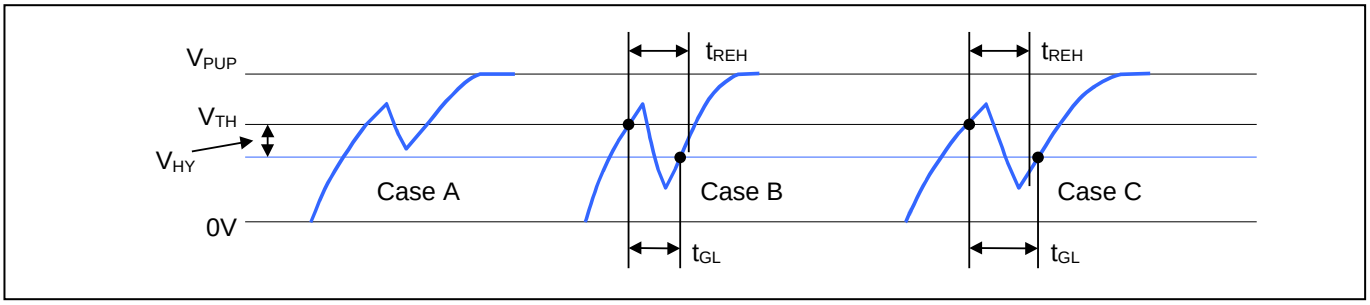
In a 1-Wire environment, line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, consequently, result in a Search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS28EC20 uses a new 1-Wire front-end, which makes it less sensitive to noise.

The 1-Wire front-end of the DS28EC20 differs from traditional slave devices in three characteristics:

1) There is additional low-pass filtering in the circuit that detects the falling edge at the beginning of a time slot. This reduces the sensitivity to high-frequency noise. This additional filtering does not apply at overdrive speed.
2) There is a hysteresis at the low-to-high switching threshold V_{TH}. If a negative glitch crosses V_{TH} but does not go below $V_{TH} – V_{HY}$, it is not recognized (Figure 12, Case A). The hysteresis is effective at any 1-Wire speed.
3) There is a time window specified by the rising edge hold-off time t_{REH} during which glitches are ignored, even if they extend below $V_{TH} – V_{HY}$ threshold (Figure 12, Case B, $t_{GL} < t_{REH}$). Deep voltage droops or glitches that appear late after crossing the V_{TH} threshold and extend beyond the t_{REH} window cannot be filtered out and are taken as the beginning of a new time slot (Figure 12, Case C, $t_{GL} \geq t_{REH}$).

Devices that have the parameters V_{HY} and t_{REH} specified in their electrical characteristics use the improved 1-Wire front-end.

Figure 12. Noise Suppression Scheme



CRC GENERATION

The DS28EC20 uses two different types of CRCs. One CRC is an 8-bit type and is stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS28EC20 to determine if the ROM data has been received error-free. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (noninverted) form. It is computed at the factory and programmed into the ROM.

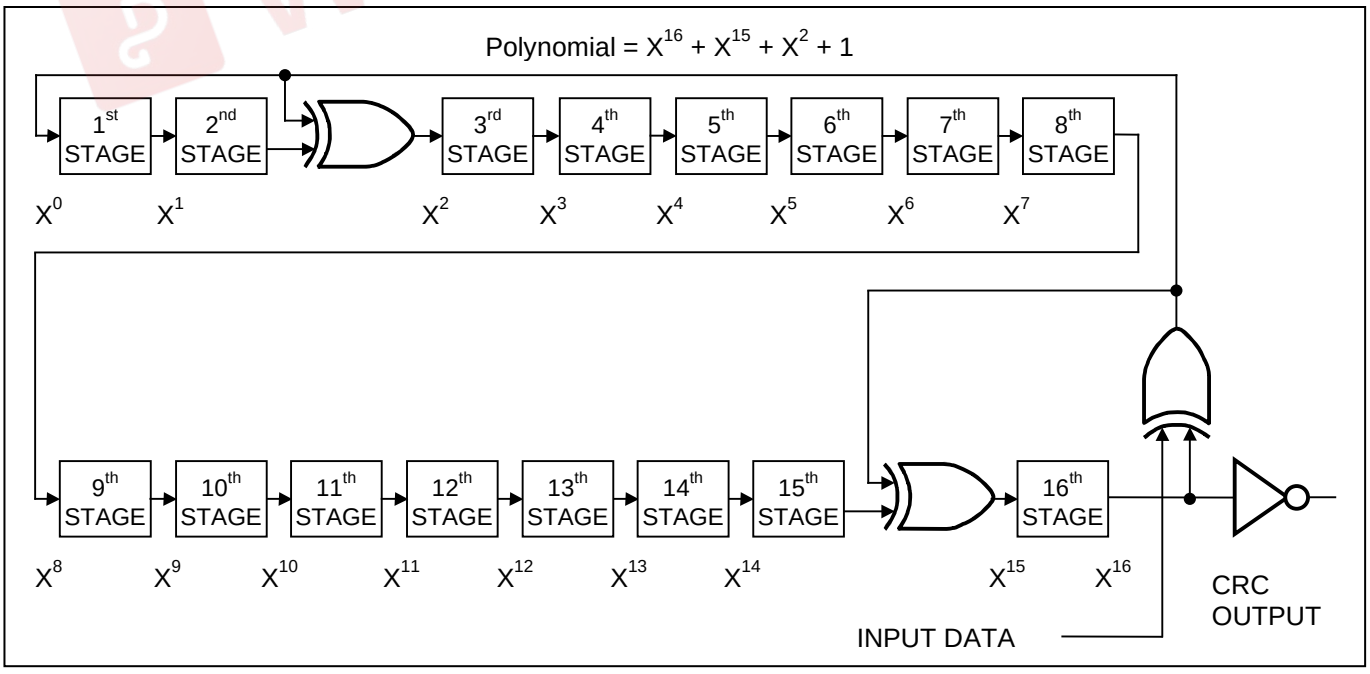
The other CRC is a 16-bit type, generated according to the standardized CRC16 polynomial function $X^{16} + X^{15} + X^2 + 1$. This CRC is used for fast verification of a data transfer when writing to or reading from the scratchpad and with the Extended Read Memory command. In contrast to the 8-bit CRC, the 16-bit CRC is always communicated in the inverted form. A CRC generator inside the DS28EC20 (Figure 13) calculates a new 16-bit CRC, as shown in the command flowchart (Figure 7). The bus master compares the CRC value read from the device to the one it calculates from the data, and decides whether to continue with an operation or to reread the portion of the data with the CRC error.

With the Write Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, and all the data bytes as they were sent by the bus master. The DS28EC20 transmits this CRC only if the data bytes written to the scratchpad include scratchpad ending offset 11111b. The data can start at any location within the scratchpad.

With the Read Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, the E/S byte, and the scratchpad data as they were sent by the DS28EC20 starting at the target address. The DS28EC20 transmits this CRC only if the reading continues through the end of the scratchpad, regardless of the actual ending offset.

With the initial pass through the extended read memory flow, the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the two address bytes and the data bytes. Subsequent passes through the extended read memory flow generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the data bytes. For more information on generating CRC values refer to *Application Note 27*: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton Products* (**www.maximintegrated.com/AN27**).

Figure 13. CRC16 Hardware Description and Polynomial



COMMAND-SPECIFIC 1-Wire COMMUNICATION PROTOCOL—LEGEND

SYMBOL	DESCRIPTION
RST	1-Wire reset pulse generated by master.
PD	1-Wire presence pulse generated by slave.
Select	Command and data to satisfy the ROM function protocol.
WS	Command “Write Scratchpad”.
RS	Command “Read Scratchpad”.
CPS	Command “Copy Scratchpad”.
RM	Command “Read Memory”.
ERM	Command “Extended Read Memory”.
TA	Target address TA1, TA2.
TA-E/S	Target address TA1, TA2 with E/S byte.
<data to EOS>	Transfer of as many bytes as needed to reach the end of the scratchpad for a given target address.
<data to EOM>	Transfer of as many data bytes as are needed to reach the end of the memory.
<data to EOP>	Transfer of as many data bytes as are needed to reach the end of the page for a given target address.
CRC16\	Transfer of an inverted CRC16.
FF loop	Indefinite loop where the master reads FF bytes.
AA loop	Indefinite loop where the master reads AA bytes.
Programming	Data transfer to EEPROM; no activity on the 1-Wire bus permitted during this time.

COMMAND-SPECIFIC 1-Wire COMMUNICATION PROTOCOL—COLOR CODES

Master to Slave	Slave to Master	Programming

WRITE SCRATCHPAD (CANNOT FAIL)

RST	PD	Select	WS	TA	<Data to EOS>	CRC16\	FF Loop

[redacted]

READ SCRATCHPAD

RST	PD	Select	RS	TA-E/S	<Data to EOS>	CRC16\	FF Loop

[redacted]

COPY SCRATCHPAD (SUCCESS)

RST	PD	Select	CPS	TA-E/S	Programming	AA Loop

COPY SCRATCHPAD (BS = 1 OR PF = 1 OR COPY PROTECTED)

RST	PD	Select	CPS	TA-E/S	FF Loop

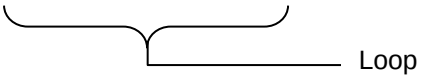
[redacted]

READ MEMORY (CANNOT FAIL)

RST	PD	Select	RM	TA	<Data to EOM>	FF Loop

EXTENDED READ MEMORY (CANNOT FAIL)

RST	PD	Select	ERM	TA	<Data to EOP>	CRC16\	<32 Bytes>	CRC16\



PACKAGE INFORMATION

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 TSOC	D6+1	21-0382	90-0321
3 TO-92 (bulk)	Q3+1	21-0248	—
3 TO-92 (tape and reel)	Q3+4	21-0250	—
6 TDFN	T633+2	21-0137	90-0058

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	071007	Initial release	—
1	091707	TSOC package added; corrected *Electrical Characteristics* table Note 20	1, 4
2	040109	Updated the text and graphics to mark which features are not applicable in the low-voltage environment	1, 3, 7, 11, 17, 18, 20, 21
		Created a second *Electrical Characteristics* table for 3.3V V_{PUP} (±5%), operating temp range 0°C to +70°C, no overdrive	4, 5
3	11/11	Removed information about the registration number being factory lasered into the chip in the *General Description* section, *64-Bit ROM* section, Figure 3, and *CRC Generation* section	1, 7, 24
		Changed 125kbps to 90kbps in the *Features* and *Hardware Configuration* sections	1, 16
		Updated the soldering information and added lead temperature information in the *Absolute Maximum Ratings* section	2
		Updated the *5.0V/3.0V Supply Electrical Characteristics* tables parameters for C_{IO}, I_L, t_{REC}, t_{SLOT}, I_{PROG}, and related notes	2–5
		Replaced the last sentence of the *Read Memory [F0h]* and *Extended Read Memory [A5h]* sections to clarify the command	16
		Added the *Package Information* table	26
4	3/12	Revised the *5.0V Supply Electrical Characteristics* table Notes 1, 4, and 15	3
		Revised the *3.3V Supply Electrical Characteristics* table Notes 3 and 14	5
5	9/13	In the *5.0V Supply Electrical Characteristics* table, changed the $t_{RL(MIN)}$ overdrive speed from 1µs to 0.800µs; changed the $t_{MSR(MAX)}$ overdrive speed from 2µs to 2.27µs	2
6	11/16	Added TDFN package in *Ordering Information*, *Pin Configuration*, *Absolute Maximum Ratings*, and *Package Information* sections	1, 2, 26
7	9/17	Updated voltage ranges	1–3, 7, 11, 17, 18, 20, 21

DS3231

Extremely Accurate I²C-Integrated RTC/TCXO/Crystal

General Description

The DS3231 is a low-cost, extremely accurate I²C real-time clock (RTC) with an integrated temperature-compensated crystal oscillator (TCXO) and crystal. The device incorporates a battery input, and maintains accurate timekeeping when main power to the device is interrupted. The integration of the crystal resonator enhances the long-term accuracy of the device as well as reduces the piece-part count in a manufacturing line. The DS3231 is available in commercial and industrial temperature ranges, and is offered in a 16-pin, 300-mil SO package.

The RTC maintains seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. Two programmable time-of-day alarms and a programmable square-wave output are provided. Address and data are transferred serially through an I²C bidirectional bus.

A precision temperature-compensated voltage reference and comparator circuit monitors the status of V_{CC} to detect power failures, to provide a reset output, and to automatically switch to the backup supply when necessary. Additionally, the $\overline{RST}$ pin is monitored as a pushbutton input for generating a µP reset.

Benefits and Features

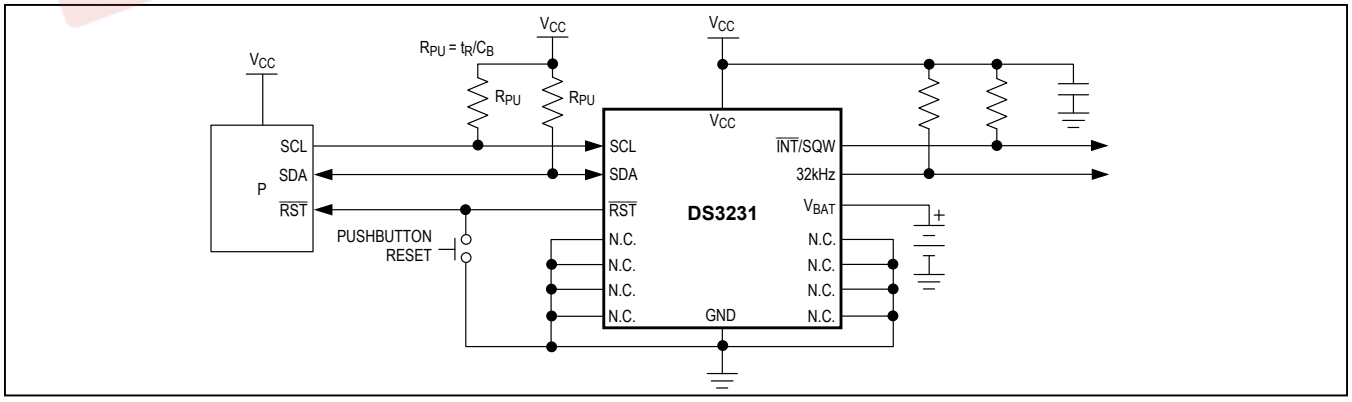
- Highly Accurate RTC Completely Manages All Timekeeping Functions
  - Real-Time Clock Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year, with Leap-Year Compensation Valid Up to 2100
  - Accuracy ±2ppm from 0°C to +40°C
  - Accuracy ±3.5ppm from -40°C to +85°C
  - Digital Temp Sensor Output: ±3°C Accuracy
  - Register for Aging Trim
  - $\overline{RST}$ Output/Pushbutton Reset Debounce Input
  - Two Time-of-Day Alarms
  - Programmable Square-Wave Output Signal
- Simple Serial Interface Connects to Most Microcontrollers
  - Fast (400kHz) I²C Interface
- Battery-Backup Input for Continuous Timekeeping
  - Low Power Operation Extends Battery-Backup Run Time
  - 3.3V Operation
- Operating Temperature Ranges: Commercial (0°C to +70°C) and Industrial (-40°C to +85°C)
- Underwriters Laboratories® (UL) Recognized

Applications

- Servers
- Telematics
- Utility Power Meters
- GPS

Ordering Information and Pin Configuration appear at end of data sheet.

Typical Operating Circuit



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maxim integrated™

Absolute Maximum Ratings

Voltage Range on Any Pin Relative to Ground ....-0.3V to +6.0V
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)73°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1) ....23°C/W
Operating Temperature Range
DS3231S .....0°C to +70°C
DS3231SN..... -40°C to +85°C
Junction Temperature.....+125°C
Storage Temperature Range..... -40°C to +85°C
Lead Temperature (soldering, 10s) .....+260°C
Soldering Temperature (reflow, 2 times max) .....+260°C
(see the *Handling*, *PCB Layout*, *and Assembly* section)

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.3	3.3	5.5	V
	V_{BAT}		2.3	3.0	5.5	V
Logic 1 Input SDA, SCL	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Logic 0 Input SDA, SCL	V_{IL}		-0.3		0.3 x V_{CC}	V

Electrical Characteristics

(V_{CC} = 2.3V to 5.5V, V_{CC} = Active Supply (see Table 1), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Typical values are at V_{CC} = 3.3V, V_{BAT} = 3.0V, and T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Active Supply Current	I_{CCA}	(Notes 4, 5)	V_{CC} = 3.63V			200	µA
			V_{CC} = 5.5V			300	
Standby Supply Current	I_{CCS}	I²C bus inactive, 32kHz output on, SQW output off (Note 5)	V_{CC} = 3.63V			110	µA
			V_{CC} = 5.5V			170	
Temperature Conversion Current	$I_{CCSCONV}$	I²C bus inactive, 32kHz output on, SQW output off	V_{CC} = 3.63V			575	µA
			V_{CC} = 5.5V			650	
Power-Fail Voltage	V_{PF}			2.45	2.575	2.70	V
Logic 0 Output, 32kHz, $\overline{INT}$/SQW, SDA	V_{OL}	I_{OL} = 3mA				0.4	V
Logic 0 Output, $\overline{RST}$	V_{OL}	I_{OL} = 1mA				0.4	V
Output Leakage Current 32kHz, $\overline{INT}$/SQW, SDA	I_{LO}	Output high impedance		-1	0	+1	µA
Input Leakage SCL	I_{LI}			-1		+1	µA
$\overline{RST}$ Pin I/O Leakage	I_{OL}	$\overline{RST}$ high impedance (Note 6)		-200		+10	µA
V_{BAT} Leakage Current (V_{CC} Active)	I_{BATLKG}				25	100	nA

Electrical Characteristics (continued)

(V_{CC} = 2.3V to 5.5V, V_{CC} = Active Supply (see Table 1), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Typical values are at V_{CC} = 3.3V, V_{BAT} = 3.0V, and T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Frequency	f_{OUT}	V_{CC} = 3.3V or V_{BAT} = 3.3V			32.768		kHz
Frequency Stability vs. Temperature (Commercial)	$\Delta f/f_{OUT}$	V_{CC} = 3.3V or V_{BAT} = 3.3V, aging offset = 00h	0°C to +40°C			±2	ppm
			>40°C to +70°C			±3.5	
Frequency Stability vs. Temperature (Industrial)	$\Delta f/f_{OUT}$	V_{CC} = 3.3V or V_{BAT} = 3.3V, aging offset = 00h	-40°C to <0°C			±3.5	ppm
			0°C to +40°C			±2	
			>40°C to +85°C			±3.5	
Frequency Stability vs. Voltage	Δf/V				1		ppm/V
Trim Register Frequency Sensitivity per LSB	Δf/LSB	Specified at:	-40°C		0.7		ppm
			+25°C		0.1		
			+70°C		0.4		
			+85°C		0.8		
Temperature Accuracy	Temp	V_{CC} = 3.3V or V_{BAT} = 3.3V		-3		+3	°C
Crystal Aging	$\Delta f/f_O$	After reflow, not production tested	First year		±1.0		ppm
			0–10 years		±5.0		

Electrical Characteristics

(**V_{CC} = 0V, V_{BAT} = 2.3V to 5.5V**, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Active Battery Current	I_{BATA}	$\overline{EOSC}$ = 0, BBSQW = 0, SCL = 400kHz (Note 5)	V_{BAT} = 3.63V			70	µA
			V_{BAT} = 5.5V			150	
Timekeeping Battery Current	I_{BATT}	$\overline{EOSC}$ = 0, BBSQW = 0, EN32kHz = 1, SCL = SDA = 0V or SCL = SDA = V_{BAT} (Note 5)	V_{BAT} = 3.63V		0.84	3.0	µA
			V_{BAT} = 5.5V		1.0	3.5	
Temperature Conversion Current	I_{BATTC}	$\overline{EOSC}$ = 0, BBSQW = 0, SCL = SDA = 0V or SCL = SDA = V_{BAT}	V_{BAT} = 3.63V			575	µA
			V_{BAT} = 5.5V			650	
Data-Retention Current	I_{BATTDR}	$\overline{EOSC}$ = 1, SCL = SDA = 0V, +25°C				100	nA

AC Electrical Characteristics

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$ or V_{BAT} = $V_{BAT(MIN)}$ to $V_{BAT(MAX)}$, V_{BAT} > V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

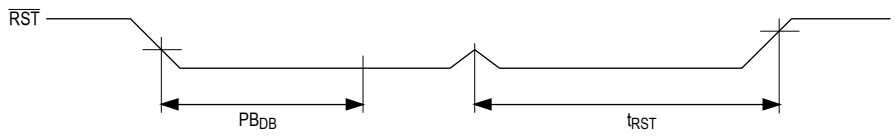
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode	100		400	kHz
		Standard mode	0		100	
Bus Free Time Between STOP and START Conditions	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Note 7)	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
Low Period of SCL Clock	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
High Period of SCL Clock	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Data Hold Time (Notes 8, 9)	$t_{HD:DAT}$	Fast mode	0		0.9	µs
		Standard mode	0		0.9	
Data Setup Time (Note 10)	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
START Setup Time	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Rise Time of Both SDA and SCL Signals (Note 11)	t_R	Fast mode	20 + 0.1C_B		300	ns
		Standard mode			1000	
Fall Time of Both SDA and SCL Signals (Note 11)	t_F	Fast mode	20 + 0.1C_B		300	ns
		Standard mode			300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.7			
Capacitive Load for Each Bus Line	C_B	(Note 11)			400	pF
Capacitance for SDA, SCL	$C_{I/O}$			10		pF
Pulse Width of Spikes That Must Be Suppressed by the Input Filter	t_{SP}			30		ns
Pushbutton Debounce	PB_{DB}			250		ms
Reset Active Time	t_{RST}			250		ms
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 12)		100		ms
Temperature Conversion Time	t_{CONV}			125	200	ms

Power-Switch Characteristics

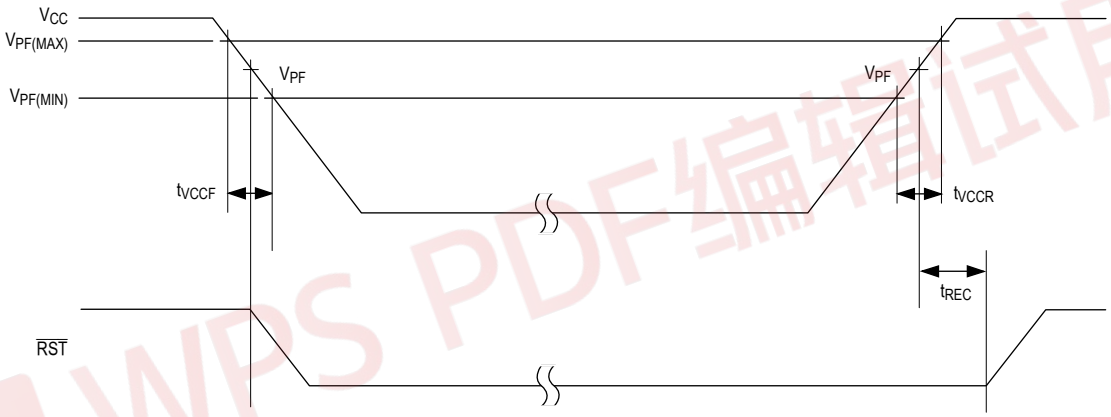
(T_A = T_{MIN} to T_{MAX})

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_{VCCF}		300			µs
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_{VCCR}		0			µs
Recovery at Power-Up	t_{REC}	(Note 13)		250	300	ms

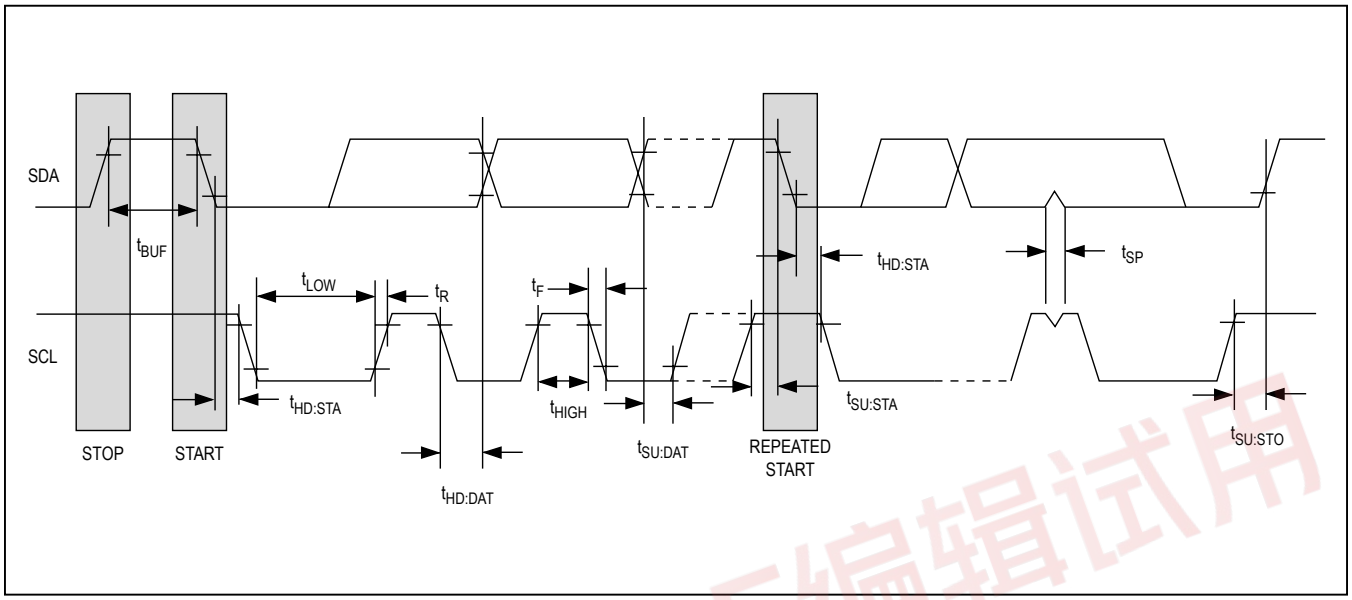
Pushbutton Reset Timing



Power-Switch Timing



Data Transfer on I2C Serial Bus



WARNING: Negative undershoots below -0.3V while the part is in battery-backed mode may cause loss of data.

Note 2: Limits at -40°C are guaranteed by design and not production tested.

Note 3: All voltages are referenced to ground.

Note 4: I_{CCA}—SCL clocking at max frequency = 400kHz.

Note 5: Current is the averaged input current, which includes the temperature conversion current.

Note 6: The $\overline{RST}$ pin has an internal 50kΩ (nominal) pullup resistor to V_{CC}.

Note 7: After this period, the first clock pulse is generated.

Note 8: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 9: The maximum $t_{HD:DAT}$ needs only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 10: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R(MAX)} + t_{SU:DAT} = 1000 + 250 = 1250ns$ before the SCL line is released.

Note 11: C_B—total capacitance of one bus line in pF.

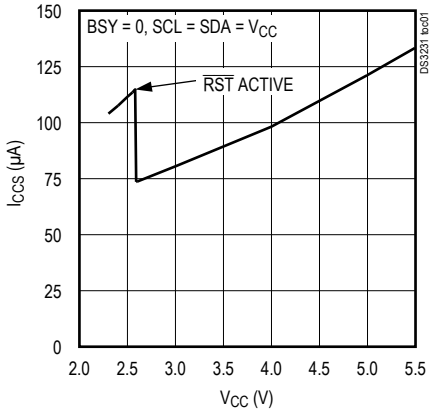
Note 12: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over the voltage range of $0.0V \leq V_{CC} \leq V_{CC(MAX)}$ and $2.3V \leq V_{BAT} \leq 3.4V$.

Note 13: This delay applies only if the oscillator is enabled and running. If the $\overline{EOSC}$ bit is a 1, t_{REC} is bypassed and $\overline{RST}$ immediately goes high. The state of $\overline{RST}$ does not affect the I2C interface, RTC, or TCXO.

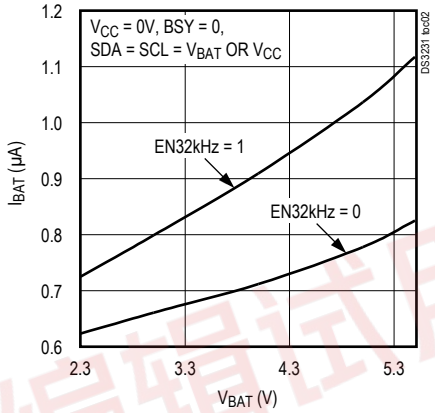
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

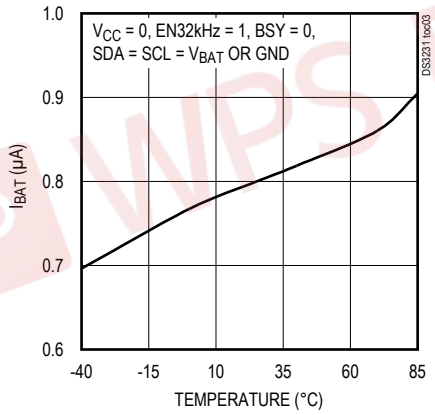
STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE



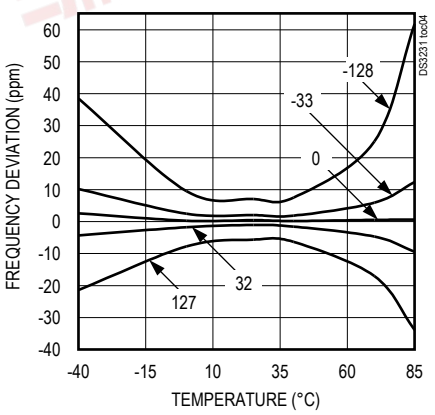
SUPPLY CURRENT vs. SUPPLY VOLTAGE



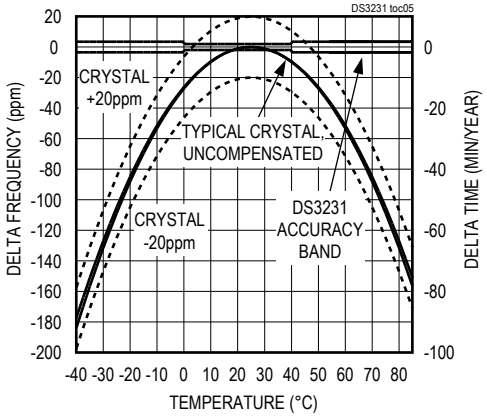
SUPPLY CURRENT vs. TEMPERATURE



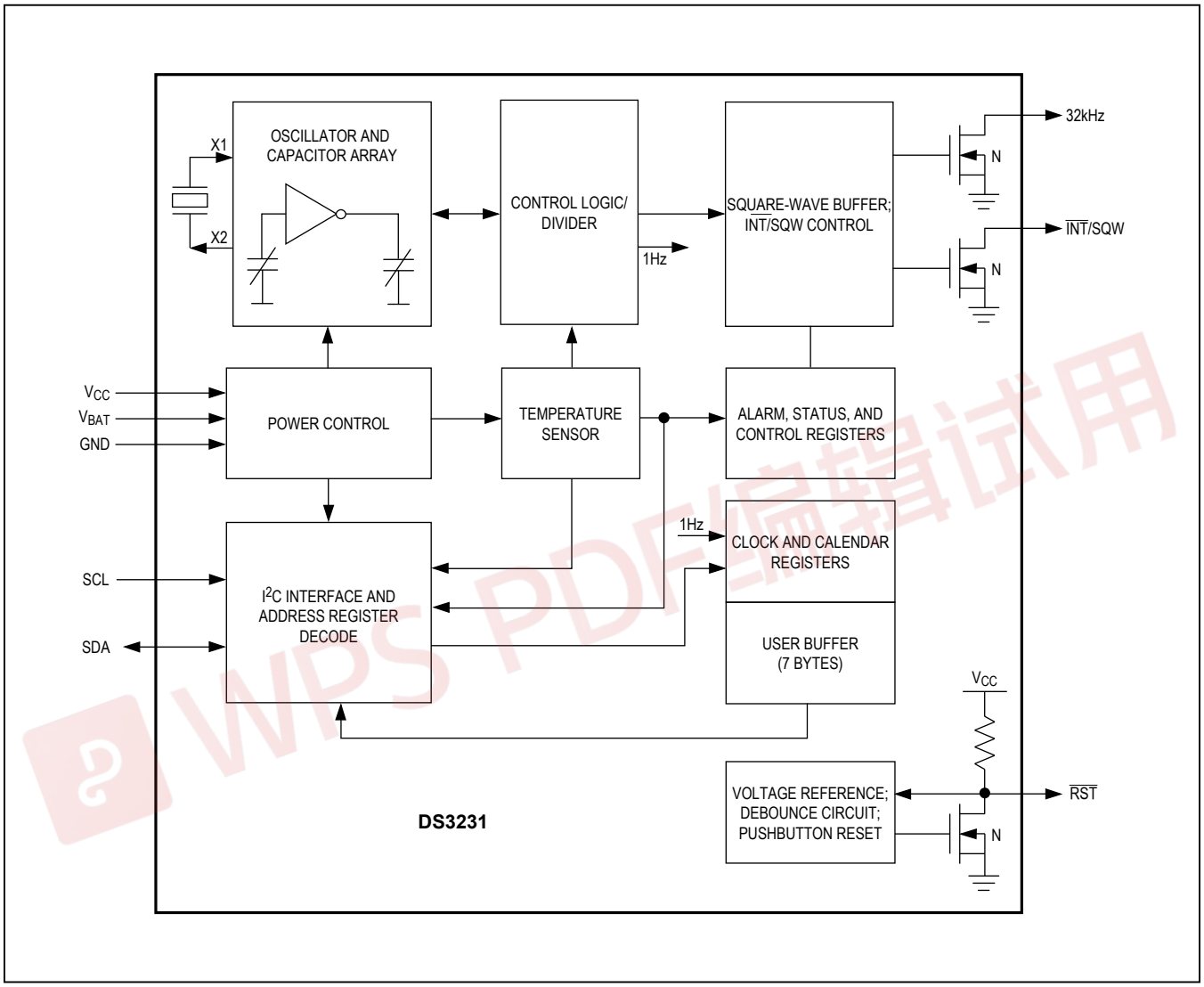
FREQUENCY DEVIATION vs. TEMPERATURE vs. AGING VALUE



DELTA TIME AND FREQUENCY vs. TEMPERATURE



Block Diagram



Pin Description

PIN	NAME	FUNCTION
1	32kHz	32kHz Output. This open-drain pin requires an external pullup resistor. When enabled, the output operates on either power supply. It may be left open if not used.
2	V_{CC}	DC Power Pin for Primary Power Supply. This pin should be decoupled using a 0.1µF to 1.0µF capacitor. If not used, connect to ground.
3	$\overline{INT}$/SQW	Active-Low Interrupt or Square-Wave Output. This open-drain pin requires an external pullup resistor connected to a supply at 5.5V or less. This multifunction pin is determined by the state of the INTCN bit in the Control Register (0Eh). When INTCN is set to logic 0, this pin outputs a square wave and its frequency is determined by RS2 and RS1 bits. When INTCN is set to logic 1, then a match between the timekeeping registers and either of the alarm registers activates the $\overline{INT}$/SQW pin (if the alarm is enabled). Because the INTCN bit is set to logic 1 when power is first applied, the pin defaults to an interrupt output with alarms disabled. The pullup voltage can be up to 5.5V, regardless of the voltage on V_{CC}. If not used, this pin can be left unconnected.
4	$\overline{RST}$	Active-Low Reset. This pin is an open-drain input/output. It indicates the status of V_{CC} relative to the V_{PF} specification. As V_{CC} falls below V_{PF}, the $\overline{RST}$ pin is driven low. When V_{CC} exceeds V_{PF}, for t_{RST}, the $\overline{RST}$ pin is pulled high by the internal pullup resistor. The active-low, open-drain output is combined with a debounced pushbutton input function. This pin can be activated by a pushbutton reset request. It has an internal 50kΩ nominal value pullup resistor to V_{CC}. No external pullup resistors should be connected. If the oscillator is disabled, t_{REC} is bypassed and $\overline{RST}$ immediately goes high.
5–12	N.C.	No Connection. Must be connected to ground.
13	GND	Ground
14	V_{BAT}	Backup Power-Supply Input. When using the device with the V_{BAT} input as the primary power source, this pin should be decoupled using a 0.1µF to 1.0µF low-leakage capacitor. When using the device with the V_{BAT} input as the backup power source, the capacitor is not required. If V_{BAT} is not used, connect to ground. The device is UL recognized to ensure against reverse charging when used with a primary lithium battery. Go to www.maximintegrated.com/qa/info/ul.
15	SDA	Serial Data Input/Output. This pin is the data input/output for the I²C serial interface. This open-drain pin requires an external pullup resistor. The pullup voltage can be up to 5.5V, regardless of the voltage on V_{CC}.
16	SCL	Serial Clock Input. This pin is the clock input for the I²C serial interface and is used to synchronize data movement on the serial interface. Up to 5.5V can be used for this pin, regardless of the voltage on V_{CC}.

Detailed Description

The DS3231 is a serial RTC driven by a temperature-compensated 32kHz crystal oscillator. The TCXO provides a stable and accurate reference clock, and maintains the RTC to within ±2 minutes per year accuracy from -40°C to +85°C. The TCXO frequency output is available at the 32kHz pin. The RTC is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output. The $\overline{INT}$/SQW provides either an interrupt signal due to alarm conditions or a square-wave output. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an $\overline{AM}$/PM indicator. The internal registers are accessible though an I²C bus interface.

A temperature-compensated voltage reference and comparator circuit monitors the level of V_{CC} to detect power failures and to automatically switch to the backup supply when necessary. The $\overline{RST}$ pin provides an external pushbutton function and acts as an indicator of a power-fail event.

Operation

The block diagram shows the main elements of the DS3231. The eight blocks can be grouped into four functional groups: TCXO, power control, pushbutton function, and RTC. Their operations are described separately in the following sections.

32kHz TCXO

The temperature sensor, oscillator, and control logic form the TCXO. The controller reads the output of the on-chip temperature sensor and uses a lookup table to determine the capacitance required, adds the aging correction in AGE register, and then sets the capacitance selection registers. New values, including changes to the AGE register, are loaded only when a change in the temperature value occurs, or when a user-initiated temperature conversion is completed. Temperature conversion occurs on initial application of V_{CC} and once every 64 seconds afterwards.

Power Control

This function is provided by a temperature-compensated voltage reference and a comparator circuit that monitors the V_{CC} level. When V_{CC} is greater than V_{PF}, the part is powered by V_{CC}. When V_{CC} is less than V_{PF} but greater than V_{BAT}, the DS3231 is powered by V_{CC}. If V_{CC} is less than V_{PF} and is less than V_{BAT}, the device is powered by V_{BAT}. See Table 1.

Table 1. Power Control

SUPPLY CONDITION	ACTIVE SUPPLY
$V_{CC} < V_{PF}$, $V_{CC} < V_{BAT}$	V_{BAT}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BAT}$	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BAT}$	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BAT}$	V_{CC}

To preserve the battery, the first time V_{BAT} is applied to the device, the oscillator will not start up until V_{CC} exceeds V_{PF}, or until a valid I2C address is written to the part. Typical oscillator startup time is less than one second. Approximately 2 seconds after V_{CC} is applied, or a valid I2C address is written, the device makes a temperature measurement and applies the calculated correction to the oscillator. Once the oscillator is running, it continues to run as long as a valid power source is available (V_{CC} or V_{BAT}), and the device continues to measure the temperature and correct the oscillator frequency every 64 seconds.

On the first application of power (V_{CC}) or when a valid I2C address is written to the part (V_{BAT}), the time and date registers are reset to 01/01/00 01 00:00:00 (DD/MM/YY DOW HH:MM:SS).

V_{BAT} Operation

There are several modes of operation that affect the amount of V_{BAT} current that is drawn. While the device is powered by V_{BAT} and the serial interface is active, active battery current, I_{BATA}, is drawn. When the serial interface is inactive, timekeeping current (I_{BATT}), which includes the averaged temperature conversion current, I_{BATTC}, is used (refer to Application Note 3644: *Power Considerations for Accurate Real-Time Clocks* for details). Temperature conversion current, I_{BATTC}, is specified since the system must be able to support the periodic higher current pulse and still maintain a valid voltage level. Data retention current, I_{BATTDR}, is the current drawn by the part when the oscillator is stopped ($\overline{EOSC}$ = 1). This mode can be used to minimize battery requirements for times when maintaining time and date information is not necessary, e.g., while the end system is waiting to be shipped to a customer.

Pushbutton Reset Function

The DS3231 provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS3231 is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low going edge. If an edge transition is detected, the DS3231 debounces the switch by pulling the $\overline{RST}$ low. After the internal timer has expired (PB_{DB}), the DS3231 continues to monitor the $\overline{RST}$ line. If the line is still low, the DS3231 continuously monitors the line looking for a rising edge. Upon detecting release, the DS3231 forces the $\overline{RST}$ pin low and holds it low for t_{RST}.

$\overline{RST}$ is also used to indicate a power-fail condition. When V_{CC} is lower than V_{PF}, an internal power-fail signal is generated, which forces the $\overline{RST}$ pin low. When V_{CC} returns to a level above V_{PF}, the $\overline{RST}$ pin is held low for approximately 250ms (t_{REC}) to allow the power supply to stabilize. If the oscillator is not running (see the *Power Control* section) when V_{CC} is applied, t_{REC} is bypassed and $\overline{RST}$ immediately goes high. Assertion of the $\overline{RST}$ output, whether by pushbutton or power-fail detection, does not affect the internal operation of the DS3231.

Real-Time Clock

With the clock source from the TCXO, the RTC provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an $\overline{AM}$/PM indicator.

The clock provides two programmable time-of-day alarms and a programmable square-wave output. The $\overline{INT}$/SQW pin either generates an interrupt due to alarm condition or outputs a square-wave signal and the selection is controlled by the bit INTCN.

ADDRESS	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB	FUNCTION	RANGE
00h	0	10 Seconds			Seconds				Seconds	00–59
01h	0	10 Minutes			Minutes				Minutes	00–59
02h	0	12/$\overline{24}$	$\overline{AM}$/PM 20 Hour	10 Hour	Hour				Hours	1–12 + $\overline{AM}$/PM 00–23
03h	0	0	0	0	0	Day			Day	1–7
04h	0	0	10 Date		Date				Date	01–31
05h	Century	0	0	10 Month	Month				Month/ Century	01–12 + Century
06h	10 Year				Year				Year	00–99
07h	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00–59
08h	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00–59
09h	A1M3	12/$\overline{24}$	$\overline{AM}$/PM 20 Hour	10 Hour	Hour				Alarm 1 Hours	1–12 + $\overline{AM}$/PM 00–23
0Ah	A1M4	DY/$\overline{DT}$	10 Date		Day				Alarm 1 Day	1–7
					Date				Alarm 1 Date	1–31
0Bh	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00–59
0Ch	A2M3	12/$\overline{24}$	$\overline{AM}$/PM 20 Hour	10 Hour	Hour				Alarm 2 Hours	1–12 + $\overline{AM}$/PM 00–23
0Dh	A2M4	DY/$\overline{DT}$	10 Date		Day				Alarm 2 Day	1–7
					Date				Alarm 2 Date	1–31
0Eh	$\overline{EOSC}$	BBSQW	CONV	RS2	RS1	INTCN	A2IE	A1IE	Control	—
0Fh	OSF	0	0	0	EN32kHz	BSY	A2F	A1F	Control/Status	—
10h	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA	Aging Offset	—
11h	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA	MSB of Temp	—
12h	DATA	DATA	0	0	0	0	0	0	LSB of Temp	—

Figure 1. Timekeeping Registers

Note: *Unless otherwise specified, the registers' state is not defined when power is first applied.*

Address Map

Figure 1 shows the address map for the DS3231 timekeeping registers. During a multibyte access, when the address pointer reaches the end of the register space (12h), it wraps around to location 00h. On an I²C START or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to reread the registers in case the main registers update during a read.

I²C Interface

The I²C interface is accessible whenever either V_{CC} or V_{BAT} is at a valid level. If a microcontroller connected to the DS3231 resets because of a loss of V_{CC} or other event, it is possible that the microcontroller and DS3231 I²C communications could become unsynchronized, e.g., the microcontroller resets while reading data from the DS3231. When the microcontroller resets, the DS3231 I²C interface may be placed into a known state by toggling SCL until SDA is observed to be at a high level. At that point the microcontroller should pull SDA low while SCL is high, generating a START condition.

Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. Figure 1 illustrates the RTC registers. The time and calendar data are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded

decimal (BCD) format. The DS3231 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{AM}$/PM bit with logic-high being PM. In the 24-hour mode, bit 5 is the 20-hour bit (20–23 hours). The century bit (bit 7 of the month register) is toggled when the years register overflows from 99 to 00.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any START and when the register pointer rolls over to zero. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read.

The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge from the DS3231. Once the countdown chain is reset, to avoid rollover issues the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enabled, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

Alarms

The DS3231 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh. The alarms can be programmed (by the alarm enable and INTCN bits of the control register) to activate the $\overline{INT}$/SQW output on an alarm match condition. Bit 7 of each of the time-of-day/date alarm registers are mask bits (Table 2). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 2 shows the possible settings. Configurations not listed in the table will result in illogical operation.

The DY/$\overline{DT}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/$\overline{DT}$ is written to logic 0, the alarm will be the result of a match with date of the month. If DY/$\overline{DT}$ is written to logic 1, the alarm will be the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding Alarm Flag ‘A1F’ or ‘A2F’ bit is set to logic 1. If the corresponding Alarm Interrupt Enable ‘A1IE’ or ‘A2IE’ is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition will activate the $\overline{INT}$/SQW signal. The match is tested on the once-per-second update of the time and date registers.

Table 2. Alarm Mask Bits

DY/$\overline{DT}$	ALARM 1 REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/$\overline{DT}$	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 seconds of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

Control Register (0Eh)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	$\overline{EOSC}$	BBSQW	CONV	RS2	RS1	INTCN	A2IE	A1IE
POR:	0	0	0	1	1	1	0	0

Special-Purpose Registers

The DS3231 has two additional registers (control and status) that control the real-time clock, alarms, and square-wave output.

Control Register (0Eh)

Bit 7: Enable Oscillator ($\overline{EOSC}$). When set to logic 0, the oscillator is started. When set to logic 1, the oscillator is stopped when the DS3231 switches to V_{BAT}. This bit is clear (logic 0) when power is first applied. When the DS3231 is powered by V_{CC}, the oscillator is always on regardless of the status of the $\overline{EOSC}$ bit. When $\overline{EOSC}$ is disabled, all register data is static.

Bit 6: Battery-Backed Square-Wave Enable (BBSQW). When set to logic 1 with INTCN = 0 and $V_{CC} < V_{PF}$, this bit enables the square wave. When BBSQW is logic 0, the $\overline{INT}$/SQW pin goes high impedance when $V_{CC} < V_{PF}$. This bit is disabled (logic 0) when power is first applied.

Bit 5: Convert Temperature (CONV). Setting this bit to 1 forces the temperature sensor to convert the temperature into digital code and execute the TCXO algorithm to update the capacitance array to the oscillator. This can only happen when a conversion is not already in progress. The user should check the status bit BSY before forcing the controller to start a new TCXO execution. A user-initiated temperature conversion does not affect the internal 64-second update cycle.

A user-initiated temperature conversion does not affect the BSY bit for approximately 2ms. The CONV bit remains at a 1 from the time it is written until the conversion is finished, at which time both CONV and BSY go to 0. The CONV bit should be used when monitoring the status of a user-initiated conversion.

Bits 4 and 3: Rate Select (RS2 and RS1). These bits control the frequency of the square-wave output when the square wave has been enabled. The following table shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (8.192kHz) when power is first applied.

SQUARE-WAVE OUTPUT FREQUENCY

RS2	RS1	SQUARE-WAVE OUTPUT FREQUENCY
0	0	1Hz
0	1	1.024kHz
1	0	4.096kHz
1	1	8.192kHz

Bit 2: Interrupt Control (INTCN). This bit controls the $\overline{INT}$/SQW signal. When the INTCN bit is set to logic 0, a square wave is output on the $\overline{INT}$/SQW pin. When the INTCN bit is set to logic 1, then a match between the timekeeping registers and either of the alarm registers activates the $\overline{INT}$/SQW output (if the alarm is also enabled). The corresponding alarm flag is always set regardless of the state of the INTCN bit. The INTCN bit is set to logic 1 when power is first applied.

Bit 1: Alarm 2 Interrupt Enable (A2IE). When set to logic 1, this bit permits the alarm 2 flag (A2F) bit in the status register to assert $\overline{INT}$/SQW (when INTCN = 1). When the A2IE bit is set to logic 0 or INTCN is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Bit 0: Alarm 1 Interrupt Enable (A1IE). When set to logic 1, this bit permits the alarm 1 flag (A1F) bit in the status register to assert $\overline{INT}$/SQW (when INTCN = 1). When the A1IE bit is set to logic 0 or INTCN is set to logic 0, the A1F bit does not initiate the $\overline{INT}$/SQW signal. The A1IE bit is disabled (logic 0) when power is first applied.

Status Register (0Fh)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	OSF	0	0	0	EN32kHz	BSY	A2F	A1F
POR:	1	0	0	0	1	X	X	X

Status Register (0Fh)

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period and may be used to judge the validity of the timekeeping data. This bit is set to logic 1 any time that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltages present on both V_{CC} and V_{BAT} are insufficient to support oscillation.
3) The $\overline{EOSC}$ bit is turned off in battery-backed mode.
4) External influences on the crystal (i.e., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.

Bit 3: Enable 32kHz Output (EN32kHz). This bit controls the status of the 32kHz pin. When set to logic 1, the 32kHz pin is enabled and outputs a 32.768kHz square-wave signal. When set to logic 0, the 32kHz pin goes to a high-impedance state. The initial power-up state of this bit is logic 1, and a 32.768kHz square-wave signal appears at the 32kHz pin after a power source is applied to the DS3231 (if the oscillator is running).

Bit 2: Busy (BSY). This bit indicates the device is busy executing TCXO functions. It goes to logic 1 when the conversion signal to the temperature sensor is asserted and then is cleared when the device is in the 1-minute idle state.

Bit 1: Alarm 2 Flag (A2F). A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. If the A2IE bit is logic 1 and the INTCN bit is set to logic 1, the $\overline{INT}$/SQW pin is also asserted. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Bit 0: Alarm 1 Flag (A1F). A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is logic 1 and the INTCN bit is set to logic 1, the $\overline{INT}$/SQW pin is also asserted. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Aging Offset

The aging offset register takes a user-provided value to add to or subtract from the codes in the capacitance array registers. The code is encoded in two's complement, with bit 7 representing the sign bit. One LSB represents one small capacitor to be switched in or out of the capacitance array at the crystal pins. The aging offset register capacitance value is added or subtracted from the capacitance value that the device calculates for each temperature compensation. The offset register is added to the capacitance array during a normal temperature conversion, if the temperature changes from the previous conversion, or during a manual user conversion (setting the CONV bit). To see the effects of the aging register on the 32kHz output frequency immediately, a manual conversion should be started after each aging register change.

Positive aging values add capacitance to the array, slowing the oscillator frequency. Negative values remove capacitance from the array, increasing the oscillator frequency.

The change in ppm per LSB is different at different temperatures. The frequency vs. temperature curve is shifted by the values used in this register. At +25°C, one LSB typically provides about 0.1ppm change in frequency.

Use of the aging register is not needed to achieve the accuracy as defined in the EC tables, but could be used to help compensate for aging at a given temperature. See the *Typical Operating Characteristics* section for a graph showing the effect of the register on accuracy over temperature.

Aging Offset (10h)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	Sign	Data	Data	Data	Data	Data	Data	Data
POR:	0	0	0	0	0	0	0	0

Temperature Register (Upper Byte) (11h)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	Sign	Data	Data	Data	Data	Data	Data	Data
POR:	0	0	0	0	0	0	0	0

Temperature Register (Lower Byte) (12h)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	Data	Data	0	0	0	0	0	0
POR:	0	0	0	0	0	0	0	0

Temperature Registers (11h–12h)

Temperature is represented as a 10-bit code with a resolution of 0.25°C and is accessible at location 11h and 12h. The temperature is encoded in two's complement format. The upper 8 bits, the integer portion, are at location 11h and the lower 2 bits, the fractional portion, are in the upper nibble at location 12h. For example, 00011001 01b = +25.25°C. Upon power reset, the registers are set to a default temperature of 0°C and the controller starts a temperature conversion. The temperature is read on initial application of V_{CC} or I2C access on V_{BAT} and once every 64 seconds afterwards. The temperature registers are updated after each user-initiated conversion and on every 64-second conversion. The temperature registers are read-only.

I2C Serial Data Bus

The DS3231 supports a bidirectional I2C bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data is defined as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS3231 operates as a slave on the I2C bus. Connections to the bus are made through the SCL input and open-drain SDA I/O lines. Within the bus specifications, a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The DS3231 works in both modes.

The following bus protocol has been defined (Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain high.

START data transfer: A change in the state of the data line from high to low, while the clock line is high, defines a START condition.

STOP data transfer: A change in the state of the data line from low to high, while the clock line is high, defines a STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and the STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generat-

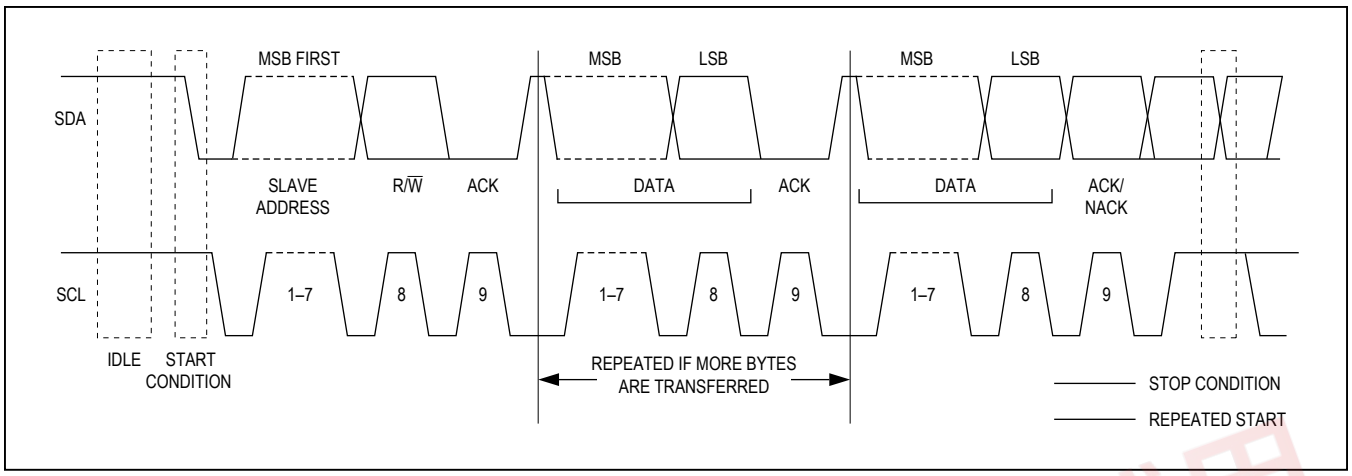


Figure 2. I2C Data Transfer Overview

ing an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

Figures 3 and 4 detail how data transfer is accomplished on the I2C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the

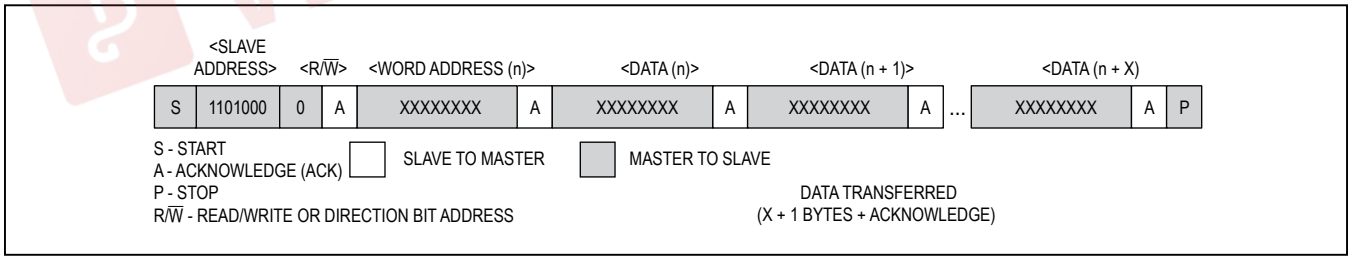


Figure 3. Data Write—Slave Receiver Mode

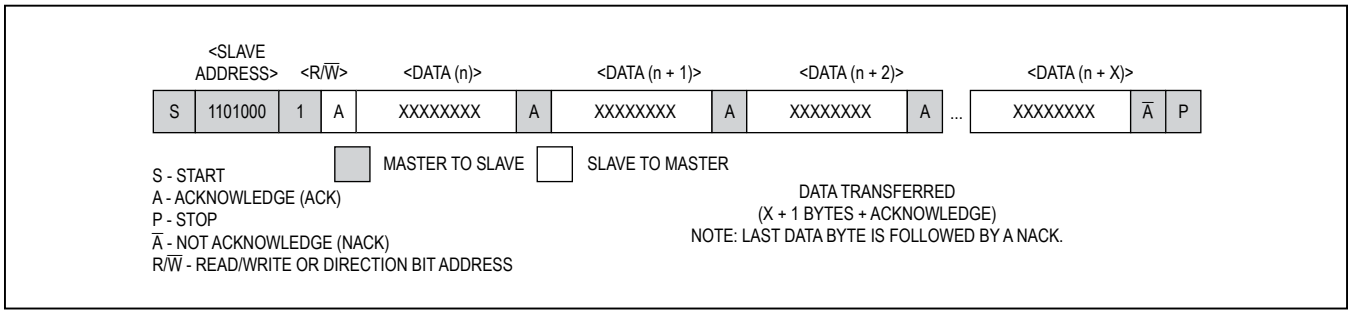


Figure 4. Data Read—Slave Transmitter Mode

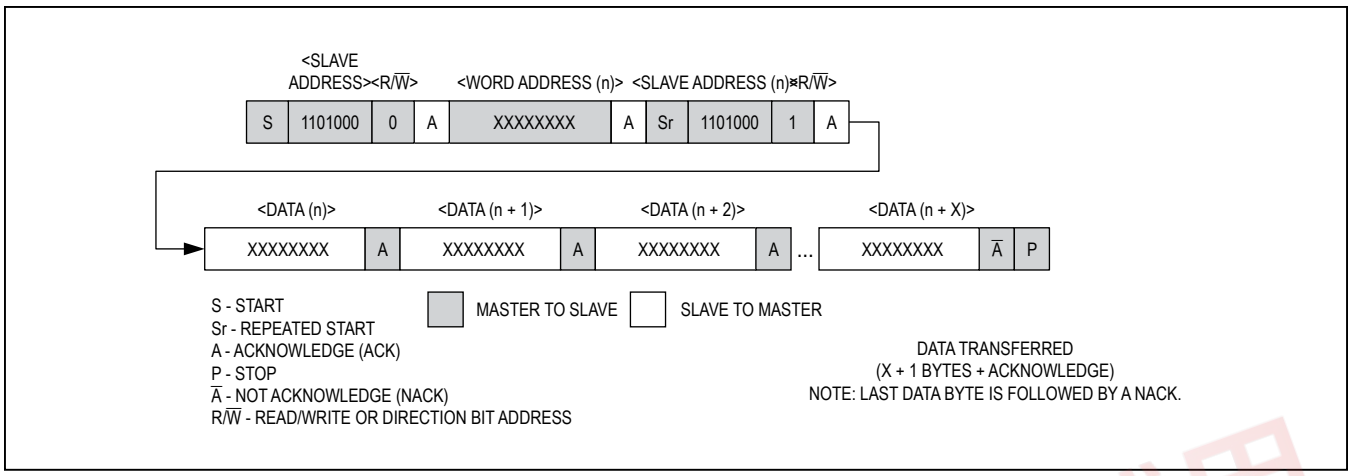


Figure 5. Data Write/Read (Write Pointer, Then Read)—Slave Receive and Transmit

last byte. At the end of the last received byte, a not acknowledge is returned.

The master device generates all the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released. Data is transferred with the most significant bit (MSB) first.

The DS3231 can operate in the following two modes:

Slave receiver mode (DS3231 write mode): Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit. The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit DS3231 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 0 for a write. After receiving and decoding the slave address byte, the DS3231 outputs an acknowledge on SDA. After the DS3231 acknowledges the slave address + write bit, the master transmits a word address to the DS3231. This sets the register pointer on the DS3231, with the DS3231 acknowledging the transfer. The master may then transmit zero or more bytes of data, with the DS3231 acknowledging each byte received. The register pointer increments after each data byte is transferred. The master generates a STOP condition to terminate the data write.

Slave transmitter mode (DS3231 read mode): The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS3231 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit DS3231 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 1 for a read. After receiving and decoding the slave address byte, the DS3231 outputs an acknowledge on SDA. The DS3231 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode, the first address that is read is the last one stored in the register pointer. The DS3231 must receive a not acknowledge to end a read.

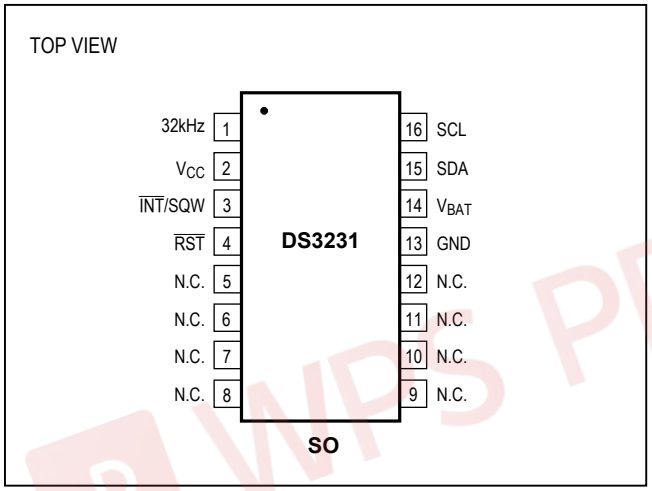
Handling, PCB Layout, and Assembly

The DS3231 package contains a quartz tuning-fork crystal. Pick-and-place equipment can be used, but precautions should be taken to ensure that excessive shocks are avoided. Ultrasonic cleaning should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All N.C. (no connect) pins must be connected to ground.

Moisture-sensitive packages are shipped from the factory dry packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications and reflow profiles. Exposure to reflow is limited to 2 times maximum.

Pin Configuration



Chip Information

SUBSTRATE CONNECTED TO GROUND

PROCESS: CMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS3231S#	0°C to +70°C	16 SO
DS3231SN#	-40°C to +85°C	16 SO

#Denotes an RoHS-compliant device that may include lead (Pb) that is exempt under RoHS requirements. The lead finish is JESD97 category e3, and is compatible with both lead-based and lead-free soldering processes. A "#" anywhere on the top mark denotes an RoHS-compliant device.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 SO	W16#H2	21-0042	90-0107

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/05	Initial release.	—
1	2/05	Changed Digital Temp Sensor Output from ±2°C to ±3°C.	1, 3
		Updated *Typical Operating Circuit*.	1
		Changed T_A = -40°C to +85°C to T_A = T_{MIN} to T_{MAX}.	2, 3, 4
		Updated *Block Diagram*.	8
2	6/05	Added “UL Recognized” to Features; added lead-free packages and removed S from top mark info in *Ordering Information* table; added ground connections to the N.C. pin in the Typical Operating Circuit.	1
		Added “noncondensing” to operating temperature range; changed V_{PF} MIN from 2.35V to 2.45V.	2
		Added aging offset specification.	3
		Relabeled TOC4.	7
		Added arrow showing input on X1 in the *Block Diagram*.	8
		Updated pin descriptions for V_{CC} and V_{BAT}.	9
		Added the I²C Interface section.	10
		Figure 1: Added sign bit to aging and temperature registers; added MSB and LSB.	11
		Corrected title for rate select bits frequency table.	13
		Added note that frequency stability over temperature spec is with aging offset register = 00h; changed bit 7 from Data to Sign (Crystal Aging Offset Register).	14
		Changed bit 7 from Data to Sign (Temperature Register); correct pin definitions in *I²C Serial Data Bus* section.	15
		Modified the *Handing*, *PC Board Layout*, and *Assembly* section to refer to J-STD-020 for reflow profiles for lead-free and leaded packages.	17
3	11/05	Changed lead-free packages to RoHS-compliant packages.	1
4	10/06	Changed $\overline{RST}$ and UL bullets in *Features*.	1
		Changed EC condition “V_{CC} > V_{BAT}” to “V_{CC} = Active Supply (see Table 1).”	2, 3
		Modified Note 12 to correct t_{REC} operation.	6
		Added various conditions text to TOCs 1, 2, and 3.	7
		Added text to pin descriptions for 32kHz, V_{CC}, and $\overline{RST}$.	9
		Table 1: Changed column heading “Powered By” to “Active Supply”; changed “applied” to “exceeds V_{PF}” in the *Power Control* section.	10
		Indicated BBSQW applies to both SQW and interrupts; simplified temp convert description (bit 5); added “output” to $\overline{INT}$/SQW (bit 2).	13
		Changed the *Crystal Aging* section to the *Aging Offset* section; changed “this bit indicates” to “this bit controls” for the enable 32kHz output bit.	14
5	4/08	Added Warning note to EC table notes; updated Note 12.	6
		Updated the *Typical Operating Characteristics* graphs.	7
		In the *Power Control* section, added information about the POR state of the time and date registers; in the *Real-Time Clock* section, added to the description of the RST function.	10
		In Figure 1, corrected the months date range for 04h from 00–31 to 01–31.	11

Revision History (continued)

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
6	10/08	Updated the *Typical Operating Circuit*.	1
		Removed the V_{PU} parameter from the *Recommended DC Operating Conditions* table and added verbiage about the pullup to the *Pin Description* table for $\overline{INT}$/SQW, SDA, and SCL.	2, 9
		Added the Delta Time and Frequency vs. Temperature graph in the *Typical Operating Characteristics* section.	7
		Updated the *Block Diagram*.	8
		Added the V_{BAT} *Operation* section, improved some sections of text for the *32kHz TCXO* and *Pushbutton Reset Function* sections.	10
		Added the register bit POR values to the register tables.	13, 14, 15
		Updated the *Aging Offset* and *Temperature Registers (11h–12h)* sections.	14, 15
		Updated the I2C timing diagrams (Figures 3, 4, and 5).	16, 17
7	3/10	Removed the “S” from the top mark in the *Ordering Information* table and the *Pin Configuration* to match the packaging engineering marking specification.	1, 18
8	7/10	Updated the *Typical Operating Circuit*; removed the “Top Mark” column from the *Ordering Information*; in the *Absolute Maximum Ratings* section, added the theta-JA and theta-JC thermal resistances and Note 1, and changed the soldering temperature to +260°C (lead(Pb)-free) and +240°C (leaded); updated the functional description of the V_{BAT} pin in the *Pin Description*; changed the timekeeping registers 02h, 09h, and 0Ch to “20 Hour” in Bit 5 of Figure 1; updated the BBSQW bit description in the *Control Register (0Eh)* section; added the land pattern no. to the *Package Information* table.	1, 2, 3, 4, 6, 9, 11, 12, 13, 18
9	1/13	Updated *Absolute Maximum Ratings*, and last paragraph in *Power Control* section	2, 10
10	3/15	Revised *Benefits and Features* section.	1

DS3234

Extremely Accurate SPI Bus RTC with Integrated Crystal and SRAM

General Description

The DS3234 is a low-cost, extremely accurate SPI bus real-time clock (RTC) with an integrated temperature-compensated crystal oscillator (TCXO) and crystal. The DS3234 incorporates a precision, temperature-compensated voltage reference and comparator circuit to monitor V_{CC}. When V_{CC} drops below the power-fail voltage (V_{PF}), the device asserts the $\overline{RST}$ output and also disables read and write access to the part when V_{CC} drops below both V_{PF} and V_{BAT}. The $\overline{RST}$ pin is monitored as a pushbutton input for generating a µP reset. The device switches to the backup supply input and maintains accurate timekeeping when main power to the device is interrupted. The integration of the crystal resonator enhances the long-term accuracy of the device as well as reduces the piece-part count in a manufacturing line. The DS3234 is available in commercial and industrial temperature ranges, and is offered in an industry-standard 300-mil, 20-pin SO package.

The DS3234 also integrates 256 bytes of battery-backed SRAM. In the event of main power loss, the contents of the memory are maintained by the power source connected to the V_{BAT} pin. The RTC maintains seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. Two programmable time-of-day alarms and a programmable square-wave output are provided. Address and data are transferred serially by an SPI bidirectional bus.

Applications

Servers
Telematics
Utility Power Meters
GPS

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Benefits and Features

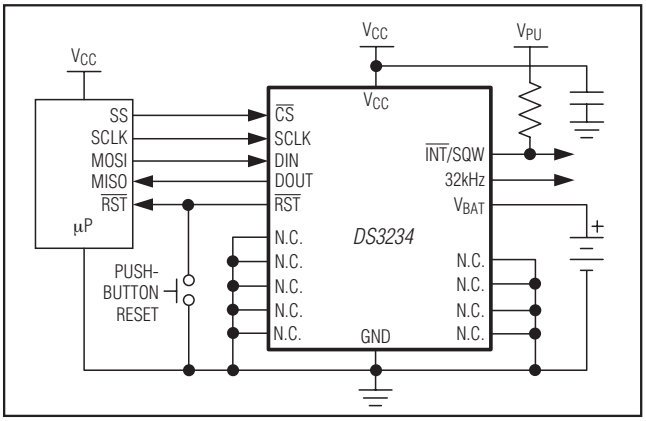
- Highly Accurate RTC with Integrated Crystal and SRAM Completely Manages All Timekeeping Functions
  - Accuracy ±2ppm from 0°C to +40°C
  - Accuracy ±3.5ppm from -40°C to +85°C
  - Real-Time Clock Counts Seconds, Minutes, Hours, Day, Date, Month, and Year, with Leap Year Compensation Valid Up to 2099
  - Digital Temp Sensor Output: ±3°C Accuracy
  - Register for Aging Trim
  - $\overline{RST}$ Input/Output
  - Two Time-of-Day Alarms
  - Programmable Square-Wave Output
- Simple Serial Interface Connects to Most Microcontrollers
  - 4MHz SPI Bus Supports Modes 1 and 3
- Battery-Backup Input for Continuous Timekeeping
  - Low Power Operation Extends Battery Backup Run Time
- Operating Temperature Ranges: Commercial: 0°C to +70°C, Industrial: -40°C to +85°C
- 300-Mil, 20-Pin SO Package
- Underwriters Laboratories® (UL) Recognized

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
DS3234S#	0°C to +70°C	20 SO	DS3234S
DS3234SN#	-40°C to +85°C	20 SO	DS3234SN

#Denotes an RoHS-compliant device that may include lead(Pb) that is exempt under the RoHS requirements. Lead finish is JESD97 Category e3, and is compatible with both lead-based and lead-free soldering processes. A "#" anywhere on the top mark denotes an RoHS-compliant device.

Typical Operating Circuit



19-5339; Rev 4; 3/15

maxim integrated™

Absolute Maximum Ratings

Voltage Range on Any Pin Relative to Ground.....-0.3V to +6.0V
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1) ...55°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1).....24°C/W
Operating Temperature Range
(noncondensing) .....-40°C to +85°C
Junction Temperature.....+125°C
Storage Temperature Range .....-40°C to +85°C
Lead Temperature (soldering, 10s) .....+260°C
Soldering Temperature (reflow, 2 times max) .....+260°C
(See the *Handling, PC Board Layout, and Assembly* section.)

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.0	3.3	5.5	V
	V_{BAT}		2.0	3.0	3.8	
Logic 1 Input $\overline{CS}$, SCLK, DIN	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Logic 0 Input $\overline{CS}$, SCLK, DIN, $\overline{RST}$	V_{IL}	2.0V ≤ V_{CC} ≤ 3.63V	-0.3		+0.2 x V_{CC}	V
		3.63V < V_{CC} ≤ 5.5V	-0.3		+0.7	

Electrical Characteristics

(V_{CC} = 2.0V to 5.5V, V_{CC} = active supply (see Table 1), T_A = -40°C to +85°C, unless otherwise noted.) (Typical values are at **V_{CC} = 3.3V, V_{BAT} = 3.0V**, and T_A = +25°C, unless otherwise noted. TCXO operation guaranteed from 2.3V to 5.5V on V_{CC} and 2.3V to 3.8V on V_{BAT}.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Active Supply Current	I_{CCA}	SCLK = 4MHz, BSY = 0 (Notes 4, 5)	V_{CC} = 3.63V			400	µA
			V_{CC} = 5.5V			700	
Standby Supply Current	I_{CCS}	$\overline{CS}$ = V_{IH}, 32kHz output off, SQW output off (Note 5)	V_{CC} = 3.63V			120	µA
			V_{CC} = 5.5V			160	
Temperature Conversion Current	$I_{CCSCONV}$	SPI bus inactive, 32kHz output off, SQW output off	V_{CC} = 3.63V			500	µA
			V_{CC} = 5.5V			600	
Power-Fail Voltage	V_{PF}			2.45	2.575	2.70	V
V_{BAT} Leakage Current	I_{BATLKG}				25	100	nA
(V_{CC} = 2.0V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2 and 3)							
Logic 1 Output, 32kHz I_{OH} = -500µA I_{OH} = -250µA I_{OH} = -125µA	V_{OH}	V_{CC} > 3.63V, 3.63V > V_{CC} > 2.7V, 2.7V > (V_{CC} or V_{BAT}) > 2.0V (BB32kHz = 1)		0.85 x V_{CC}			V

Electrical Characteristics (continued)

(V_{CC} = 2.0V to 5.5V, V_{CC} = active supply (see Table 1), T_A = -40°C to +85°C, unless otherwise noted.) (Typical values are at **V_{CC} = 3.3V, V_{BAT} = 3.0V**, and T_A = +25°C, unless otherwise noted. TCXO operation guaranteed from 2.3V to 5.5V on V_{CC} and 2.3V to 3.8V on V_{BAT}.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic 0 Output, 32kHz	V_{OL}	I_{OL} = 1mA				0.4	V
Logic 1 Output, DOUT	V_{OH}	I_{OH} = -1.0mA		0.85 x V_{CC}			V
Logic 0 Output, DOUT, $\overline{INT}$/SQW	V_{OL}	I_{OL} = 3mA				0.4	V
Logic 0 Output, $\overline{RST}$	V_{OL}	I_{OL} = 1.0mA				0.4	V
Output Leakage Current 32kHz, $\overline{INT}$/SQW, DOUT	I_{LO}	Output high impedance		-1	0	+1	µA
Input Leakage DIN, $\overline{CS}$, SCLK	I_{LI}			-1		+1	µA
$\overline{RST}$ Pin I/O Leakage	I_{OL}	$\overline{RST}$ high impedance (Note 6)		-200		+10	µA
TCXO (V_{CC} = 2.3V to 5.5V, V_{BAT} = 2.3V to 3.8V, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2 and 3)							
Output Frequency	f_{OUT}	V_{CC} = 3.3V or V_{BAT} = 3.3V			32.768		kHz
Frequency Stability vs. Temperature	$\Delta f/f_{OUT}$	V_{CC} = 3.3V or V_{BAT} = 3.3V	0°C to +40°C	-2		+2	ppm
			-40°C to 0°C and +40°C to +85°C	-3.5		+3.5	
Frequency Stability vs. Voltage	$\Delta f/V$				1		ppm/V
Trim Register Frequency Sensitivity per LSB	Δf/LSB	Specified at:	-40°C		0.7		ppm
			+25°C		0.1		
			+70°C		0.4		
			+85°C		0.8		
Temperature Accuracy	Temp			-3		+3	°C
Crystal Aging	$\Delta f/f_{OUT}$	After reflow, not production tested	First year		±1.0		ppm
			0–10 years		±5.0		

Electrical Characteristics

(**V_{CC} = 0V, V_{BAT} = 2.0V to 3.8V**, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Timekeeping Battery Current (Note 5)	I_{BATT}	$\overline{EOSC}$ = 0, BBSQW = 0, CRATE1 = CRATE0 = 0	V_{BAT} = 3.4V		1.5	2.3	µA
			V_{BAT} = 3.8V		1.5	2.5	
Temperature Conversion Current	I_{BATTC}	$\overline{EOSC}$ = 0, BBSQW = 0				400	µA
Data-Retention Current	I_{BATTDR}	$\overline{EOSC}$ = 1				100	nA

Electrical Characteristics

(V_{CC} = 2.0V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Frequency	f_{SCL}	2.7V ≤ V_{CC} ≤ 5.5V			4	MHz
		2.0V ≤ V_{CC} < 2.7V			2	
Data to SCLK Setup	t_{DC}		30			ns
SCLK to Data Hold	t_{CDH}		30			ns
SCLK to $\overline{CS}$ Setup	t_{CCS}		30			ns
SCLK to Data Valid (Note 7)	t_{CDD}	2.7V ≤ V_{CC} ≤ 5.5V			80	ns
		2.0V ≤ V_{CC} < 2.7V			160	
SCLK Low Time	t_{CL}	2.7V ≤ V_{CC} ≤ 5.5V	110			ns
		2.0V ≤ V_{CC} < 2.7V	220			
SCLK High Time	t_{CH}	2.7V ≤ V_{CC} ≤ 5.5V	110			ns
		2.0V ≤ V_{CC} < 2.7V	220			
SCLK Rise and Fall	t_R, t_F				200	ns
$\overline{CS}$ to SCLK Setup	t_{CC}		400			ns
SCLK to $\overline{CS}$ Hold	t_{CCH}	2.7V ≤ V_{CC} ≤ 5.5V	100			ns
		2.0V ≤ V_{CC} < 2.7V	200			
$\overline{CS}$ Inactive Time	t_{CWH}		400			ns
$\overline{CS}$ to Output High Impedance	t_{CDZ}	(Note 8)			40	ns
Pushbutton Debounce	PBDB			250		ms
Reset Active Time	t_{RST}			250		ms
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 9)		100		ms
Temperature Conversion Time	t_{CONV}			125	200	ms

Power-Switch Characteristics

5(T_A = -40°C to +85°C)

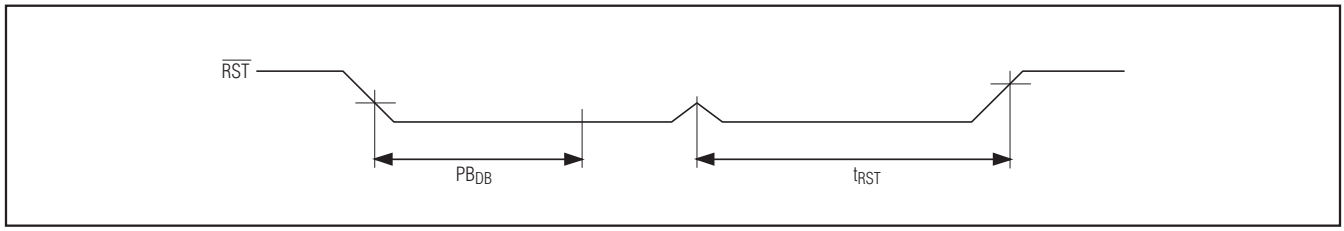
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_{VCCF}		300			µs
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_{VCCR}		0			µs
Recovery at Power-Up	t_{REC}	(Note 10)		125	300	ms

Capacitance

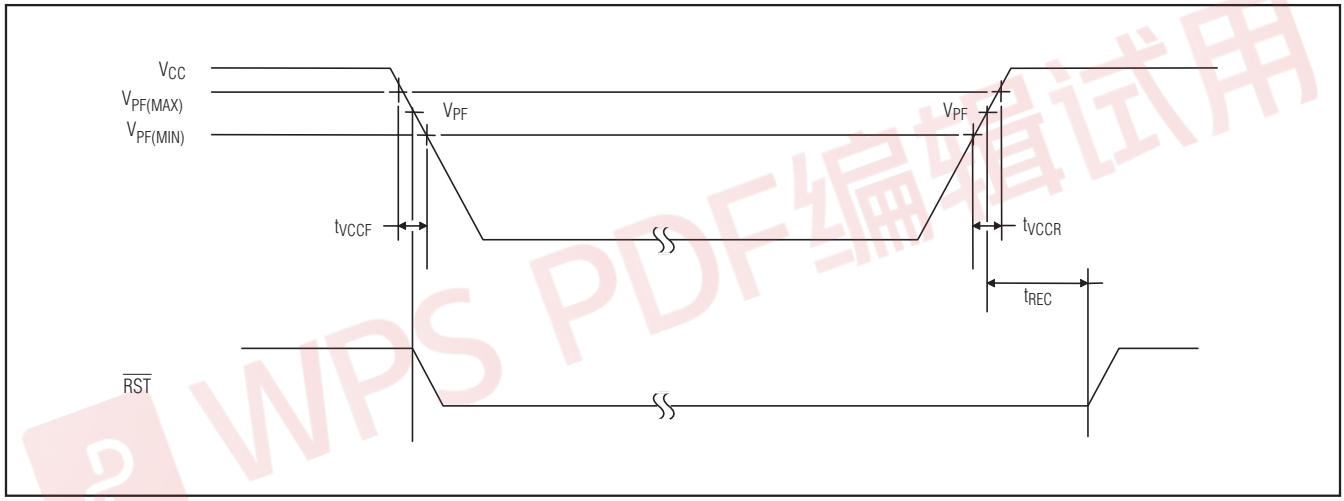
(T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Capacitance on All Input Pins	C_{IN}	(Note 11)			10	pF
Capacitance on All Output Pins	C_{IO}	Outputs high impedance (Note 11)			10	pF

Pushbutton Reset Timing



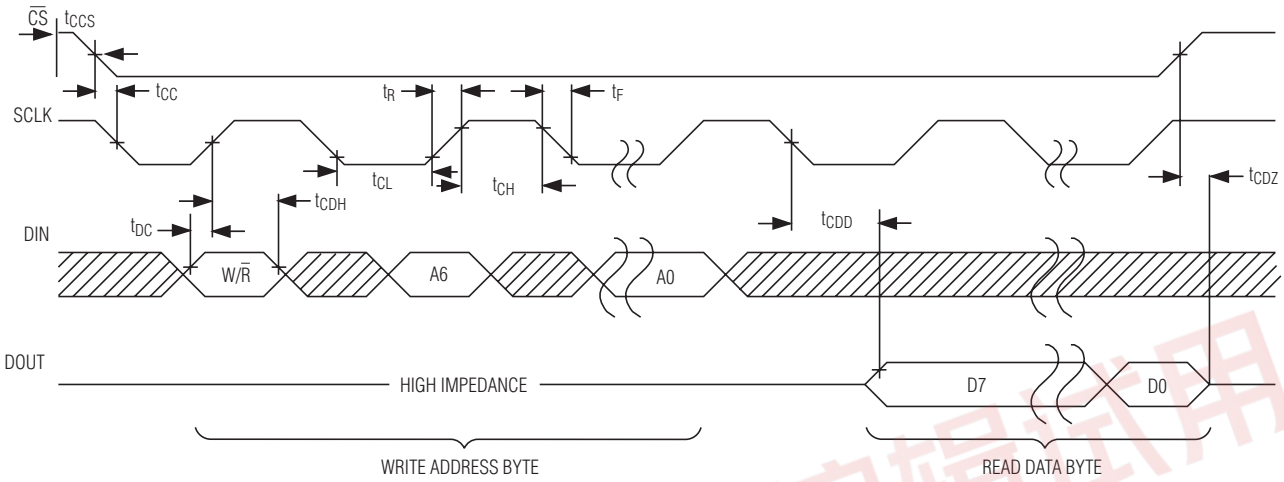
Power-Switch Timing



WARNING: Negative undershoots below -0.3V while the part is in battery-backed mode may cause loss of data.

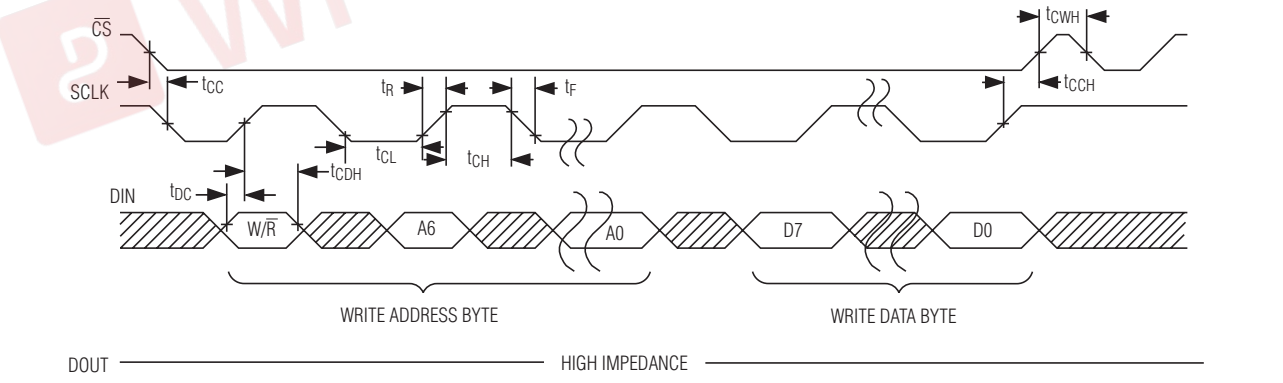
Note 2: Limits at -40°C are guaranteed by design and not production tested.
Note 3: All voltages are referenced to ground.
Note 4: Measured at V_{IH} = 0.8 x V_{CC} or V_{IL} = 0.2 x V_{CC}, 10ns rise/fall time, DOUT = no load.
Note 5: Current is the averaged input current, which includes the temperature conversion current. CRATE1 = CRATE0 = 0.
Note 6: The $\overline{RST}$ pin has an internal 50kΩ (nominal) pullup resistor to V_{CC}.
Note 7: Measured at V_{OH} = 0.8 x V_{CC} or V_{OL} = 0.2 x V_{CC}. Measured from the 50% point of SCLK to the V_{OH} minimum of DOUT.
Note 8: With 50pF load.
Note 9: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over the voltage range of 0V ≤ V_{CC} ≤ $V_{CC(MAX)}$ and 2.3V ≤ V_{BAT} ≤ $V_{BAT(MAX)}$.
Note 10: This delay only applies if the oscillator is enabled and running. If the $\overline{EOSC}$ bit is 1, t_{REC} is bypassed and $\overline{RST}$ immediately goes high.
Note 11: Guaranteed by design and not production tested.

Timing Diagram—SPI Read Transfer



NOTE: SCLK CAN BE EITHER POLARITY, SHOWN FOR CPOL = 1.

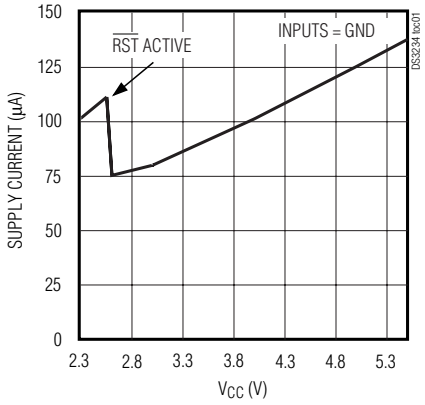
Timing Diagram—SPI Write Transfer



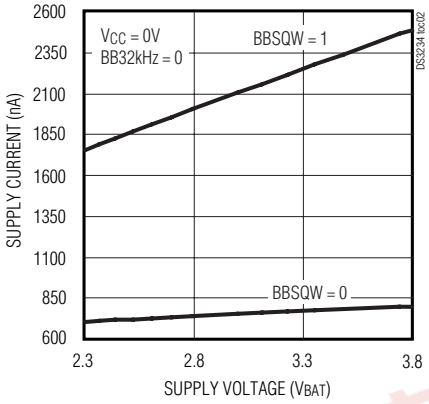
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

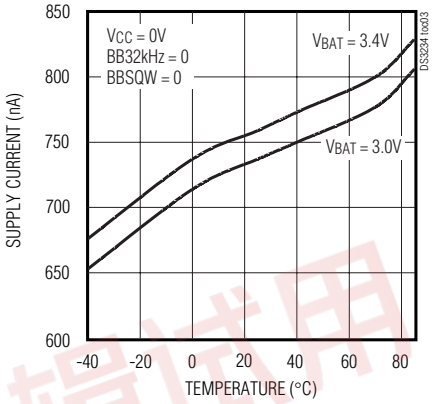
STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE



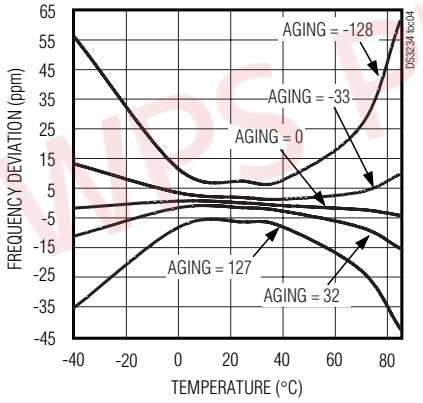
BATTERY CURRENT vs. SUPPLY VOLTAGE



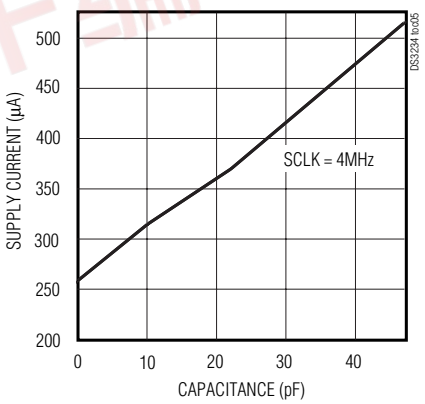
BATTERY CURRENT vs. TEMPERATURE



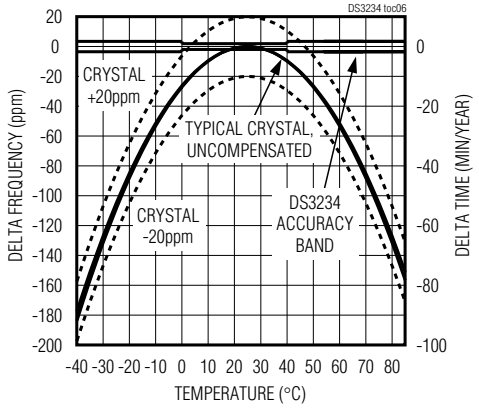
FREQUENCY DEVIATION vs. TEMPERATURE vs. AGING VALUE



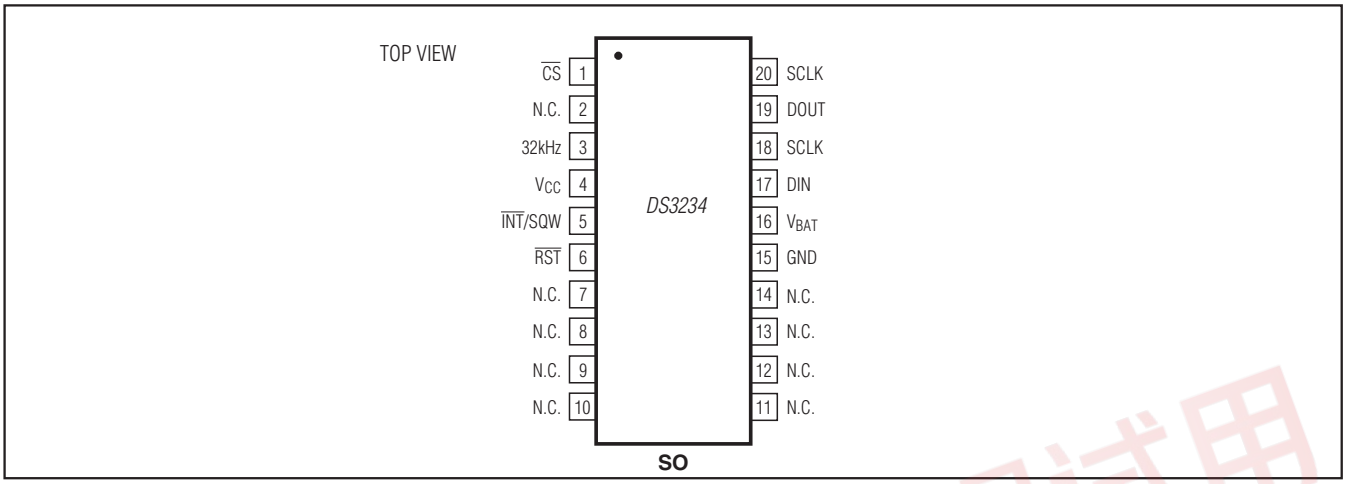
ICCA vs. DOUT LOAD



DELTA TIME AND FREQUENCY vs. TEMPERATURE



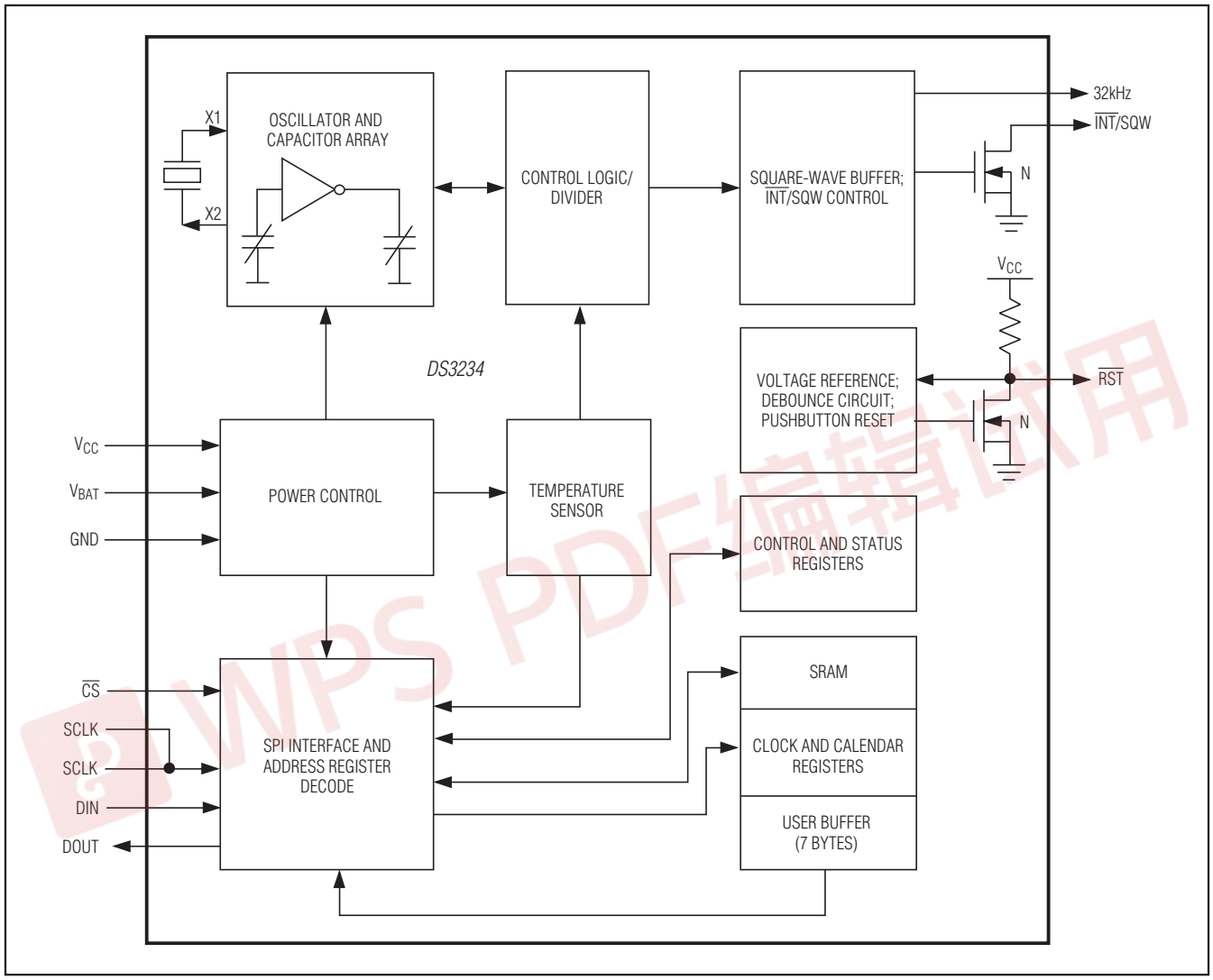
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	$\overline{CS}$	Active-Low Chip Select Input. Used to select or deselect the device.
2, 7–14	N.C.	No Connection. Not connected internally. Must be connected to ground.
3	32kHz	32kHz Push-Pull Output. If disabled with either EN32kHz = 0 or BB32kHz = 0, the state of the 32kHz pin will be low.
4	V_{CC}	DC Power Pin for Primary Power Supply. This pin should be decoupled using a 0.1µF to 1.0µF capacitor.
5	$\overline{INT}$/SQW	Active-Low Interrupt or Square-Wave Output. This open-drain pin requires an external pullup resistor. It can be left open if not used. This multifunction pin is determined by the state of the INTCN bit in the Control Register (0Eh). When INTCN is set to logic 0, this pin outputs a square wave and its frequency is determined by RS2 and RS1 bits. When INTCN is set to logic 1, then a match between the timekeeping registers and either of the alarm registers activates the $\overline{INT}$/SQW pin (if the alarm is enabled). Because the INTCN bit is set to logic 1 when power is first applied, the pin defaults to an interrupt output with alarms disabled. The pullup voltage can be up to 5.5V, regardless of the voltage on V_{CC}. If not used, this pin can be left unconnected.
6	$\overline{RST}$	Active-Low Reset. This pin is an open-drain input/output. It indicates the status of V_{CC} relative to the V_{PF} specification. As V_{CC} falls below V_{PF}, the $\overline{RST}$ pin is driven low. When V_{CC} exceeds V_{PF}, for t_{RST}, the $\overline{RST}$ pin is driven high impedance. The active-low, open-drain output is combined with a debounced pushbutton input function. This pin can be activated by a pushbutton reset request. It has an internal 50k_ nominal value pullup resistor to V_{CC}. No external pullup resistors should be connected. On first power-up, or if the crystal oscillator is disabled, t_{RST} is bypassed and $\overline{RST}$ immediately goes high.
15	GND	Ground
16	V_{BAT}	Backup Power-Supply Input. If V_{BAT} is not used, connect to ground. Diodes placed in series between the V_{BAT} pin and the battery can cause improper operation. UL recognized to ensure against reverse charging when used with a lithium battery. Go to **www.maximintegrated.com/qa/info/ul**.
17	DIN	SPI Data Input. Used to shift address and data into the device.
18, 20	SCLK	SPI Clock Input. Used to control timing of data into and out of the device. Either clock polarity can be used. The clock polarity is determined by the device based on the state of SCLK when $\overline{CS}$ goes low. Pins 18 and 20 are electrically connected together internally.
19	DOUT	SPI Data Output. Data is output on this pin when the device is in read mode; CMOS push-pull driver.

Block Diagram



Detailed Description

The DS3234 is a TCXO and RTC with integrated crystal and 256 bytes of SRAM. An integrated sensor periodically samples the temperature and adjusts the oscillator load to compensate for crystal drift caused by temperature variations. The DS3234 provides user-selectable sample rates. This allows the user to select a temperature sensor sample rate that allows for various temperature rates of change, while minimizing current consumption by temperature sensor sampling. The user should select a sample rate based upon the expected temperature rate of change, with faster sample rates for applications where the ambient temperature changes significantly over a short time. The TCXO provides a stable and accurate reference clock, and maintains the RTC to within ±2 minutes per year accuracy from -40°C to +85°C. The TCXO frequency output is available at the 32kHz pin. The RTC is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output. The INT/SQW provides either an interrupt signal due to alarm conditions or a square-wave output. The clock/calendar provides seconds, minutes, hours, day,

date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. Access to the internal registers is possible through an SPI bus interface.

A temperature-compensated voltage reference and comparator circuit monitors the level of V_{CC} to detect power failures and to automatically switch to the backup supply when necessary. When operating from the backup supply, access is inhibited to minimize supply current. Oscillator, time and date, and TCXO operations can continue while the backup supply powers the device. The $\overline{RST}$ pin provides an external pushbutton function and acts as an indicator of a power-fail event.

Operation

The block diagram shows the main elements of the DS3234. The eight blocks can be grouped into four functional groups: TCXO, power control, pushbutton function, and RTC. Their operations are described separately in the following sections.

32kHz TCXO

The temperature sensor, oscillator, and control logic form the TCXO. The controller reads the output of the on-chip temperature sensor and uses a lookup table to determine the capacitance required, adds the aging correction in the AGE register, and then sets the capacitance selection registers. New values, including changes to the AGE register, are loaded only when a change in the temperature value occurs. The temperature is read on initial application of V_{CC} and once every 64 seconds (default, see the description for CRATE1 and CRATE0 in the *Control/Status Register* section) afterwards.

Power Control

The power control function is provided by a temperature-compensated voltage reference and a comparator circuit that monitors the V_{CC} level. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below both V_{PF} and V_{BAT}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BAT}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BAT}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{BAT}. After V_{CC} returns above both V_{PF} and V_{BAT}, read and write access is allowed after $\overline{RST}$ goes high (Table 1).

To preserve the battery, the first time V_{BAT} is applied to the device, the oscillator does not start up until V_{CC} crosses V_{PF}. After the first time V_{CC} is ramped up, the oscillator starts up and the V_{BAT} source powers the oscillator during power-down and keeps the oscillator running. When the DS3234 switches to V_{BAT}, the oscillator may be disabled by setting the $\overline{EOSC}$ bit.

Table 1. Power Control

SUPPLY CONDITION	READ/WRITE ACCESS	ACTIVE SUPPLY	$\overline{RST}$
$V_{CC} < V_{PF}$, $V_{CC} < V_{BAT}$	No	V_{BAT}	Active
$V_{CC} < V_{PF}$, $V_{CC} > V_{BAT}$	Yes	V_{CC}	Active
$V_{CC} > V_{PF}$, $V_{CC} < V_{BAT}$	Yes	V_{CC}	Inactive
$V_{CC} > V_{PF}$, $V_{CC} > V_{BAT}$	Yes	V_{CC}	Inactive

V_{BAT} Operation

There are several modes of operation that affect the amount of V_{BAT} current that is drawn. When the part is powered by V_{BAT}, timekeeping current (I_{BATT}), which includes the averaged temperature conversion current, I_{BATTC}, is drawn (refer to Application Note 3644: *Power Considerations for Accurate Real-Time Clocks* for details). Temperature conversion current, I_{BATTC}, is specified since the system must be able to support the periodic higher current pulse and still maintain a valid voltage level. Data retention current, I_{BATTDR}, is the current drawn by the part when the oscillator is stopped ($\overline{EOSC}$ = 1). This mode can be used to minimize battery requirements for times when maintaining time and date information is not necessary, e.g., while the end system is waiting to be shipped to a customer.

Pushbutton Reset Function

The DS3234 provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS3234 is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low going edge. If an edge transition is detected, the DS3234 debounces the switch by pulling the $\overline{RST}$ low. After the internal timer has expired (PB_{DB}), the DS3234 continues to monitor the $\overline{RST}$ line. If the line is still low, the DS3234 continuously monitors the line looking for a rising edge. Upon detecting release, the DS3234 forces the $\overline{RST}$ pin low and holds it low for t_{RST}.

The same pin, $\overline{RST}$, is used to indicate a power-fail condition. When V_{CC} is lower than V_{PF}, an internal power-fail signal is generated, which forces the $\overline{RST}$ pin low. When V_{CC} returns to a level above V_{PF}, the $\overline{RST}$ pin is held low for t_{REC} to allow the power supply to stabilize. If the $\overline{EOSC}$ bit is set to logic 1 (to disable the oscillator in battery-backup mode), t_{REC} is bypassed and $\overline{RST}$ immediately goes high.

When $\overline{RST}$ is active due to a power-fail condition (see Table 1), SPI operations are inhibited while the TCXO and RTC continue to operate. When $\overline{RST}$ is active due to a pushbutton event, it does not affect the operation of the TCXO, SPI interface, or RTC functions.

Real-Time Clock

With the clock source from the TCXO, the RTC provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an $\overline{AM}$/PM indicator.

The clock provides two programmable time-of-day alarms and a programmable square-wave output. The $\overline{INT}$/SQW pin either generates an interrupt due to alarm condition or outputs a square-wave signal and the selection is controlled by the bit INTCN.

SRAM

The DS3234 provides 256 bytes of general-purpose battery-backed read/write memory. The SRAM can be written or read whenever V_{CC} is above either V_{PF} or V_{BAT}.

Address Map

Figure 1 shows the address map for the DS3234 timekeeping registers. During a multibyte access, when the address pointer reaches the end of the register space (13h read, 93h write), it wraps around to the beginning (00h read, 80h write). The DS3234 does not respond to a read or write to any reserved address, and the internal address pointer does not increment. Address pointer operation when accessing the 256-byte SRAM data is covered in the description of the SRAM address and data registers. On the falling edge of $\overline{CS}$, or during a multibyte access when the address pointer increments to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the internal clock registers continue to increment normally. If the time and date registers are read using a multibyte read, this eliminates the need to reread the registers in case the main registers update during a read.

SPI Interface

The DS3234 operates as a slave device on the SPI serial bus. Access is obtained by selecting the part by the $\overline{CS}$ pin and clocking data into/out of the part using the SCLK and DIN/DOUT pins. Multiple byte transfers are supported within one $\overline{CS}$ low period. The SPI on the DS3234 interface is accessible whenever V_{CC} is above either V_{BAT} or V_{PF}.

Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. Figure 1 illustrates the RTC registers. The time and calendar data are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in binary-coded decimal (BCD) format. The DS3234 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode select bit. When high, 12-hour mode is selected. In 12-hour mode, bit 5 is the $\overline{AM}$/PM bit with logic-high being PM. In 24-hour mode, bit 5 is the 20-hour bit (20–23 hours). The century bit (bit 7 of the month register) is toggled when the years register overflows from 99 to 00.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on the falling edge of $\overline{CS}$ or and when the register pointer rolls over to zero. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read.

The countdown chain is reset whenever the seconds register is written. Write transfers occur when the last bit of a byte is clocked in. Once the countdown chain is reset, to avoid rollover issues the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enabled, transitions high 500ms after the seconds data transfer.

Figure 1. Address Map for DS3234 Timekeeping Registers and SRAM

ADDRESS READ/WRITE		MSB BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0	FUNCTION	RANGE
00h	80h	0	10 Seconds			Seconds				Seconds	00–59
01h	81h	0	10 Minutes			Minutes				Minutes	00–59
02h	82h	0	12/$\overline{24}$	$\overline{AM}$/PM 20 hr	10 hr	Hour				Hours	1-12 +$\overline{AM}$ /PM 00-23
03h	83h	0	0	0	0	0	Day			Day	1-7
04h	84h	0	0	10 Date		Date				Date	01-31
05h	85h	Century	0	0	10 Mo	Month				Month/ Century	01-12 + Century
06h	86h	10 Year				Year				Year	00-99
07h	87h	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00-59
08h	88h	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00-59
09h	89h	A1M3	12/$\overline{24}$	$\overline{AM}$/PM 20 hr	10 hr	Hour				Alarm 1 Hours	1-12 +$\overline{AM}$ /PM 00-23
0Ah	8Ah	A1M4	DY/$\overline{DT}$	0 10 Date		Day Date				Alarm 1 Day Alarm 1 Date	1-7 01-31
0Bh	8Bh	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00-59
0Ch	8Ch	A2M3	12/$\overline{24}$	$\overline{AM}$/PM 20 hr	10 hr	Hour				Alarm 2 Hours	1-12 +$\overline{AM}$ /PM 00-23
0Dh	8Dh	A2M4	DY/$\overline{DT}$	0 10 Date		Day Date				Alarm 2 Day Alarm 2 Date	1-7 01-31
0Eh	8Eh	$\overline{EOSC}$	BBSQW	CONV	RS2	RS1	INTCN	A2IE	A1IE	Control	—
0Fh	8Fh	OSF	BB32kHz	CRATE1	CRATE0	EN32kHz	BSY	A2F	A1F	Control/ Status	—
10h	90h	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA	Crystal Aging Offset	—
11h	91h	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA	Temp MSB	Read Only
12h	92h	DATA	DATA	0	0	0	0	0	0	Temp LSB	Read Only
13h	93h	0	0	0	0	0	0	0	BB_TD	Disable Temp Conversions	—
14h–17h	94h–97h	—	—	—	—	—	—	—	—	Reserved	—
18h	98h	A7	A6	A5	A4	A3	A2	A1	A0	SRAM Address	—
19h	99h	D7	D6	D5	D4	D3	D2	D1	D0	SRAM Data	—

Note: *Unless otherwise specified, the registers' state is not defined when power is first applied. Bits defined as 0 cannot be written to 1 and will always read 0.*

Alarms

The DS3234 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh. The alarms can be programmed (by the alarm enable and INTCN bits of the control register) to activate the $\overline{INT}$/SQW output on an alarm match condition. Bit 7 of each of the time-of-day/date alarm registers are mask bits (Table 2). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 2 shows the possible settings. Configurations not listed in the table will result in illogical operations.

The DY/$\overline{DT}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/$\overline{DT}$ is written to logic 0, the alarm will be the result of a match with date of the month. If DY/$\overline{DT}$ is written to logic 1, the alarm will be the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding Alarm Flag 'A1F' or 'A2F' bit is set to logic 1. If the corresponding Alarm Interrupt Enable 'A1IE' or 'A2IE' is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition activates the $\overline{INT}$/SQW signal. The match is tested on the once-per-second update of the time and date registers.

Table 2. Alarm Mask Bits

DY/$\overline{DT}$	ALARM 1 REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/$\overline{DT}$	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 seconds of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

Control Register (0Eh/8Eh)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	$\overline{EOSC}$	BBSQW	CONV	RS2	RS1	INTCN	A2IE	A1IE
POR*:	0	0	0	1	1	1	0	0

**POR is defined as the first application of power to the device, either V_{BAT} or V_{CC}.*

Special-Purpose Registers

The DS3234 has two additional registers (control and control/status) that control the real-time clock, alarms, and square-wave output.

Control Register (0Eh/8Eh)

Bit 7: Enable Oscillator ($\overline{EOSC}$). When set to logic 0, the oscillator is started. When set to logic 1, the oscillator is stopped when the DS3234 switches to battery power. This bit is clear (logic 0) when power is first applied. When the DS3234 is powered by V_{CC}, the oscillator is always on regardless of the status of the $\overline{EOSC}$ bit. When $\overline{EOSC}$ is disabled, all register data is static.

Bit 6: Battery-Backed Square-Wave Enable (BBSQW). When set to logic 1 with INTCN = 0 and V_{CC} < V_{PF}, this bit enables the square wave. When BBSQW is logic 0, the $\overline{INT}$/SQW pin goes high impedance when V_{CC} < V_{PF}. This bit is disabled (logic 0) when power is first applied.

Bit 5: Convert Temperature (CONV). Setting this bit to 1 forces the temperature sensor to convert the temperature into digital code and execute the TCXO algorithm to update the capacitance array to the oscillator. This can only happen when a conversion is not already in progress. The user should check the status bit BSY before forcing the controller to start a new TCXO execution. A user-initiated temperature conversion does not affect the internal 64-second (default interval) update cycle. This bit is disabled (logic 0) when power is first applied.

A user-initiated temperature conversion does not affect the BSY bit for approximately 2ms. The CONV bit remains at a 1 from the time it is written until the conversion is finished, at which time both CONV and BSY go to 0. The CONV bit should be used when monitoring the status of a user-initiated conversion.

Bits 4 and 3: Rate Select (RS2 and RS1). These bits control the frequency of the square-wave output when the square wave has been enabled. The following table shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (8.192kHz) when power is first applied.

SQUARE-WAVE OUTPUT FREQUENCY

RS2	RS1	SQUARE-WAVE OUTPUT FREQUENCY
0	0	1Hz
0	1	1.024kHz
1	0	4.096kHz
1	1	8.192kHz

Bit 2: Interrupt Control (INTCN). This bit controls the $\overline{INT}$/SQW signal. When the INTCN bit is set to logic 0, a square wave is output on the $\overline{INT}$/SQW pin. When the INTCN bit is set to logic 1, a match between the timekeeping registers and either of the alarm registers activates the $\overline{INT}$/SQW (if the alarm is also enabled). The corresponding alarm flag is always set regardless of the state of the INTCN bit. The INTCN bit is set to logic 1 when power is first applied.

Bit 1: Alarm 2 Interrupt Enable (A2IE). When set to logic 1, this bit permits the alarm 2 flag (A2F) bit in the status register to assert $\overline{INT}$/SQW (when INTCN = 1). When the A2IE bit is set to logic 0 or INTCN is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Bit 0: Alarm 1 Interrupt Enable (A1IE). When set to logic 1, this bit permits the alarm 1 flag (A1F) bit in the status register to assert $\overline{INT}$/SQW (when INTCN = 1). When the A1IE bit is set to logic 0 or INTCN is set to logic 0, the A1F bit does not initiate the $\overline{INT}$/SQW signal. The A1IE bit is disabled (logic 0) when power is first applied.

Control/Status Register (0Fh/8Fh)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	OSF	BB32kHz	CRATE1	CRATE0	EN32kHz	BSY	A2F	A1F
POR*:	1	1	0	0	1	0	0	0

**POR is defined as the first application of power to the device, either V_{BAT} or V_{CC}.*

Control/Status Register (0Fh/8Fh)

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period and may be used to judge the validity of the timekeeping data. This bit is set to logic 1 any time that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltages present on both V_{CC} and V_{BAT} are insufficient to support oscillation.
3) The $\overline{EOSC}$ bit is turned off in battery-backed mode.
4) External influences on the crystal (i.e., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.

Bit 6: Battery-Backed 32kHz Output (BB32kHz). This bit enables the 32kHz output when powered from V_{BAT} (provided EN32kHz is enabled). If BB32kHz = 0, the 32kHz output is low when the part is powered by V_{BAT}. This bit is enabled (logic 1) when power is first applied.

Bits 5 and 4: Conversion Rate (CRATE1 and CRATE0). These two bits control the sample rate of the TCXO. The sample rate determines how often the temperature sensor makes a conversion and applies compensation to the oscillator. Decreasing the sample rate decreases the overall power consumption by decreasing the frequency at which the temperature sensor operates. However, significant temperature changes that occur between samples may not be completely compensated for, which reduce overall accuracy. These bits are set to logic 0 when power is first applied.

CRATE1	CRATE0	SAMPLE RATE (seconds)
0	0	64
0	1	128
1	0	256
1	1	512

Bit 3: Enable 32kHz Output (EN32kHz). This bit indicates the status of the 32kHz pin. When set to logic 1, the 32kHz pin is enabled and outputs a 32.768kHz square-wave signal. When set to logic 0, the 32kHz pin is low. The initial power-up state of this bit is logic 1, and a 32.768kHz square-wave signal appears at the 32kHz pin after a power source is applied to the DS3234. This bit is enabled (logic 1) when power is first applied.

Bit 2: Busy (BSY). This bit indicates the device is busy executing TCXO functions. It goes to logic 1 when the conversion signal to the temperature sensor is asserted and then is cleared when the conversion is complete.

Bit 1: Alarm 2 Flag (A2F). A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. If the A2IE bit and INTCN bit are set to logic 1, the $\overline{INT}$/SQW pin is driven low while A2F is active. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Bit 0: Alarm 1 Flag (A1F). A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit and the INTCN bit are set to logic 1, the $\overline{INT}$/SQW pin is driven low while A1F is active. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Aging Offset (10h/90h)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA
POR*:	0	0	0	0	0	0	0	0

Temperature Register (MSB) (11h)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA
POR*:	0	0	0	0	0	0	0	0

Temperature Register (LSB) (12h)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	DATA	DATA	0	0	0	0	0	0
POR*:	0	0	0	0	0	0	0	0

**POR is defined as the first application of power to the device, either V_{BAT} or V_{CC}.*

Aging Offset Register (10h/90h)

The aging offset register takes a user-provided value to add to or subtract from the oscillator capacitor array. The data is encoded in two's complement, with bit 7 representing the SIGN bit. One LSB represents the smallest capacitor to be switched in or out of the capacitance array at the crystal pins. The aging offset register capacitance value is added or subtracted from the capacitance value that the device calculates for each temperature compensation. The offset register is added to the capacitance array during a normal temperature conversion, if the temperature changes from the previous conversion, or during a manual user conversion (setting the CONV bit). To see the effects of the aging register on the 32kHz output frequency immediately, a manual conversion should be performed after each aging offset register change.

Positive aging values add capacitance to the array, slowing the oscillator frequency. Negative values remove capacitance from the array, increasing the oscillator frequency.

The change in ppm per LSB is different at different temperatures. The frequency vs. temperature curve is shifted by the values used in this register. At +25°C, one LSB typically provides about 0.1ppm change in frequency. These bits are all set to logic 0 when power is first applied.

Use of the aging register is not needed to achieve the accuracy as defined in the EC tables, but could be used to help compensate for aging at a given temperature. See the *Typical Operating Characteristics* section for a graph showing the effect of the register on accuracy over temperature.

Temperature Registers (11h–12h)

Temperature is represented as a 10-bit code with a resolution of 0.25°C and is accessible at location 11h and 12h. The temperature is encoded in two's complement format, with bit 7 in the MSB representing the SIGN bit. The upper 8 bits, the integer portion, are at location 11h and the lower 2 bits, the fractional portion, are in the upper nibble at location 12h. Example: 00011001 01b = +25.25°C. Upon power reset, the registers are set to a default temperature of 0°C and the controller starts a temperature conversion.

The temperature is read on initial application of V_{CC} and once every 64 seconds afterwards. The temperature registers are updated after each user-initiated conversion and on every 64-second conversion. The temperature registers are read-only.

Temperature Control (13h/93h)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	0	0	0	0	0	0	0	BB_TD
POR*:	0	0	0	0	0	0	0	0

**POR is defined as the first application of power to the device, either V_{BAT} or V_{CC}.*

SRAM Address (18h/98h)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	A7	A6	A5	A4	A2	A1	A1	A0

SRAM Data (19h/99h)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	D7	D6	D5	D4	D2	D1	D1	D0

Note: *These registers do not default to any specific value.*

Temperature Control Register (13h/93h)

Bit 0: Battery-Backed Temperature Conversion Disable (BB_TD). The battery-backed tempconv disable bit prevents automatic temperature conversions when the device is powered by the V_{BAT} supply. This reduces the battery current at the expense of frequency accuracy.

SRAM Address Register (18h/98h)

The SRAM address register provides the 8-bit address of the 256-byte memory array. The desired memory address should be written to this register before the data register is accessed. The contents of this register are incremented automatically if the data register is accessed more than once during a single transfer. When the contents of the address register reach 0FFh, the next access causes the register to roll over to 00h.

SRAM Data Register (19h/99h)

The SRAM data register provides the data to be written to or the data read from the 256-byte memory array. During a read cycle, the data in this register is that found in the memory location in the SRAM address register (18h/98h). During a write cycle, the data in this register is placed in the memory location in the SRAM address register (18h/98h). When the SRAM data register is read or written, the internal register pointer remains at 19h/99h and the SRAM address register increments after each byte that is read or written, allowing multibyte transfers.

SPI Serial Data Bus

The DS3234 provides a 4-wire SPI serial data bus to communicate in systems with an SPI host controller. The DS3234 supports both single byte and multiple byte data transfers for maximum flexibility. The DIN and DOUT pins are the serial data input and output pins, respectively. The $\overline{CS}$ input is used to initiate and terminate a data transfer. The SCLK pin is used to synchronize data movement between the master (microcontroller) and the slave devices (see Table 3). The shift clock (SCLK), which is generated by the microcontroller, is active only during address and data transfer to any device on the SPI bus. Input data (DIN) is latched on the internal strobe edge and output data (DOUT) is shifted out on the shift edge (Figure 2). There is one clock for each bit transferred. Address and data bits are transferred in groups of eight.

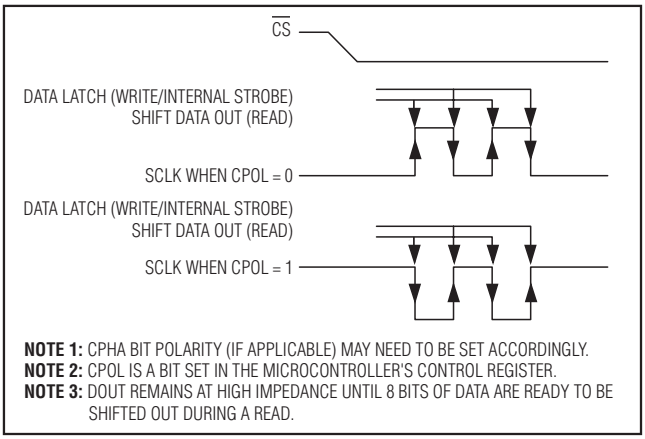


Figure 2. Serial Clock as a Function of Microcontroller Clock-Polarity Bit

Address and data bytes are shifted MSB first into the serial data input (DIN) and out of the serial data output (DOUT). Any transfer requires the address of the byte to specify a write or read, followed by one or more bytes of data. Data is transferred out of the DOUT pin for a read operation and into the DIN for a write operation (Figures 3 and 4).

The address byte is always the first byte entered after $\overline{CS}$ is driven low. The most significant bit of this byte determines if a read or write takes place. If the MSB is 0, one or more read cycles occur. If the MSB is 1, one or more write cycles occur.

Table 3. SPI Pin Function

MODE	$\overline{CS}$	SCLK	DIN	DOUT
Disable	H	Input Disabled	Input Disabled	High Impedance
Write	L	*CPOL = 1, SCLK Rising	Data Bit Latch	High Impedance
		CPOL = 0, SCLK Falling		
Read	L	CPOL = 1, SCLK Falling	X	Next Data Bit Shift**
		CPOL = 0, SCLK Rising		
Read Invalid Location	L	Don't Care	Don't Care	High Impedance

**CPOL is the clock-polarity bit set in the control register of the host microprocessor.*

***DOUT remains at high impedance until 8 bits of data are ready to be shifted out during a read.*

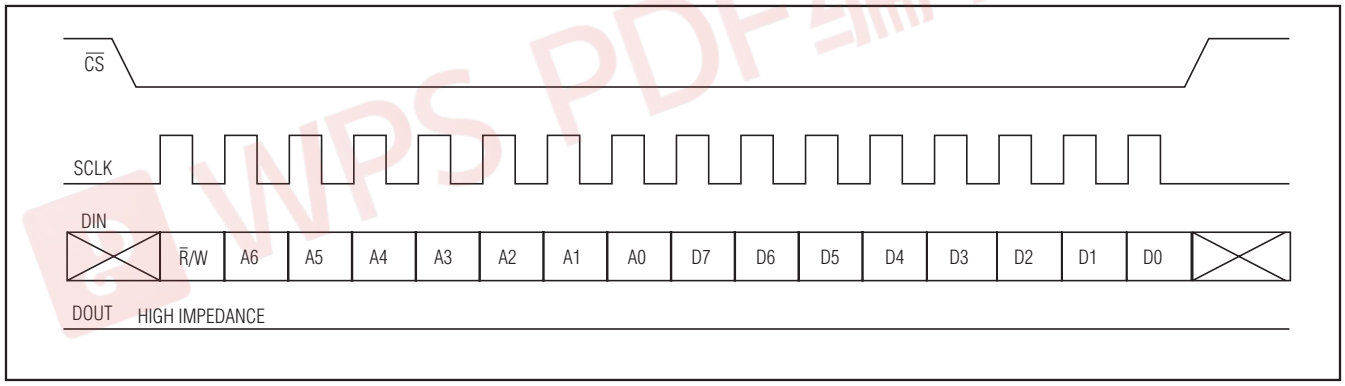


Figure 3. SPI Single-Byte Write

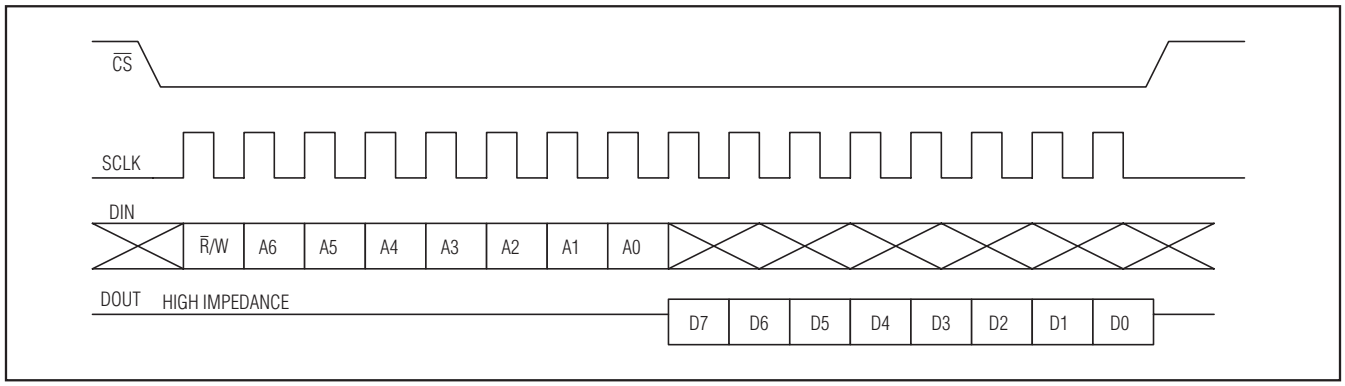


Figure 4. SPI Single-Byte Read

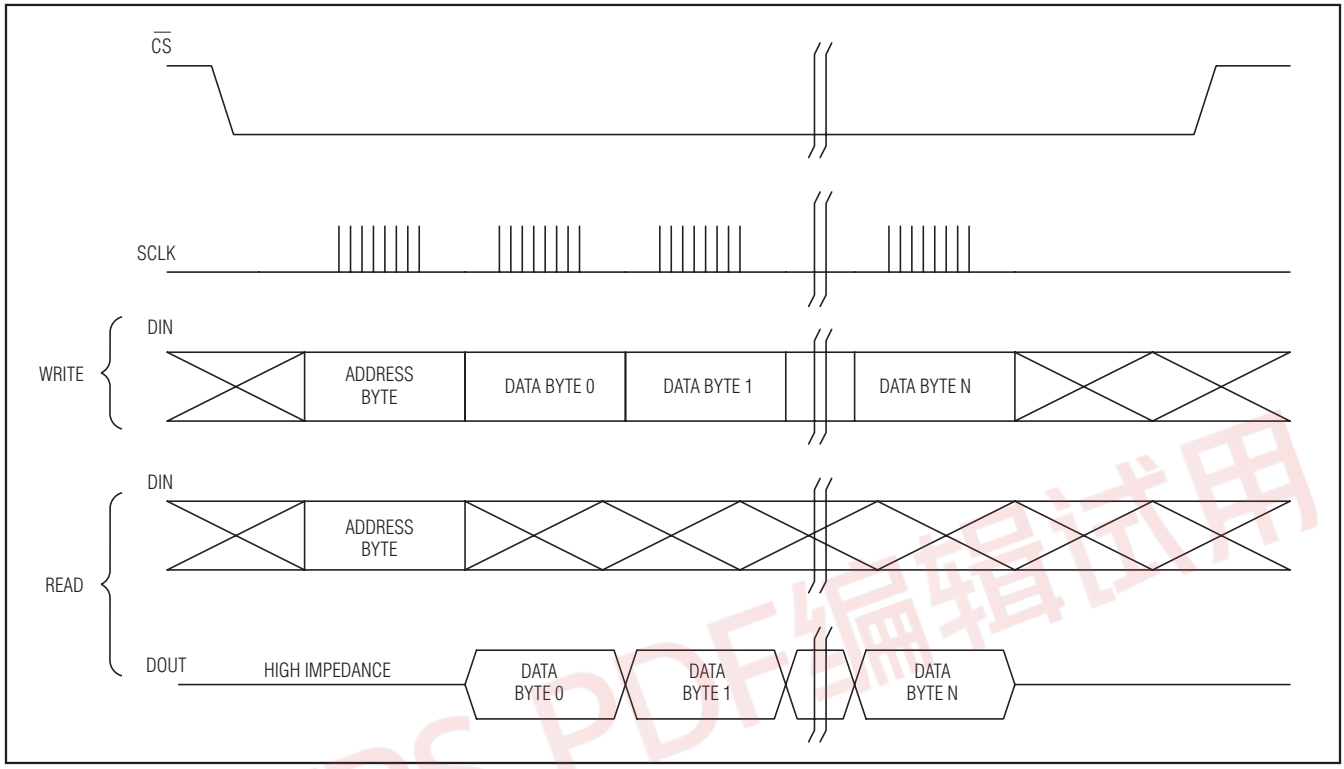


Figure 5. SPI Multiple-Byte Burst Transfer

Data transfers can occur one byte at a time or in multiple-byte burst mode. After $\overline{CS}$ is driven low, an address is written to the DS3234. After the address, one or more data bytes can be written or read. For a single-byte transfer, one byte is read or written and then $\overline{CS}$ is driven high. For a multiple-byte transfer, however, multiple bytes can be read or written after the address has been written (Figure 5). Each read or write cycle causes the RTC register address to automatically increment, which continues until the device is disabled. The address wraps to 00h after incrementing to 13h (during a read) and wraps to 80h after incrementing to 93h (during a write). An updated copy of the time is loaded into the user buffers upon the falling edge of $\overline{CS}$ and each time the address pointer increments from 13h to 00h. Because the internal and user copies of the time are only synchronized on these two events, an alarm condition can occur internally and activate the $\overline{INT}$/SQW pin independently of the user data.

If the SRAM is accessed by reading (address 19h) or writing (address 99h) the SRAM data register, the contents of the SRAM address register are automatically incremented after the first access, and all data cycles will use the SRAM data register.

Handling, PC Board Layout, and Assembly

The DS3234 package contains a quartz tuning-fork crystal. Pick-and-place equipment can be used, but precautions should be taken to ensure that excessive shock and vibration are avoided. Exposure to reflow is limited to 2 times maximum. Ultrasonic cleaning should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All N.C. (no connect) pins must be connected to ground.

Chip Information

SUBSTRATE CONNECTED TO GROUND

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 SO	W20#H2	**21-0042**	**90-0108**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/06	Initial release	—
1	7/07	Clarified the behavior of t_{REC} on initial power-up in the $\overline{RST}$ description of the *Pin Description*	8
		Corrected the POR for the BB32kHz bit from 0 to 1	15
2	10/08	Updated the *Typical Operating Circuit*	1
		Removed the V_{PU} parameter from the *Recommended DC Operating Conditions* table and added verbiage about the pullup to the *Pin Description* table for $\overline{INT}$/SQW	2, 8
		In the *Electrical Characteristics* table, added CRATE1 = CRATE0 = 0 to the I_{BATT} parameter and changed the symbols for Timekeeping Battery Current, Temperature Conversion Current, and Data-Retention Current from I_{BAT}, I_{TC}, and I_{BATTC} to I_{BATT}, I_{BATTC}, and I_{BATTDR}, respectively	3
		In the *AC Electrical Characteristics*, changed the t_{CWH} specification from 400ns (max) to 400ns (min)	4
		Added the Delta Time and Frequency vs. Temperature graph in the *Typical Operating Characteristics* section	7
		Updated the *Block Diagram*	9
		Added the V_{BAT} *Operation* section, improved some sections of text for the *Pushbutton Reset Function, Aging Offset Register (10h/90h)*, and *Temperature Registers (11h–12h)* sections	10, 16
		Corrected the description of when the countdown chain is reset in the *Clock and Calendar* section	11
3	7/10	In the *Absolute Maximum Ratings* section, added the theta-JA and theta-JC thermal resistances and Note 1, and changed the soldering temperature to +260°C; changed the 10-hour bit to 20-hour bit in the *Clock and Calendar* section and Table 1; updated the BBSQW bit description in the *Control Register (0Eh/8Eh)* section; added the land pattern no. to the *Package Information* table	2–5, 8, 11, 12, 14, 20
4	3/15	Updated *Benefits and Features* section	1

GigaDevice Semiconductor Inc.

GD32F307xx
ARM® Cortex®-M4 32-bit MCU

Datasheet

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1. General description

The GD32F307xx device belongs to the mainstream line of GD32 MCU Family. It is a new 32-bit general-purpose microcontroller based on the ARM® Cortex®-M4 RISC core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Cortex®-M4 core features implements a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32F307xx device incorporates the ARM® Cortex®-M4 32-bit processor core operating at 120 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 1024 KB on-chip Flash memory and 96 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to two 12-bit 2.6 MSPS ADCs, two 12-bit DACs, up to ten general 16-bit timers, two 16-bit PWM advanced timers, and two 16-bit basic timers, as well as standard and advanced communication interfaces: up to three SPIs, two I2Cs, three USARTs and two UARTs, two I2Ss, two CANs, a USBFS and an ENET.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make GD32F307xx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, communication networks, embedded modules, human machine interface, security and alarm systems, graphic display, automotive navigation, IoT and so on.

2. Device overview

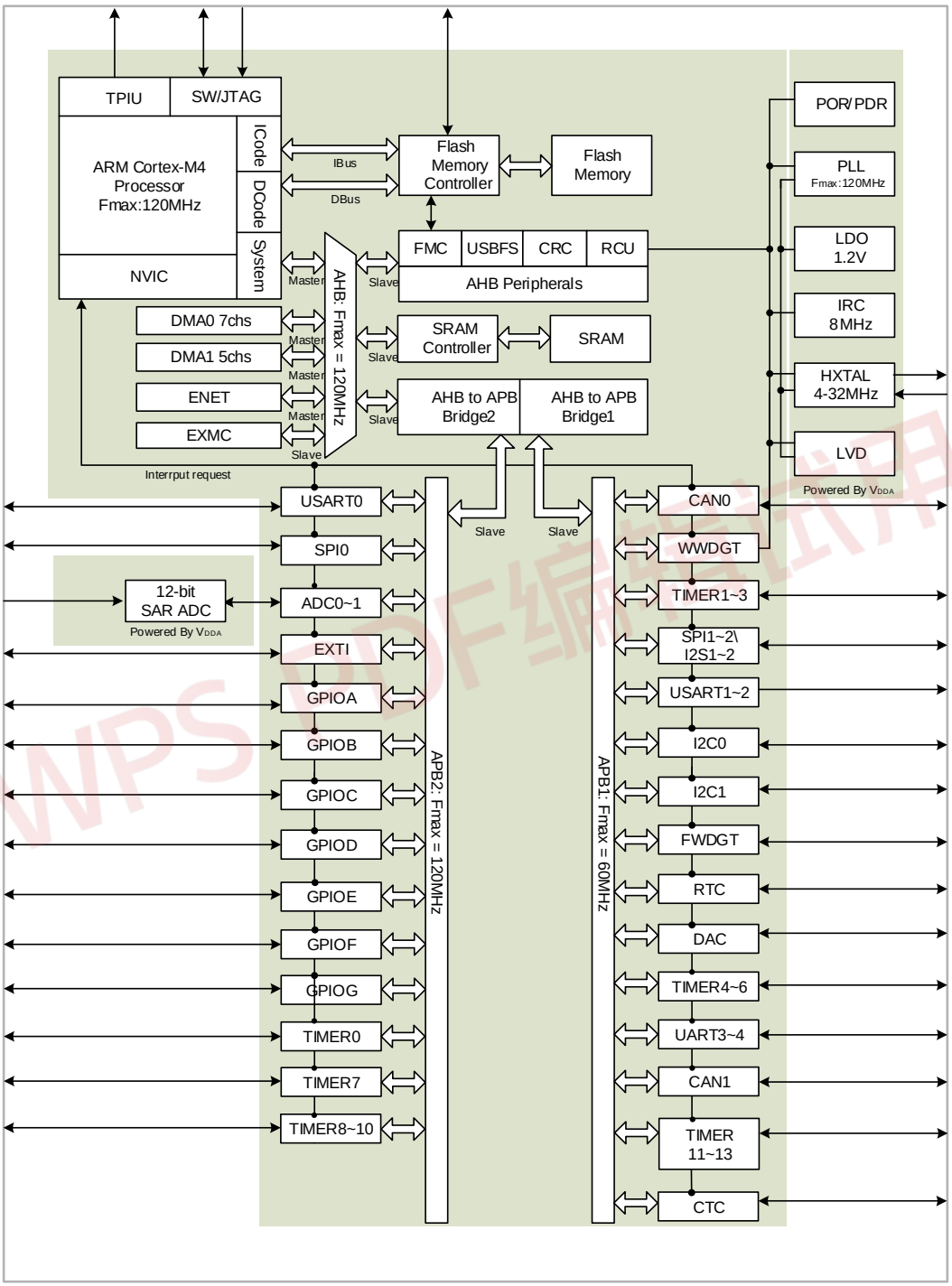
2.1. Device information

Table 2-1. GD32F307xx devices features and peripheral list

Part Number		GD32F307xx								
		RC	RE	RG	VC	VE	VG	ZC	ZE	ZG
Flash	Code area (KB)	256	256	256	256	256	256	256	256	256
	Data area (KB)	0	256	768	0	256	768	0	256	768
	Total (KB)	256	512	1024	256	512	1024	256	512	1024
SRAM (KB)		96	96	96	96	96	96	96	96	96
Timers	General timer(16-bit)	4 (1-4)	4 (1-4)	10 (1-4,8-13)	4 (1-4)	4 (1-4)	10 (1-4,8-13)	4 (1-4)	4 (1-4)	10 (1-4,8-13)
	Advanced timer(16-bit)	1 (0)	2 (0,7)	2 (0,7)	1 (0)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)
	Basic timer(16-bit)	2 (5-6)	2 (5-6)	2 (5-6)	2 (5-6)	2 (5-6)	2 (5-6)	2 (5-6)	2 (5-6)	2 (5-6)
	SysTick	1	1	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1
Connectivity	USART	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)
	UART	2 (3-4)	2 (3-4)	2 (3-4)	2 (3-4)	2 (3-4)	2 (3-4)	2 (3-4)	2 (3-4)	2 (3-4)
	I2C	2	2	2	2	2	2	2	2	2
	SPI/I2S	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)
	ENET	1	1	1	1	1	1	1	1	1
	CAN	2	2	2	2	2	2	2	2	2
	USBFS	1	1	1	1	1	1	1	1	1
GPIO		51	51	51	80	80	80	112	112	112
EXMC		0	0	0	1	1	1	1	1	1
EXTI		16	16	16	16	16	16	16	16	16
ADC Unit (CHs)		2(16)	2(16)	2(16)	2(16)	2(16)	2(16)	2(21)	2(21)	2(21)
DAC		2	2	2	2	2	2	2	2	2
Package		LQFP64			LQFP100			LQFP144		

2.2. Block diagram

Figure 2-1 GD32F307xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2 GD32F307Zx LQFP144 pinouts

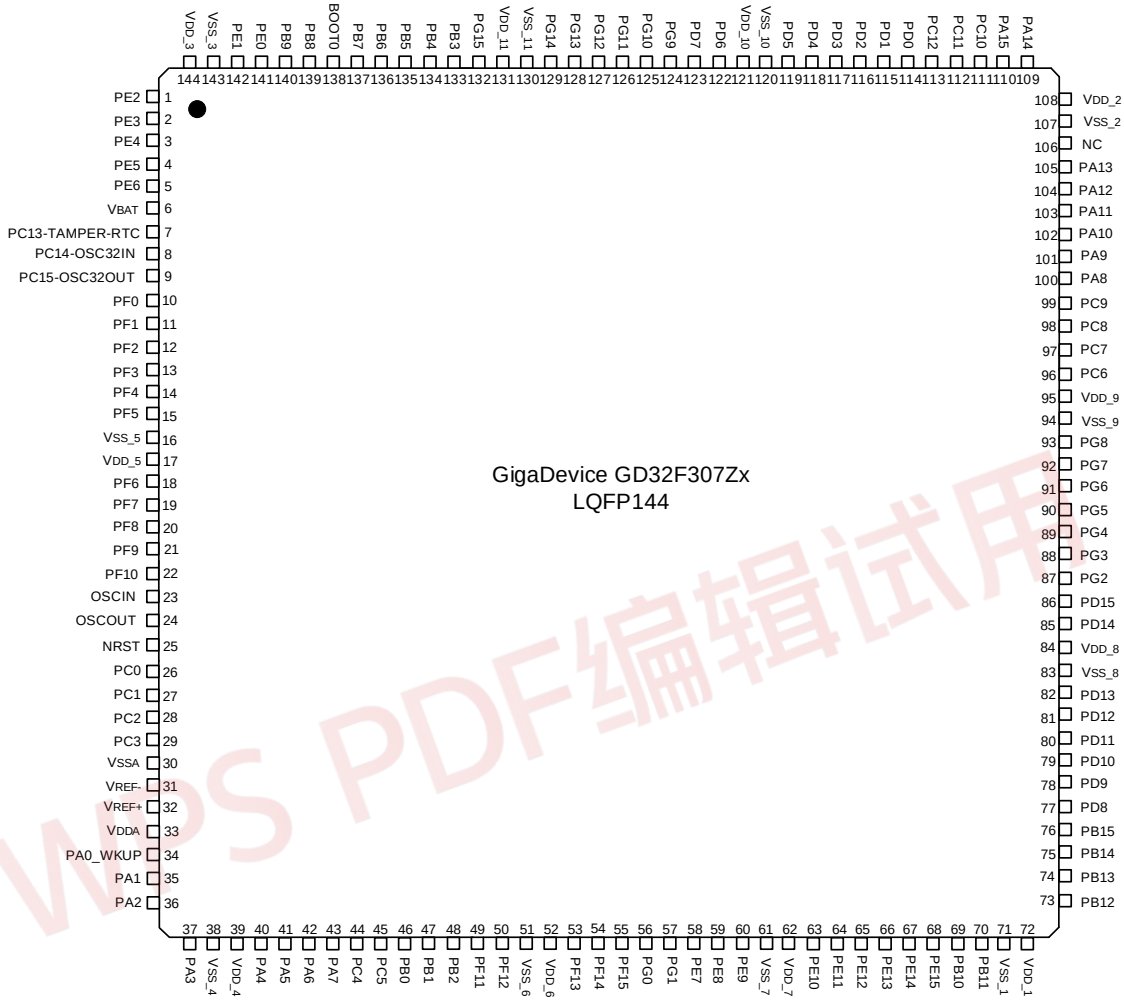


Figure 2-3 GD32F307Vx LQFP100 pinouts

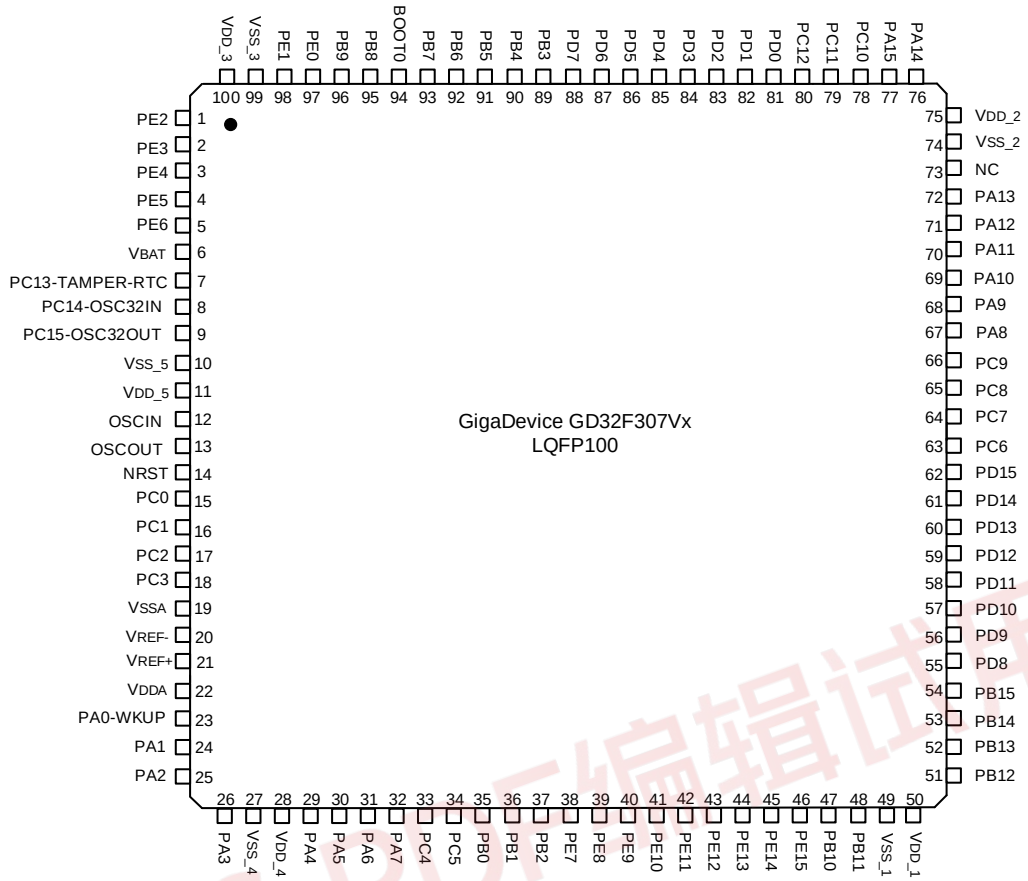
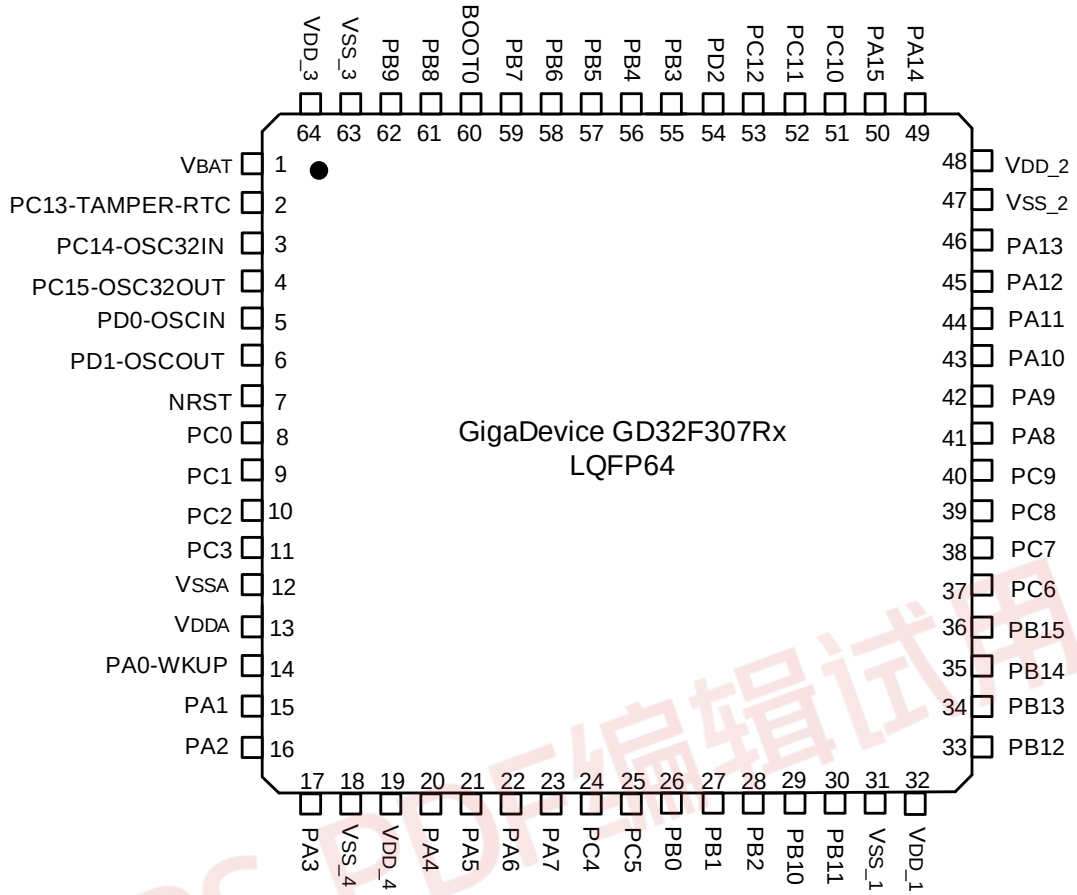


Figure 2-4 GD32F307Rx LQFP64 pinouts



2.4. Memory map

Table 2-2. GD32F307xx memory map

Pre-defined Regions	Bus	Address	Peripherals
External device	AHB3	0xA000 0000 - 0xA000 0FFF	EXMC - SWREG
External RAM		0x9000 0000 - 0x9FFF FFFF	EXMC - PC CARD
		0x7000 0000 - 0x8FFF FFFF	EXMC - NAND
		0x6000 0000 - 0x6FFF FFFF	EXMC - NOR/PSRAM/SRAM
Peripheral	AHB1	0x5000 0000 - 0x5003 FFFF	USBFS
		0x4008 0000 - 0x4FFF FFFF	Reserved
		0x4004 0000 - 0x4007 FFFF	Reserved
		0x4002 BC00 - 0x4003 FFFF	Reserved
		0x4002 B000 - 0x4002 BBFF	Reserved
		0x4002 A000 - 0x4002 AFFF	Reserved
		0x4002 8000 - 0x4002 9FFF	ENET
		0x4002 6800 - 0x4002 7FFF	Reserved
		0x4002 6400 - 0x4002 67FF	Reserved
		0x4002 6000 - 0x4002 63FF	Reserved
		0x4002 5000 - 0x4002 5FFF	Reserved
		0x4002 4000 - 0x4002 4FFF	Reserved
		0x4002 3C00 - 0x4002 3FFF	Reserved
		0x4002 3800 - 0x4002 3BFF	Reserved
		0x4002 3400 - 0x4002 37FF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2C00 - 0x4002 2FFF	Reserved
		0x4002 2800 - 0x4002 2BFF	Reserved
		0x4002 2400 - 0x4002 27FF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1C00 - 0x4002 1FFF	Reserved
		0x4002 1800 - 0x4002 1BFF	Reserved
		0x4002 1400 - 0x4002 17FF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	Reserved
		0x4002 0400 - 0x4002 07FF	DMA1
		0x4002 0000 - 0x4002 03FF	DMA0
		0x4001 8400 - 0x4001 FFFF	Reserved
		0x4001 8000 - 0x4001 83FF	Reserved
	APB2	0x4001 7C00 - 0x4001 7FFF	Reserved
		0x4001 7800 - 0x4001 7BFF	Reserved
		0x4001 7400 - 0x4001 77FF	Reserved

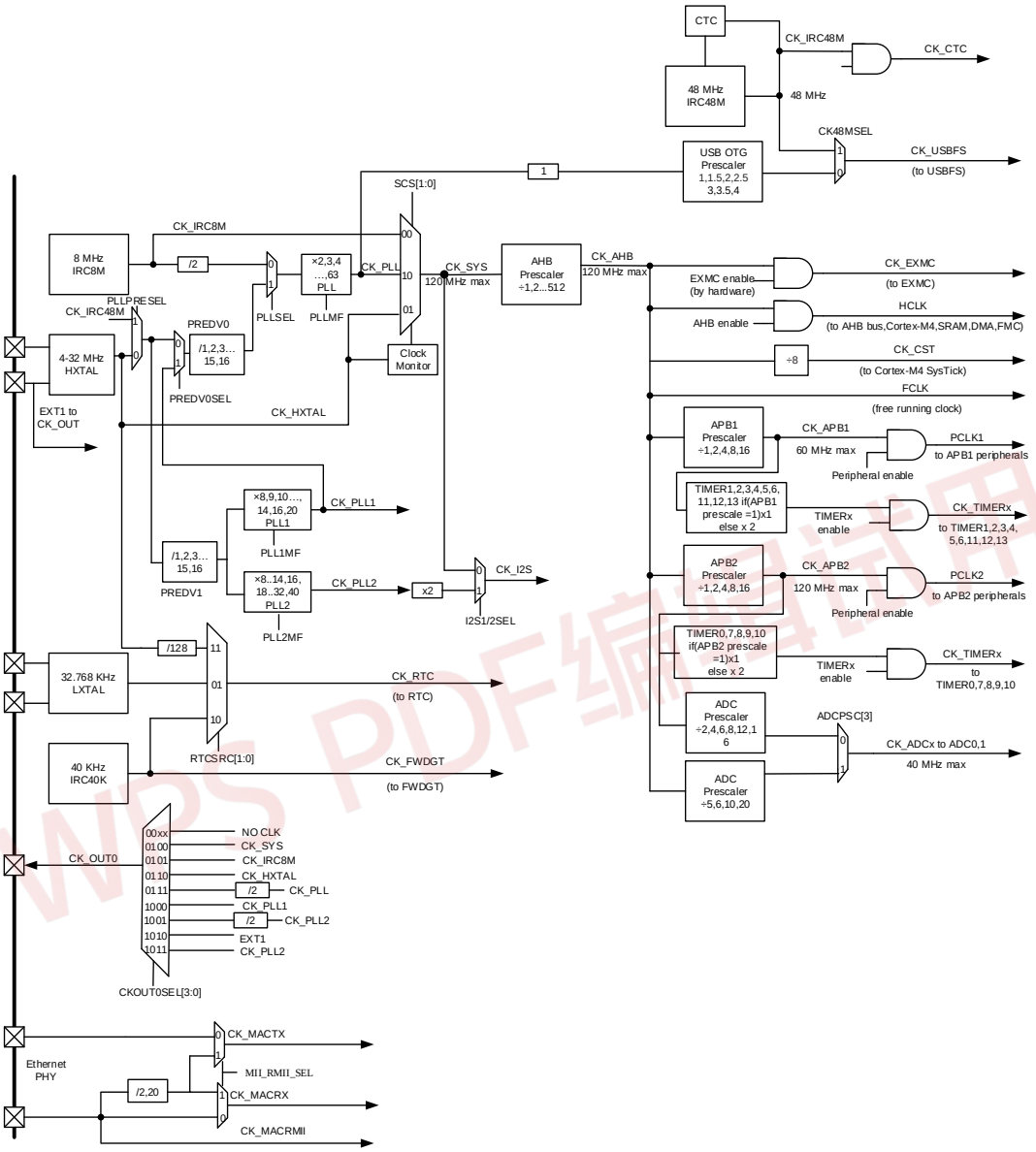
Pre-defined Regions	Bus	Address	Peripherals
		0x4001 7000 - 0x4001 73FF	Reserved
		0x4001 6C00 - 0x4001 6FFF	Reserved
		0x4001 6800 - 0x4001 6BFF	Reserved
		0x4001 5C00 - 0x4001 67FF	Reserved
		0x4001 5800 - 0x4001 5BFF	Reserved
		0x4001 5400 - 0x4001 57FF	TIMER10
		0x4001 5000 - 0x4001 53FF	TIMER9
		0x4001 4C00 - 0x4001 4FFF	TIMER8
		0x4001 4800 - 0x4001 4BFF	Reserved
		0x4001 4400 - 0x4001 47FF	Reserved
		0x4001 4000 - 0x4001 43FF	Reserved
		0x4001 3C00 - 0x4001 3FFF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	TIMER7
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	ADC1
		0x4001 2400 - 0x4001 27FF	ADC0
		0x4001 2000 - 0x4001 23FF	GPIOG
		0x4001 1C00 - 0x4001 1FFF	GPIOF
		0x4001 1800 - 0x4001 1BFF	GPIOE
		0x4001 1400 - 0x4001 17FF	GPIOD
		0x4001 1000 - 0x4001 13FF	GPIOC
		0x4001 0C00 - 0x4001 0FFF	GPIOB
		0x4001 0800 - 0x4001 0BFF	GPIOA
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	AFIO
	APB1	0x4000 CC00 - 0x4000 FFFF	Reserved
		0x4000 C800 - 0x4000 CBFF	CTC
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	Reserved
		0x4000 8000 - 0x4000 BFFF	Reserved
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	DAC
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6C00 - 0x4000 6FFF	BKP
		0x4000 6800 - 0x4000 6BFF	CAN1
		0x4000 6400 - 0x4000 67FF	CAN0
		0x4000 6000 - 0x4000 63FF	CAN SRAM 512 bytes

Pre-defined Regions	Bus	Address	Peripherals
		0x4000 5C00 - 0x4000 5FFF	Reserved
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	UART4
		0x4000 4C00 - 0x4000 4FFF	UART3
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	SPI2/I2S2
		0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 1C00 - 0x4000 1FFF	TIMER12
		0x4000 1800 - 0x4000 1BFF	TIMER11
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x4000 0800 - 0x4000 0BFF	TIMER3
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM	AHB	0x2007 0000 - 0x3FFF FFFF	Reserved
		0x2006 0000 - 0x2006 FFFF	Reserved
		0x2003 0000 - 0x2005 FFFF	Reserved
		0x2001 8000 - 0x2002 FFFF	Reserved
		0x2000 0000 - 0x2001 7FFF	SRAM
Code	AHB	0x1FFF F810 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF F80F	Option Bytes
		0x1FFF F000 - 0x1FFF F7FF	Boot loader
		0x1FFF C010 - 0x1FFF EFFF	
		0x1FFF C000 - 0x1FFF C00F	
		0x1FFF B000 - 0x1FFF BFFF	
		0x1FFF 7A10 - 0x1FFF AFFF	Reserved
		0x1FFF 7800 - 0x1FFF 7A0F	Reserved
		0x1FFF 0000 - 0x1FFF 77FF	Reserved
		0x1FFE C010 - 0x1FFE FFFF	Reserved
		0x1FFE C000 - 0x1FFE C00F	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x1001 0000 - 0x1FFE BFFF	Reserved
		0x1000 0000 - 0x1000 FFFF	Reserved
		0x083C 0000 - 0x0FFF FFFF	Reserved
		0x0830 0000 - 0x083B FFFF	Reserved
		0x0810 0000 - 0x082F FFFF	Reserved
		0x0800 0000 - 0x080F FFFF	Main Flash
		0x0030 0000 - 0x07FF FFFF	Reserved
		0x0010 0000 - 0x002F FFFF	Aliased to Main Flash or Boot loader
		0x0002 0000 - 0x000F FFFF	
		0x0000 0000 - 0x0001 FFFF	

2.5. Clock tree

Figure 2-5 GD32F307xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillators

IRC40K: Internal 40K RC oscillator

IRC48M: Internal 48M RC oscillators

2.6. Pin definitions

2.6.1. GD32F307Zx LQFP144 pin definitions

Table 2-3. GD32F307Zx LQFP144 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PE2	1	I/O	5VT	Default: PE2 Alternate: TRACECK, EXMC_A23
PE3	2	I/O	5VT	Default: PE3 Alternate: TRACED0, EXMC_A19
PE4	3	I/O	5VT	Default: PE4 Alternate:TRACED1, EXMC_A20
PE5	4	I/O	5VT	Default: PE5 Alternate:TRACED2, EXMC_A21 Remap: TIMER8_CH0(3)
PE6	5	I/O	5VT	Default: PE6 Alternate:TRACED3, EXMC_A22 Remap: TIMER8_CH1(3)
V_{BAT}	6	P		Default: V_{BAT}
PC13-TAMPER-RTC	7	I/O		Default: PC13 Alternate: TAMPER-RTC
PC14-OSC32IN	8	I/O		Default: PC14 Alternate: OSC32IN
PC15-OSC32OUT	9	I/O		Default: PC15 Alternate: OSC32OUT
PF0	10	I/O	5VT	Default: PF0 Alternate: EXMC_A0 Remap: CTC_SYNC
PF1	11	I/O	5VT	Default: PF1 Alternate: EXMC_A1
PF2	12	I/O	5VT	Default: PF2 Alternate: EXMC_A2
PF3	13	I/O	5VT	Default: PF3 Alternate: EXMC_A3
PF4	14	I/O	5VT	Default: PF4 Alternate: EXMC_A4
PF5	15	I/O	5VT	Default: PF5 Alternate: EXMC_A5
V_{SS_5}	16	P		Default: V_{SS_5}
V_{DD_5}	17	P		Default: V_{DD_5}

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PF6	18	I/O		Default: PF6 Alternate: EXMC_NIORD Remap: TIMER9_CH0
PF7	19	I/O		Default: PF7 Alternate: EXMC_NREG Remap: TIMER10_CH0(3)
PF8	20	I/O		Default: PF8 Alternate: EXMC_NIOWR Remap: TIMER12_CH0(3)
PF9	21	I/O		Default: PF9 Alternate: EXMC_CD Remap: TIMER13_CH0(3)
PF10	22	I/O		Default: PF10 Alternate: EXMC_INTR
OSCIN	23	I		Default: OSCIN Remap: PD0
OSCOUT	24	O		Default: OSCOUT Remap: PD1
NRST	25	I/O		Default: NRST
PC0	26	I/O		Default: PC0 Alternate: ADC01_IN10
PC1	27	I/O		Default: PC1 Alternate: ADC01_IN11, ENET_MDC
PC2	28	I/O		Default: PC2 Alternate: ADC01_IN12, ENET_MII_TXD2
PC3	29	I/O		Default: PC3 Alternate: ADC01_IN13, ENET_MII_TX_CLK
V_{SSA}	30	P		Default: V_{SSA}
V_{REF-}	31	P		Default: V_{REF-}
V_{REF+}	32	P		Default: V_{REF+}
V_{DDA}	33	P		Default: V_{DDA}
PA0-WKUP	34	I/O		Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, ENET_MII_CRS
PA1	35	I/O		Default: PA1 Alternate: USART1_RTS, ADC01_IN1, TIMER1_CH1, TIMER4_CH1, ENET_MII_RX_CLK, ENET_RMII_REF_CLK
PA2	36	I/O		Default: PA2 Alternate: USART1_TX, ADC01_IN2, TIMER1_CH2, TIMER4_CH2, TIMER8_CH0(3), ENET_MDIO,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				SPI0_IO2
PA3	37	I/O		Default: PA3 Alternate: USART1_RX, ADC01_IN3, TIMER1_CH3, TIMER4_CH3, TIMER8_CH1(3), ENET_MII_COL, SPI0_IO3
V_{SS_4}	38	P		Default: V_{SS_4}
V_{DD_4}	39	P		Default: V_{DD_4}
PA4	40	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4, DAC_OUT0 Remap:SPI2_NSS, I2S2_WS
PA5	41	I/O		Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1
PA6	42	I/O		Default: PA6 Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0, TIMER7_BRKIN, TIMER12_CH0(3) Remap: TIMER0_BRKIN
PA7	43	I/O		Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1, TIMER7_CH0_ON, TIMER13_CH0(3), ENET_MII_RX_DV, ENET_RMII_CRS_DV Remap: TIMER0_CH0_ON
PC4	44	I/O		Default: PC4 Alternate: ADC01_IN14, ENET_MII_RXD0, ENET_RMII_RXD0
PC5	45	I/O		Default: PC5 Alternate: ADC01_IN15, ENET_MII_RXD1, ENET_RMII_RXD1
PB0	46	I/O		Default: PB0 Alternate: ADC01_IN8, TIMER2_CH2, TIMER7_CH1_ON, ENET_MII_RXD2 Remap: TIMER0_CH1_ON
PB1	47	I/O		Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3, TIMER7_CH2_ON, ENET_MII_RXD3 Remap: TIMER0_CH2_ON
PB2	48	I/O	5VT	Default: PB2, BOOT1
PF11	49	I/O	5VT	Default: PF11 Alternate: EXMC_NIOS16
PF12	50	I/O	5VT	Default: PF12 Alternate: EXMC_A6
V_{SS_6}	51	P		Default: V_{SS_6}

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{DD_6}	52	P		Default: V_{DD_6}
PF13	53	I/O	5VT	Default: PF13 Alternate: EXMC_A7
PF14	54	I/O	5VT	Default: PF14 Alternate: EXMC_A8
PF15	55	I/O	5VT	Default: PF15 Alternate: EXMC_A9
PG0	56	I/O	5VT	Default: PG0 Alternate: EXMC_A10
PG1	57	I/O	5VT	Default: PG1 Alternate: EXMC_A11
PE7	58	I/O	5VT	Default: PE7 Alternate: EXMC_D4 Remap: TIMER0_ETI
PE8	59	I/O	5VT	Default: PE8 Alternate: EXMC_D5 Remap: TIMER0_CH0_ON
PE9	60	I/O	5VT	Default: PE9 Alternate: EXMC_D6 Remap: TIMER0_CH0
V_{SS_7}	61	P		Default: V_{SS_7}
V_{DD_7}	62	P		Default: V_{DD_7}
PE10	63	I/O	5VT	Default: PE10 Alternate: EXMC_D7 Remap: TIMER0_CH1_ON
PE11	64	I/O	5VT	Default: PE11 Alternate: EXMC_D8 Remap: TIMER0_CH1
PE12	65	I/O	5VT	Default: PE12 Alternate: EXMC_D9 Remap: TIMER0_CH2_ON
PE13	66	I/O	5VT	Default: PE13 Alternate: EXMC_D10 Remap: TIMER0_CH2
PE14	67	I/O	5VT	Default: PE14 Alternate: EXMC_D11 Remap: TIMER0_CH3
PE15	68	I/O	5VT	Default: PE15 Alternate: EXMC_D12 Remap: TIMER0_BRKIN
PB10	69	I/O	5VT	Default: PB10 Alternate: I2C1_SCL, USART2_TX, ENET_MII_RX_ER

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Remap: TIMER1_CH2
PB11	70	I/O	5VT	Default: PB11 Alternate: I2C1_SDA, USART2_RX, ENET_MII_TX_EN, ENET_RMII_TX_EN Remap: TIMER1_CH3
V_{SS_1}	71	P		Default: V_{SS_1}
V_{DD_1}	72	P		Default: V_{DD_1}
PB12	73	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN, I2S1_WS, CAN1_RX, ENET_MII_TXD0, ENET_RMII_TXD0
PB13	74	I/O	5VT	Default: PB13 Alternate: SPI1_SCK, USART2_CTS, TIMER0_CH0_ON, I2S1_CK, CAN1_TX, ENET_MII_TXD1, ENET_RMII_TXD1
PB14	75	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON, TIMER11_CH0(3)
PB15	76	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD, TIMER11_CH1(3)
PD8	77	I/O	5VT	Default: PD8 Alternate: EXMC_D13 Remap: USART2_TX, ENET_MII_RX_DV, ENET_RMII_CRS_DV
PD9	78	I/O	5VT	Default: PD9 Alternate: EXMC_D14 Remap: USART2_RX, ENET_MII_RXD0, ENET_RMII_RXD0
PD10	79	I/O	5VT	Default: PD10 Alternate: EXMC_D15 Remap: USART2_CK, ENET_MII_RXD1, ENET_RMII_RXD1
PD11	80	I/O	5VT	Default: PD11 Alternate: EXMC_A16 Remap: USART2_CTS, ENET_MII_RXD2
PD12	81	I/O	5VT	Default: PD12 Alternate: EXMC_A17 Remap: TIMER3_CH0, USART2_RTS, ENET_MII_RXD3
PD13	82	I/O	5VT	Default: PD13 Alternate: EXMC_A18 Remap: TIMER3_CH1

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{SS_8}	83	P		Default: V_{SS_8}
V_{DD_8}	84	P		Default: V_{DD_8}
PD14	85	I/O	5VT	Default: PD14 Alternate: EXMC_D0 Remap: TIMER3_CH2
PD15	86	I/O	5VT	Default: PD15 Alternate: EXMC_D1 Remap: TIMER3_CH3, CTC_SYNC
PG2	87	I/O	5VT	Default: PG2 Alternate: EXMC_A12
PG3	88	I/O	5VT	Default: PG3 Alternate: EXMC_A13
PG4	89	I/O	5VT	Default: PG4 Alternate: EXMC_A14
PG5	90	I/O	5VT	Default: PG5 Alternate: EXMC_A15
PG6	91	I/O	5VT	Default: PG6 Alternate: EXMC_INT1
PG7	92	I/O	5VT	Default: PG7 Alternate: EXMC_INT2
PG8	93	I/O	5VT	Default: PG8
V_{SS_9}	94	P		Default: V_{SS_9}
V_{DD_9}	95	P		Default: V_{DD_9}
PC6	96	I/O	5VT	Default: PC6 Alternate: I2S1_MCK, TIMER7_CH0 Remap: TIMER2_CH0
PC7	97	I/O	5VT	Default: PC7 Alternate: I2S2_MCK, TIMER7_CH1 Remap: TIMER2_CH1
PC8	98	I/O	5VT	Default: PC8 Alternate: TIMER7_CH2 Remap: TIMER2_CH2
PC9	99	I/O	5VT	Default: PC9 Alternate: TIMER7_CH3 Remap: TIMER2_CH3
PA8	100	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, USBFS_SOF, CTC_SYNC
PA9	101	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS
PA10	102	I/O	5VT	Default: PA10

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: USART0_RX, TIMER0_CH2, USBFS_ID
PA11	103	I/O	5VT	Default: PA11 Alternate: USART0_CTS, CAN0_RX, USBFS_DM, TIMER0_CH3
PA12	104	I/O	5VT	Default: PA12 Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI
PA13	105	I/O	5VT	Default: JTMS, SWDIO Remap: PA13
NC	106	-	-	-
V_{SS_2}	107	P		Default: V_{SS_2}
V_{DD_2}	108	P		Default: V_{DD_2}
PA14	109	I/O	5VT	Default: JTCK, SWCLK Remap: PA14
PA15	110	I/O	5VT	Default: JTDI Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS
PC10	111	I/O	5VT	Default: PC10 Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK
PC11	112	I/O	5VT	Default: PC11 Alternate: UART3_RX Remap: USART2_RX, SPI2_MISO
PC12	113	I/O	5VT	Default: PC12 Alternate: UART4_TX Remap: USART2_CK, SPI2_MOSI, I2S2_SD
PD0	114	I/O	5VT	Default: PD0 Alternate: EXMC_D2 Remap: CAN0_RX, OSCIN
PD1	115	I/O	5VT	Default: PD1 Alternate: EXMC_D3 Remap: CAN0_TX, OSCOUT
PD2	116	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX
PD3	117	I/O	5VT	Default: PD3 Alternate: EXMC_CLK Remap: USART1_CTS
PD4	118	I/O	5VT	Default: PD4 Alternate: EXMC_NOE Remap: USART1_RTS
PD5	119	I/O	5VT	Default: PD5 Alternate: EXMC_NWE

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Remap: USART1_TX
V_{SS_10}	120	P		Default: V_{SS_10}
V_{DD_10}	121	P		Default: V_{DD_10}
PD6	122	I/O	5VT	Default: PD6 Alternate: EXMC_NWAIT Remap: USART1_RX
PD7	123	I/O	5VT	Default: PD7 Alternate: EXMC_NE0, EXMC_NCE1 Remap: USART1_CK
PG9	124	I/O	5VT	Default: PG9 Alternate: EXMC_NE1, EXMC_NCE2
PG10	125	I/O	5VT	Default: PG10 Alternate: EXMC_NCE3_0, EXMC_NE2
PG11	126	I/O	5VT	Default: PG11 Alternate: EXMC_NCE3_1
PG12	127	I/O	5VT	Default: PG12 Alternate: EXMC_NE3
PG13	128	I/O	5VT	Default: PG13 Alternate: EXMC_A24
PG14	129	I/O	5VT	Default: PG14 Alternate: EXMC_A25
V_{SS_11}	130	P		Default: V_{SS_11}
V_{DD_11}	131	P		Default: V_{DD_11}
PG15	132	I/O	5VT	Default: PG15
PB3	133	I/O	5VT	Default: JTDO Alternate:SPI2_SCK, I2S2_CK Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK
PB4	134	I/O	5VT	Default: NJTRST Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO
PB5	135	I/O		Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD, ENET_MII_PPS_OUT, ENET_RMII_PPS_OUT Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX
PB6	136	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, CAN1_TX, SPI0_IO2
PB7	137	I/O	5VT	Default: PB7 Alternate: I2C0_SDA , TIMER3_CH1, EXMC_NADV Remap: USART0_RX, SPI0_IO3
BOOT0	138	I		Default: BOOT0

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PB8	139	I/O	5VT	Default: PB8 Alternate: TIMER3_CH2, TIMER9_CH0(3), ENET_MII_TXD3 Remap: I2C0_SCL, CAN0_RX
PB9	140	I/O	5VT	Default: PB9 Alternate: TIMER3_CH3, TIMER10_CH0(3) Remap: I2C0_SDA, CAN0_TX
PE0	141	I/O	5VT	Default: PE0 Alternate: TIMER3_ETI, EXMC_NBL0
PE1	142	I/O	5VT	Default: PE1 Alternate: EXMC_NBL1
V_{SS_3}	143	P		Default: V_{SS_3}
V_{DD_3}	144	P		Default: V_{DD_3}

Notes:

(1)Type: I = input, O = output, P = power.

(2)I/O Level: 5VT = 5 V tolerant.

(3)Functions are available in GD32F307ZG devices.

2.6.2. GD32F307Vx LQFP100 pin definitions

Table 2-4. GD32F307Vx LQFP100 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PE2	1	I/O	5VT	Default: PE2 Alternate: TRACECK, EXMC_A23
PE3	2	I/O	5VT	Default: PE3 Alternate: TRACED0, EXMC_A19
PE4	3	I/O	5VT	Default: PE4 Alternate:TRACED1, EXMC_A20
PE5	4	I/O	5VT	Default: PE5 Alternate:TRACED2, EXMC_A21 Remap: TIMER8_CH0(3)
PE6	5	I/O	5VT	Default: PE6 Alternate:TRACED3, EXMC_A22 Remap: TIMER8_CH1(3)
V_{BAT}	6	P		Default: V_{BAT}
PC13-TAMPER-RTC	7	I/O		Default: PC13 Alternate: TAMPER-RTC
PC14-OSC32IN	8	I/O		Default: PC14 Alternate: OSC32IN
PC15-OSC32OUT	9	I/O		Default: PC15 Alternate: OSC32OUT
V_{SS_5}	10	P		Default: V_{SS_5}
V_{DD_5}	11	P		Default: V_{DD_5}
OSCIN	12	I		Default: OSCIN Remap: PD0
OSCOUT	13	O		Default: OSCOUT Remap: PD1
NRST	14	I/O		Default: NRST
PC0	15	I/O		Default: PC0 Alternate: ADC01_IN10
PC1	16	I/O		Default: PC1 Alternate: ADC01_IN11, ENET_MDC
PC2	17	I/O		Default: PC2 Alternate: ADC01_IN12, ENET_MII_TXD2
PC3	18	I/O		Default: PC3 Alternate: ADC01_IN13, ENET_MII_TX_CLK
V_{SSA}	19	P		Default: V_{SSA}
V_{REF-}	20	P		Default: V_{REF-}
V_{REF+}	21	P		Default: V_{REF+}

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{DDA}	22	P		Default: V_{DDA}
PA0-WKUP	23	I/O		Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI(4), ENET_MII_CRS
PA1	24	I/O		Default: PA1 Alternate: USART1_RTS, ADC01_IN1, TIMER1_CH1, TIMER4_CH1, ENET_MII_RX_CLK, ENET_RMII_REF_CLK
PA2	25	I/O		Default: PA2 Alternate: USART1_TX, ADC01_IN2, TIMER1_CH2, TIMER4_CH2, TIMER8_CH0(3), ENET_MDIO,SPI0_IO2
PA3	26	I/O		Default: PA3 Alternate: USART1_RX, ADC01_IN3, TIMER1_CH3, TIMER4_CH3, TIMER8_CH1(3), ENET_MII_COL, SPI0_IO3
V_{SS_4}	27	P		Default: V_{SS_4}
V_{DD_4}	28	P		Default: V_{DD_4}
PA4	29	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4, DAC_OUT0 Remap:SPI2_NSS, I2S2_WS
PA5	30	I/O		Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1
PA6	31	I/O		Default: PA6 Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0, TIMER7_BRKIN(4), TIMER12_CH0(3) Remap: TIMER0_BRKIN
PA7	32	I/O		Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1, TIMER7_CH0_ON(4), TIMER13_CH0(3), ENET_MII_RX_DV, ENET_RMII_CRS_DV Remap: TIMER0_CH0_ON
PC4	33	I/O		Default: PC4 Alternate: ADC01_IN14, ENET_MII_RXD0, ENET_RMII_RXD0
PC5	34	I/O		Default: PC5 Alternate: ADC01_IN15, ENET_MII_RXD1, ENET_RMII_RXD1
PB0	35	I/O		Default: PB0 Alternate: ADC01_IN8, TIMER2_CH2, TIMER7_CH1_ON(4), ENET_MII_RXD2

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Remap: TIMER0_CH1_ON
PB1	36	I/O		Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3, TIMER7_CH2_ON(4), ENET_MII_RXD3 Remap: TIMER0_CH2_ON
PB2	37	I/O	5VT	Default: PB2, BOOT1
PE7	38	I/O	5VT	Default: PE7 Alternate: EXMC_D4 Remap: TIMER0_ETI
PE8	39	I/O	5VT	Default: PE8 Alternate: EXMC_D5 Remap: TIMER0_CH0_ON
PE9	40	I/O	5VT	Default: PE9 Alternate: EXMC_D6 Remap: TIMER0_CH0
PE10	41	I/O	5VT	Default: PE10 Alternate: EXMC_D7 Remap: TIMER0_CH1_ON
PE11	42	I/O	5VT	Default: PE11 Alternate: EXMC_D8 Remap: TIMER0_CH1
PE12	43	I/O	5VT	Default: PE12 Alternate: EXMC_D9 Remap: TIMER0_CH2_ON
PE13	44	I/O	5VT	Default: PE13 Alternate: EXMC_D10 Remap: TIMER0_CH2
PE14	45	I/O	5VT	Default: PE14 Alternate: EXMC_D11 Remap: TIMER0_CH3
PE15	46	I/O	5VT	Default: PE15 Alternate: EXMC_D12 Remap: TIMER0_BRKIN
PB10	47	I/O	5VT	Default: PB10 Alternate: I2C1_SCL, USART2_TX, ENET_MII_RX_ER Remap: TIMER1_CH2
PB11	48	I/O	5VT	Default: PB11 Alternate: I2C1_SDA, USART2_RX, ENET_MII_TX_EN, ENET_RMII_TX_EN Remap: TIMER1_CH3
V_{SS_1}	49	P		Default: V_{SS_1}
V_{DD_1}	50	P		Default: V_{DD_1}

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PB12	51	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN, I2S1_WS, CAN1_RX, ENET_MII_TXD0, ENET_RMII_TXD0
PB13	52	I/O	5VT	Default: PB13 Alternate: SPI1_SCK, USART2_CTS, TIMER0_CH0_ON, I2S1_CK, CAN1_TX, ENET_MII_TXD1, ENET_RMII_TXD1
PB14	53	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON, TIMER11_CH0(3)
PB15	54	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD, TIMER11_CH1(3)
PD8	55	I/O	5VT	Default: PD8 Alternate: EXMC_D13 Remap: USART2_TX, ENET_MII_RX_DV, ENET_RMII_CRS_DV
PD9	56	I/O	5VT	Default: PD9 Alternate: EXMC_D14 Remap: USART2_RX, ENET_MII_RXD0, ENET_RMII_RXD0
PD10	57	I/O	5VT	Default: PD10 Alternate: EXMC_D15 Remap: USART2_CK, ENET_MII_RXD1, ENET_RMII_RXD1
PD11	58	I/O	5VT	Default: PD11 Alternate: EXMC_A16 Remap: USART2_CTS, ENET_MII_RXD2
PD12	59	I/O	5VT	Default: PD12 Alternate: EXMC_A17 Remap: TIMER3_CH0, USART2_RTS, ENET_MII_RXD3
PD13	60	I/O	5VT	Default: PD13 Alternate: EXMC_A18 Remap: TIMER3_CH1
PD14	61	I/O	5VT	Default: PD14 Alternate: EXMC_D0 Remap: TIMER3_CH2
PD15	62	I/O	5VT	Default: PD15 Alternate: EXMC_D1 Remap: TIMER3_CH3, CTC_SYNC
PC6	63	I/O	5VT	Default: PC6

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: I2S1_MCK, TIMER7_CH0(4) Remap: TIMER2_CH0
PC7	64	I/O	5VT	Default: PC7 Alternate: I2S2_MCK, TIMER7_CH1(4) Remap: TIMER2_CH1
PC8	65	I/O	5VT	Default: PC8 Alternate: TIMER7_CH2(4) Remap: TIMER2_CH2
PC9	66	I/O	5VT	Default: PC9 Alternate: TIMER7_CH3(4) Remap: TIMER2_CH3
PA8	67	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, USBFS_SOF, CTC_SYNC
PA9	68	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS
PA10	69	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, USBFS_ID
PA11	70	I/O	5VT	Default: PA11 Alternate: USART0_CTS, CAN0_RX, USBFS_DM, TIMER0_CH3
PA12	71	I/O	5VT	Default: PA12 Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI
PA13	72	I/O	5VT	Default: JTMS, SWDIO Remap: PA13
NC	73	-	-	-
V_{SS_2}	74	P		Default: V_{SS_2}
V_{DD_2}	75	P		Default: V_{DD_2}
PA14	76	I/O	5VT	Default: JTCK, SWCLK Remap: PA14
PA15	77	I/O	5VT	Default: JTDI Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS
PC10	78	I/O	5VT	Default: PC10 Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK
PC11	79	I/O	5VT	Default: PC11 Alternate: UART3_RX Remap: USART2_RX, SPI2_MISO
PC12	80	I/O	5VT	Default: PC12

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: UART4_TX Remap: USART2_CK, SPI2_MOSI, I2S2_SD
PD0	81	I/O	5VT	Default: PD0 Alternate: EXMC_D2 Remap: CAN0_RX, OSCIN
PD1	82	I/O	5VT	Default: PD1 Alternate: EXMC_D3 Remap: CAN0_TX, OSCOUT
PD2	83	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX
PD3	84	I/O	5VT	Default: PD3 Alternate: EXMC_CLK Remap: USART1_CTS
PD4	85	I/O	5VT	Default: PD4 Alternate: EXMC_NOE Remap: USART1_RTS
PD5	86	I/O	5VT	Default: PD5 Alternate: EXMC_NWE Remap: USART1_TX
PD6	87	I/O	5VT	Default: PD6 Alternate: EXMC_NWAIT Remap: USART1_RX
PD7	88	I/O	5VT	Default: PD7 Alternate: EXMC_NE0, EXMC_NCE1 Remap: USART1_CK
PB3	89	I/O	5VT	Default: JTDO Alternate:SPI2_SCK, I2S2_CK Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK
PB4	90	I/O	5VT	Default: NJTRST Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO
PB5	91	I/O		Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD, ENET_MII_PPS_OUT, ENET_RMII_PPS_OUT Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX
PB6	92	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, CAN1_TX, SPI0_IO2
PB7	93	I/O	5VT	Default: PB7 Alternate: I2C0_SDA , TIMER3_CH1, EXMC_NADV Remap: USART0_RX, SPI0_IO3
BOOT0	94	I		Default: BOOT0

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PB8	95	I/O	5VT	Default: PB8 Alternate: TIMER3_CH2, TIMER9_CH0(3), ENET_MII_TXD3 Remap: I2C0_SCL, CAN0_RX
PB9	96	I/O	5VT	Default: PB9 Alternate: TIMER3_CH3, TIMER10_CH0(3) Remap: I2C0_SDA, CAN0_TX
PE0	97	I/O	5VT	Default: PE0 Alternate: TIMER3_ETI, EXMC_NBL0
PE1	98	I/O	5VT	Default: PE1 Alternate: EXMC_NBL1
V_{SS_3}	99	P		Default: V_{SS_3}
V_{DD_3}	100	P		Default: V_{DD_3}

Notes:

(1)Type: I = input, O = output, P = power.

(2)I/O Level: 5VT = 5 V tolerant.

(3)Functions are available in GD32F307VG devices.

(4)Functions are available in GD32F307VE/G devices.

2.6.3. GD32F307Rx LQFP64 pin definitions

Table 2-5. GD32F307Rx LQFP64 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{BAT}	1	P		Default: V_{BAT}
PC13-TAMPER-RTC	2	I/O		Default: PC13 Alternate: TAMPER-RTC
PC14-OSC32IN	3	I/O		Default: PC14 Alternate: OSC32IN
PC15-OSC32OUT	4	I/O		Default: PC15 Alternate: OSC32OUT
OSCIN	5	I		Default: OSCIN Remap: PD0(5)
OSCOUT	6	O		Default: OSCOUT Remap: PD1(5)
NRST	7	I/O		Default: NRST
PC0	8	I/O		Default: PC0 Alternate: ADC01_IN10
PC1	9	I/O		Default: PC1 Alternate: ADC01_IN11, ENET_MDC
PC2	10	I/O		Default: PC2 Alternate: ADC01_IN12, ENET_MII_TXD2
PC3	11	I/O		Default: PC3 Alternate: ADC01_IN13, ENET_MII_TX_CLK
V_{SSA}	12	P		Default: V_{SSA}
V_{DDA}	13	P		Default: V_{DDA}
PA0-WKUP	14	I/O		Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI(4), ENET_MII_CRS
PA1	15	I/O		Default: PA1 Alternate: USART1_RTS, ADC01_IN1, TIMER1_CH1, TIMER4_CH1, ENET_MII_RX_CLK, ENET_RMII_REF_CLK
PA2	16	I/O		Default: PA2 Alternate: USART1_TX, ADC01_IN2, TIMER1_CH2, TIMER4_CH2, TIMER8_CH0(3), ENET_MDIO,SPI0_IO2
PA3	17	I/O		Default: PA3 Alternate: USART1_RX, ADC01_IN3, TIMER1_CH3, TIMER4_CH3, TIMER8_CH1(3), ENET_MII_COL,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				SPI0_IO3
V_{SS_4}	18	P		Default: V_{SS_4}
V_{DD_4}	19	P		Default: V_{DD_4}
PA4	20	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4, DAC_OUT0 Remap:SPI2_NSS, I2S2_WS
PA5	21	I/O		Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1
PA6	22	I/O		Default: PA6 Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0, TIMER7_BRKIN(4), TIMER12_CH0(3) Remap: TIMER0_BRKIN
PA7	23	I/O		Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1, TIMER7_CH0_ON(4), TIMER13_CH0(3), ENET_MII_RX_DV, ENET_RMII_CRS_DV Remap: TIMER0_CH0_ON
PC4	24	I/O		Default: PC4 Alternate: ADC01_IN14, ENET_MII_RXD0, ENET_RMII_RXD0
PC5	25	I/O		Default: PC5 Alternate: ADC01_IN15, ENET_MII_RXD1, ENET_RMII_RXD1
PB0	26	I/O		Default: PB0 Alternate: ADC01_IN8, TIMER2_CH2, TIMER7_CH1_ON(4), ENET_MII_RXD2 Remap: TIMER0_CH1_ON
PB1	27	I/O		Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3, TIMER7_CH2_ON(4), ENET_MII_RXD3 Remap: TIMER0_CH2_ON
PB2	28	I/O	5VT	Default: PB2, BOOT1
PB10	29	I/O	5VT	Default: PB10 Alternate: I2C1_SCL, USART2_TX, ENET_MII_RX_ER Remap: TIMER1_CH2
PB11	30	I/O	5VT	Default: PB11 Alternate: I2C1_SDA, USART2_RX, ENET_MII_TX_EN, ENET_RMII_TX_EN Remap: TIMER1_CH3
V_{SS_1}	31	P		Default: V_{SS_1}
V_{DD_1}	32	P		Default: V_{DD_1}

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PB12	33	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN, I2S1_WS, CAN1_RX, ENET_MII_TXD0, ENET_RMII_TXD0
PB13	34	I/O	5VT	Default: PB13 Alternate: SPI1_SCK, USART2_CTS, TIMER0_CH0_ON, I2S1_CK, CAN1_TX, ENET_MII_TXD1, ENET_RMII_TXD1
PB14	35	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON, TIMER11_CH0(3)
PB15	36	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD, TIMER11_CH1(3)
PC6	37	I/O	5VT	Default: PC6 Alternate: I2S1_MCK, TIMER7_CH0(4) Remap: TIMER2_CH0
PC7	38	I/O	5VT	Default: PC7 Alternate: I2S2_MCK, TIMER7_CH1(4) Remap: TIMER2_CH1
PC8	39	I/O	5VT	Default: PC8 Alternate: TIMER7_CH2(4) Remap: TIMER2_CH2
PC9	40	I/O	5VT	Default: PC9 Alternate: TIMER7_CH3(4) Remap: TIMER2_CH3
PA8	41	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, USBFS_SOF, CTC_SYNC
PA9	42	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS
PA10	43	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, USBFS_ID
PA11	44	I/O	5VT	Default: PA11 Alternate: USART0_CTS, CAN0_RX, USBFS_DM, TIMER0_CH3
PA12	45	I/O	5VT	Default: PA12 Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI
PA13	46	I/O	5VT	Default: JTMS, SWDIO Remap: PA13
V_{SS_2}	47	P		Default: V_{SS_2}

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{DD_2}	48	P		Default: V_{DD_2}
PA14	49	I/O	5VT	Default: JTCK, SWCLK Remap: PA14
PA15	50	I/O	5VT	Default: JTDI Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS
PC10	51	I/O	5VT	Default: PC10 Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK
PC11	52	I/O	5VT	Default: PC11 Alternate: UART3_RX Remap: USART2_RX, SPI2_MISO
PC12	53	I/O	5VT	Default: PC12 Alternate: UART4_TX Remap: USART2_CK, SPI2_MOSI, I2S2_SD
PD2	54	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX
PB3	55	I/O	5VT	Default: JTDO Alternate:SPI2_SCK, I2S2_CK Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK
PB4	56	I/O	5VT	Default: NJTRST Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO
PB5	57	I/O		Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD, ENET_MII_PPS_OUT, ENET_RMII_PPS_OUT Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX
PB6	58	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, CAN1_TX, SPI0_IO2
PB7	59	I/O	5VT	Default: PB7 Alternate: I2C0_SDA , TIMER3_CH1 Remap: USART0_RX, SPI0_IO3
BOOT0	60	I		Default: BOOT0
PB8	61	I/O	5VT	Default: PB8 Alternate: TIMER3_CH2, TIMER9_CH0(3), ENET_MII_TXD3 Remap: I2C0_SCL, CAN0_RX
PB9	62	I/O	5VT	Default: PB9 Alternate: TIMER3_CH3, TIMER10_CH0(3) Remap: I2C0_SDA, CAN0_TX

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{SS_3}	63	P		Default: V_{SS_3}
V_{DD_3}	64	P		Default: V_{DD_3}

Notes:

(1)Type: I = input, O = output, P = power.

(2)I/O Level: 5VT = 5 V tolerant.

(3)Functions are available in GD32F307RG devices.

(4)Functions are available in GD32F307RE/G devices.

(5)PD0/PD1 cannot be used for EXTI in this package.

3. Functional description

3.1. ARM® Cortex®-M4 core

The ARM® Cortex®-M4 processor is a high performance embedded processor with DSP instructions which allow efficient signal processing and complex algorithm execution. It brings an efficient, easy-to-use blend of control and signal processing capabilities to meet the digital signal control markets demand. The processor is highly configurable enabling a wide range of implementations from those requiring floating point operations, memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit ARM® Cortex®-M4 processor core

- Up to 120 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated DSP instructions
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M4 processor is based on the ARMv7-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M4:

- Internal Bus Matrix connected with ICode bus, DCode bus, System bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)
- Floating Point Unit (FPU)

3.2. On-chip memory

- Up to 1024 Kbytes of Flash memory, including code Flash and data Flash
- 96 KB of SRAM

The ARM® Cortex®-M4 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 1024 Kbytes of inner flash at most, which includes code Flash that available for storing programs and data, and accessed (R/W) at CPU clock speed with zero wait states. An extra data Flash is also included for storing data mainly. ***Table 2-2. GD32F307xx memory map*** shows the memory of the GD32F307xx

series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 48 MHz RC oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the two AHB domains are 120 MHz The maximum frequency of the two APB domains including APB1 is 60 MHz and APB2 is 120 MHz See ***Figure 2-5 GD32F307xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from/down to 2.6 V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10), USART1 (PD5 and PD6) and USBFS (PA9, PA11 and PA12) is also available for boot functions. It also can be used to transfer and update the Flash memory code, the data and the vector table sections. In default

condition, boot from bank0 of Flash memory is selected. It also supports to boot from bank1 of Flash memory by setting a bit in option bytes.

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, the USB wakeup and ENET wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.
- **Standby** mode
  In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC, the FWDG reset, and the rising edge on WKUP pin.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2.6 MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range: V_{SSA} to V_{DDA} (2.6 to 3.6 V)
- Temperature sensor

Up to two 12-bit 2.6 MSPS multi-channel ADCs are integrated in the device. It has a total of 18 multiplexed channels: 16 external channels, 1 channel for internal temperature sensor (V_{SENSE}), and 1 channel for internal reference voltage (V_{REFINT}). The input voltage range is between 2.6 V and 3.6 V. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx) and the advanced timers (TIMER0 and TIMER7) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

3.7. Digital to analog converter (DAC)

- Two 12-bit DACs with independent output channels
- 8-bit or 12-bit mode in conjunction with the DMA controller

The two 12-bit buffered DACs are used to generate variable analog outputs. The DAC channels can be triggered by the timer or EXTI with DMA support. In dual DAC channel operation, conversions could be done independently or simultaneously. The maximum output value of the DAC is V_{REF+}.

3.8. DMA

- 7 channel DMA0 controller and 5 channel DMA1 controller
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs, DAC, I2S

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9. General-purpose inputs/outputs (GPIOs)

- Up to 112 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 112 general purpose I/O pins (GPIO) in GD32F307xx, named PA0 ~ PA15 and PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0-PF15, PG0-PG15 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-

up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.10. Timers and PWM generation

- Two 16-bit advanced timer (TIMER0 & TIMER7), ten 16-bit general timers (TIMER1 ~ TIMER4, TIMER8 ~ TIMER13), and two 16-bit basic timer (TIMER5 & TIMER6)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (Free watchdog timer and window watchdog timer)

The advanced timer (TIMER0 & TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer, can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 ~ TIMER4 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER8 ~ TIMER13 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 & TIMER6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F307xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler, It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in

debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter.

The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11. Real time clock (RTC)

- 32-bit up-counter with a programmable 20-bit prescaler
- Alarm function
- Interrupt and wakeup event

The real time clock is an independent timer which provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and an expected interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.

3.12. Inter-integrated circuit (I2C)

- Up to two I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides several data transfer rates of up to 100 KHz in standard mode, up to 400 KHz in fast mode and up to 1 MHz in the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.13. Serial peripheral interface (SPI)

- Up to three SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode

- Hardware CRC calculation and transmit automatic CRC error checking
- Quad-SPI configuration available in master mode (only in SPI0)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI0.

3.14. Universal synchronous asynchronous receiver transmitter (USART)

- Up to three USARTs and two UARTs with operating frequency up to 7.5M Bits/s
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- USARTs support ISO 7816-3 compliant smart card interface

The USART (USART0, USART1 and USART2) and UART (UART3 & UART4) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART/UART also supports DMA function for high speed data communication except UART4.

3.15. Inter-IC sound (I2S)

- Two I2S bus Interfaces with sampling frequency from 8 KHz to 192 KHz
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32F307xx contain two I2S-bus interfaces that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequency from 8 KHz to 192 KHz is supported.

3.16. Universal serial bus full-speed interface (USBFS)

- One USB device/host/full-speed Interface with frequency up to 12 Mbit/s
- Internal 48 MHz oscillator (IRC48M) support crystal-less operation
- Internal main PLL for USBCLK compliantly
- Internal USBFS PHY support

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers. Transaction formatting is performed by the hardware, including CRC generation and checking. It supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. The required precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HXTAL crystal oscillator) or by the internal 48 MHz oscillator (IRC48M) in automatic trimming mode that allows crystal-less operation.

3.17. Controller area network (CAN)

- Two CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for CAN CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 28 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

3.18. Ethernet (ENET)

- IEEE 802.3 compliant media access controller (MAC) for Ethernet LAN
- 10/100 Mbit/s rates with dedicated DMA controller and SRAM
- Support hardware precision time protocol (PTP) with conformity to IEEE 1588

The Ethernet media access controller (MAC) conforms to IEEE 802.3 specifications and fully supports IEEE 1588 standards. The embedded MAC provides the interface to the required external network physical interface (PHY) for LAN bus connection via an internal media independent interface (MII) or a reduced media independent interface (RMII). The number of MII signals provided up to 16 with 25 MHz output and RMII up to 7 with 50 MHz output. The function of 32-bit CRC checking is also available.

3.19. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash, NAND Flash and PC card
- Provide ECC calculating hardware module for NAND Flash memory block
- Up to 16-bit data bus
- Support to interface with Motorola 6800 and Intel 8080 type LCD directly

External memory controller (EXMC) is an abbreviation of external memory controller. It is divided in to several sub-banks for external device support, each sub-bank has its own chip selection signal but at one time, only one bank can be accessed. The EXMC support code execution from external memory except NAND Flash and PC card. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

3.20. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.21. Package and operation temperature

- LQFP144 (GD32F307Zx), LQFP100 (GD32F307Vx) and LQFP64 (GD32F307Rx)
- Operation temperature range: -40°C to +85°C (industrial level)

4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings(1) (4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin(3)	V_{SS} - 0.3	V_{DD} + 3.6	V
	Input voltage on other I/O	V_{SS} - 0.3	3.6	V
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	—	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	±25	mA
T_A	Operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C

(1). Guaranteed by design, not tested in production.

(2). All main power and ground pins should be connected to an external power source within the allowable range.

(3). V_{IN} maximum value cannot exceed 6.5 V.

(4). It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

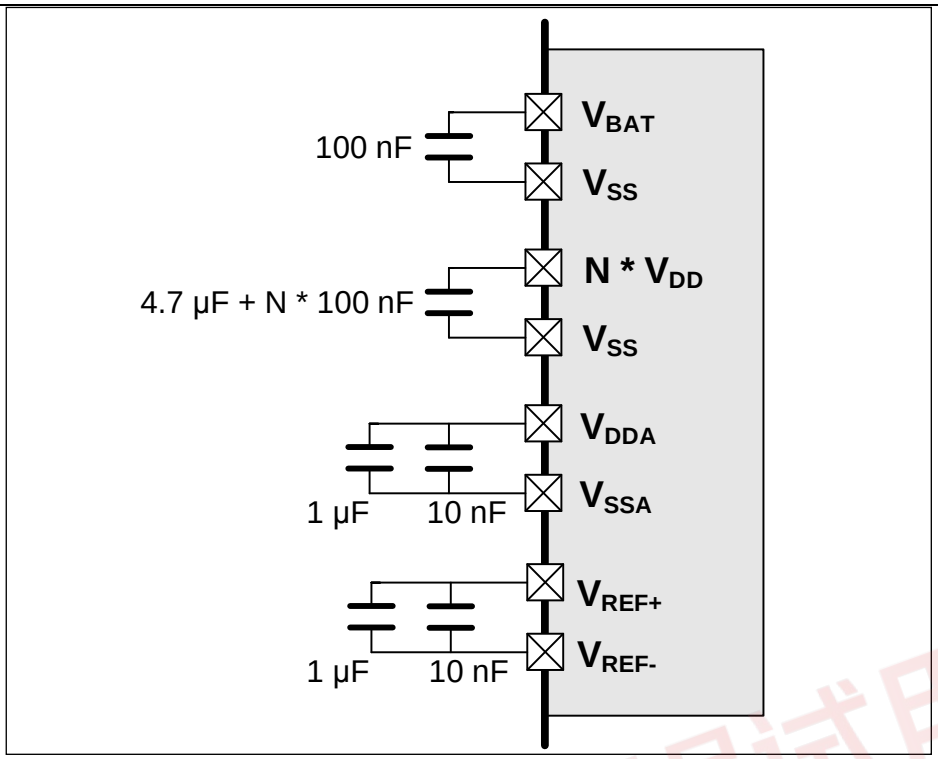
4.2. Operating conditions characteristics

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}	Supply voltage	—	2.6	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.6	3.3	3.6	V
V_{BAT}	Battery supply voltage	—	1.8	—	3.6	V

(1). Based on characterization, not tested in production.

Figure 4-1. Recommended power supply decoupling capacitors(1) (2)



(1). The V_{REF+} and V_{REF-} pins are only available on no less than 100-pin packages, or else the V_{REF+} and V_{REF-} pins are not available and internally connected to V_{DDA} and V_{SSA} pins.

(2). All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-3. Clock frequency(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	AHB clock frequency	—	—	120	MHz
f_{APB1}	APB1 clock frequency	—	—	60	MHz
f_{APB2}	APB2 clock frequency	—	—	120	MHz

(1). Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up/ Power down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	0	∞	µs/ V
	V_{DD} fall time rate		20	∞	

(1). Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions(1)(2)(3)

Symbol	Parameter	Conditions	Typ	Unit
$t_{start-up}$	Start-up time	Clock source from HXTAL	154	ms
		Clock source from IRC8M	154	

(1). Based on characterization, not tested in production.

(2). After power-up, the start-up time is the time between the rising edge of NRST high and the main function.

(3). PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics(1) (2)

Symbol	Parameter	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode	3.4	μs
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode（LDO On）	5.8	
	Wakeup from Deep-sleep mode（LDO in low power mode）	5.8	
$t_{Standby}$	Wakeup from Standby mode	154	ms

(1). Based on characterization, not tested in production.

(2). The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC8M = System clock = 8 MHz.

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7. Power consumption characteristics (2)(3)(4)(5)

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
I_{DD}+I_{DDA}	Supply current (Run mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals enabled	—	45.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals disabled	—	25.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals enabled	—	40.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals disabled	—	23.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 96 MHz, All peripherals enabled	—	36.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 96 MHz, All peripherals disabled	—	20.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 72 MHz, All peripherals enabled	—	27.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 72 MHz, All peripherals disabled	—	16.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 48 MHz, All peripherals enabled	—	19.3	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 48 MHz, All peripherals disabled	—	11.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 36 MHz, All peripherals enabled	—	15.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 36 MHz, All peripherals disabled	—	9.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 24 MHz, All peripherals enabled	—	10.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 24 MHz, All peripherals disabled	—	6.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals enabled	—	7.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals disabled	—	5.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, All peripherals enabled	—	4.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, All peripherals disabled	—	3.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, System clock = 4 MHz, All peripherals enabled	—	1.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, System clock = 4 MHz, All peripherals disabled	—	0.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, System clock = 2 MHz, All peripherals enabled	—	0.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, System Clock = 2 MHz, All peripherals disabled	—	0.6	—	mA
	Supply current (Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 120 MHz, CPU clock off, All peripherals enabled	—	31.4	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 120 MHz, CPU clock off, All peripherals disabled	—	10.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 108 MHz, CPU clock off, All peripherals enabled	—	28.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 108 MHz, CPU clock off, All peripherals disabled	—	9.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 96 MHz, CPU clock off, All peripherals enabled	—	25.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 96 MHz, CPU clock off, All peripherals disabled	—	8.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 72 MHz, CPU clock off, All peripherals enabled	—	19.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 72 MHz, CPU clock off, All peripherals disabled	—	7.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 48 MHz, CPU clock off, All peripherals enabled	—	13.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 48 MHz, CPU clock off, All peripherals disabled	—	5.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 36 MHz, CPU clock off, All peripherals enabled	—	10.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 36 MHz, CPU clock off, All peripherals disabled	—	4.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 24 MHz, CPU clock off, All peripherals enabled	—	7.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 24 MHz, CPU clock off, All peripherals disabled	—	3.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 16 MHz, CPU clock off, All peripherals enabled	—	5.9	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 16 MHz, CPU clock off, All peripherals disabled	—	3.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 8 MHz, CPU clock off, All peripherals enabled	—	4.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 8 MHz, CPU clock off, All peripherals disabled	—	2.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, System Clock = 4 MHz, CPU clock off, All peripherals enabled	—	1.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, System Clock = 4 MHz, CPU clock off, All peripherals disabled	—	0.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, System Clock = 2 MHz, CPU clock off, All peripherals enabled	—	0.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, System Clock = 2 MHz, CPU clock off, All peripherals disabled	—	0.3	—	mA
	Supply current (Deep-Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, LDO in run mode, IRC40K off, RTC off, All GPIOs analog mode	—	137.8	1100	µA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power mode, IRC40K off, RTC off, All GPIOs analog mode	—	109.1	1100	µA
		V_{DD} = V_{DDA} = 3.3 V, Main LDO in under drive mode, IRC40K off, RTC off, All GPIOs analog mode	—	124.2	1100	µA
		V_{DD} = V_{DDA} = 3.3 V, Low Power LDO in under drive mode, IRC40K off, RTC off, All GPIOs analog mode	—	94.9	1100	µA
	Supply current (Standby mode)	V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC on	—	5.2	22	µA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC off	—	4.9	22	µA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K off, RTC off	—	4.3	22	µA
I_{BAT}	Battery supply current (Backup mode)	V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	1.7	—	µA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	1.5	—	µA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.6 V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	1.3	—	µA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.8 V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	1.2	—	µA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	—	1.4	—	µA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	—	1.2	—	µA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	—	1.1	—	µA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.8 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	—	1.0	—	µA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	—	1.1	—	µA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	—	0.9	—	µA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	—	0.8	—	µA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.8 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	—	0.7	—	µA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving	—	1.0	—	µA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Low driving	—	0.9	—	µA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving	—	0.7	—	µA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.8 V, LXTAL on with external crystal, RTC on, LXTAL Low driving	—	0.6	—	μA

(1). Based on characterization, not tested in production.

(2). Unless otherwise specified, all values given for T_A = 25 ℃ and test result is mean value.

(3). When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.

(4). When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed, using PLL.

(5). When analog peripheral blocks such as ADCs, DACs, HXTAL, LXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered.

Figure 4-2. Typical supply current consumption in Run mode

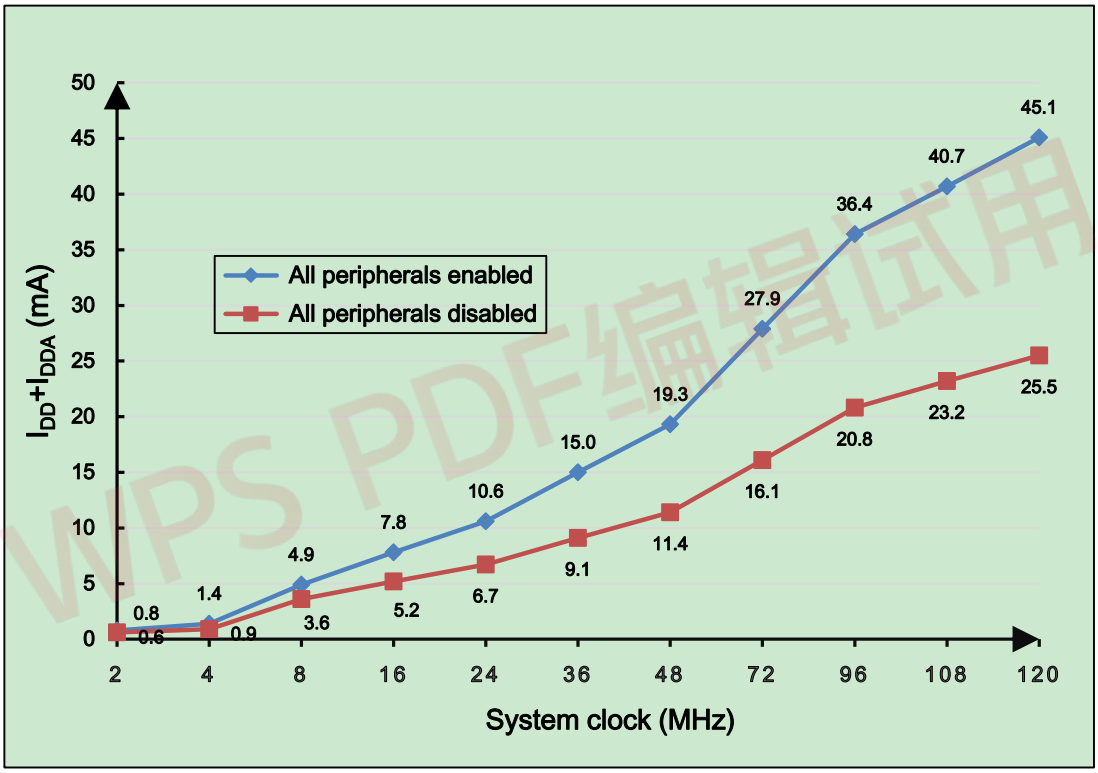


Figure 4-3. Typical supply current consumption in Sleep mode

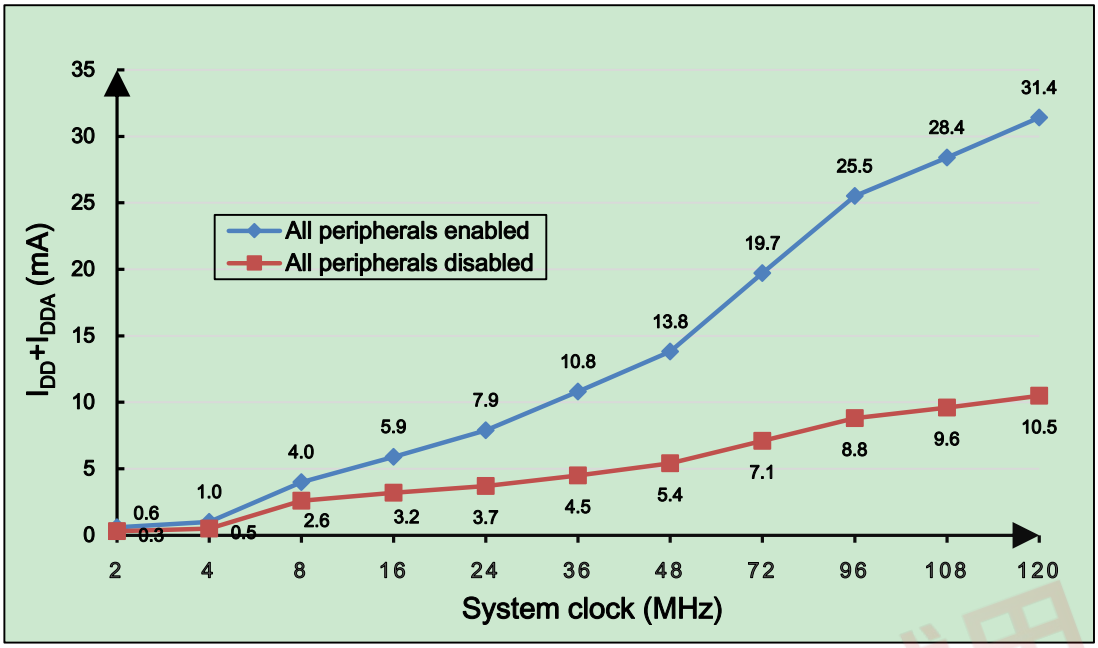


Table 4-8. Peripheral current consumption characteristics(1)

Peripherials(4)		Typical consumption at T_A = 25 ℃ (TYP)	Unit
APB1	DAC(2)	0.81	mA
	PMU	1.41	
	BKP	1.93	
	CAN1	1.39	
	CAN0	1.41	
	I2C1	1.23	
	I2C0	1.21	
	UART4	1.24	
	UART3	1.25	
	USART2	1.23	
	USART1	1.24	
	SPI2	1.17	
	SPI1	1.23	
	WWDGT	1.13	
	TIMER13	1.47	
	TIMER12	1.44	
	TIMER11	1.47	
	TIMER6	1.14	
	TIMER5	1.12	
	TIMER4	1.52	
	TIMER3	2.25	
	TIMER2	2.23	

Peripherials(4)		Typical consumption at T_A = 25 ℃ （TYP）	Unit
	TIMER1	2.25	
ADDAPB1	CTC	1.13	
APB2	TIMER10	2.25	
	TIMER9	2.23	
	TIMER8	2.24	
	USART0	2.15	
	TIMER7	2.66	
	SPI0	1.87	
	TIMER0	2.63	
	ADC1(3)	0.8	
	ADC0(3)	0.8	
	GPIOG	1.99	
	GPIOF	2	
	GPIOE	1.99	
	GPIOD	2	
	GPIOC	2	
	GPIOB	2	
	GPIOA	1.29	
AHB	ENET	5.04	
	USBFS	3.58	
	EXMC	2.59	
	CRC	1.81	
	DMA1	1.48	
	DMA0	1.61	

(1). Based on characterization, not tested in production.

(2). DEN0 and DEN1 bits in the DAC_CTL register are set to 1, and the converted value set to 0x800.

(3). system clock = f_{HCLK} = 120 Mhz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}, f_{ADCCLK} = f_{APB2}/2, ADON bit is set to 1.

(4). If there is no other description, then HXTAL = 25 MHz, system clock = f_{HCLK} = 120 MHz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}.

4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in ***Table 4-9. EMS characteristics***, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-9. EMS characteristics(1)

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C LQFP144, f_{HCLK} = 120 MHz conforms to IEC 61000-4-2	3A
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	V_{DD} = 3.3 V, T_A = 25 °C LQFP144, f_{HCLK} = 120 MHz conforms to IEC 61000-4-4	4A

(1). Based on characterization, not tested in production.

4.5. Power supply supervisor characteristics

Table 4-10. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}(1)	Low voltage Detector level selection	LVDT<2:0> = 000(rising edge)	—	2.15	—	V
		LVDT<2:0> = 000(falling edge)	—	2.04	—	
		LVDT<2:0> = 001(rising edge)	—	2.29	—	
		LVDT<2:0> = 001(falling edge)	—	2.19	—	
		LVDT<2:0> = 010(rising edge)	—	2.43	—	
		LVDT<2:0> = 010(falling edge)	—	2.33	—	
		LVDT<2:0> = 011(rising edge)	—	2.57	—	
		LVDT<2:0> = 011(falling edge)	—	2.47	—	
		LVDT<2:0> = 100(rising edge)	—	2.71	—	
		LVDT<2:0> = 100(falling edge)	—	2.6	—	
		LVDT<2:0> = 101(rising edge)	—	2.85	—	
		LVDT<2:0> = 101(falling edge)	—	2.74	—	
		LVDT<2:0> = 110(rising edge)	—	2.99	—	
		LVDT<2:0> = 110(falling edge)	—	2.89	—	
		LVDT<2:0> = 111(rising edge)	—	3.13	—	
		LVDT<2:0> = 111(falling edge)	—	3.03	—	
$V_{LVDhyst}$(2)	LVD hystersis	—	—	100	—	mV
V_{POR}(1)	Power on reset threshold	—	—	2.34	—	V
V_{PDR}(1)	Power down reset threshold		—	1.82	—	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PDRhyst}$(2)	PDR hysteresis		—	600	—	mV
$t_{RSTTEMPO}$(2)	Reset temporization		—	2	—	ms

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-11. ESD characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25 °C; JESD22-A114	—	—	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=25 °C; JESD22-C101	—	—	800	V

(1). Based on characterization, not tested in production.

Table 4-12. Static latch-up characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A=25 °C; JESD78	—	—	±200	mA
	V_{supply} over voltage		—	—	5.4	V

(1). Based on characterization, not tested in production.

4.7. External clock characteristics

Table 4-13. High speed external clock (HXTAL) generated from a crystal/ceramic

characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}(1)	Crystal or ceramic frequency	2.6 V ≤ V_{DD} ≤ 3.6 V	4	8	32	MHz
R_F(2)	Feedback resistor	V_{DD} = 3.3 V	—	400	—	kΩ
C_{HXTAL}(2) (3)	Recommended load capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Ducy_{(HXTAL)}$(2)	Crystal or ceramic duty cycle	—	30	50	70	%
g_m(2)	Oscillator transconductance	Startup	—	25	—	mA/V
$I_{DDHXTAL}$(1)	Crystal or ceramic operating current	V_{DD} = 3.3 V, f_{HCLK} = f_{IRC8M} = 8 MHz T_A = 25 °C	—	1.25	—	mA
$t_{SUHXTAL}$(1)	Crystal or ceramic startup time	V_{DD} = 3.3 V, f_{HCLK} = f_{IRC8M} = 8 MHz T_A = 25 °C	—	1.8	—	ms

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

(3). C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S), For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

Table 4-14. High speed external clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}(1)	External clock source or oscillator frequency	2.6 V ≤ V_{DD} ≤ 3.6 V	1	—	50	MHz
V_{HXTALH}(2)	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
V_{HXTALL}(2)	OSCIN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	V
$t_{H/L(HXTAL)}$ (2)	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$ (2)	OSCIN rise or fall time	—	—	—	10	ns
C_{IN}(2)	OSCIN input capacitance	—	—	5	—	pF
$Ducy_{(HXTAL)}$ (2)	Duty cycle	—	40	—	60	%

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

Table 4-15. Low speed external clock (LXTAL) generated from a crystal/ceramic

characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}(1)	Crystal or ceramic frequency	V_{DD} = 3.3 V	—	32.768	—	kHz
C_{LXTAL}(2)(3)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	10	—	pF
$Ducy_{(LXTAL)}$(2)	Crystal or ceramic duty cycle	—	30	—	70	%
g_m(2)	Oscillator transconductance	Lower driving capability	—	4	—	μA/V
		Medium low driving capability	—	6	—	
		Medium high driving capability	—	12	—	
		Higher driving capability	—	18	—	
$I_{DDLXTAL}$(1)	Crystal or ceramic operating current	LXTALDRI[1:0] = 00	—	0.7	—	μA
		LXTALDRI[1:0] = 01	—	0.8	—	
		LXTALDRI[1:0] = 10	—	1.0	—	
		LXTALDRI[1:0] = 11	—	1.3	—	
$t_{SULXTAL}$(1)(4)	Crystal or ceramic startup time	—	—	1.8	—	s

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

(3). $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(4). $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

Table 4-16. Low speed external user clock characteristics (LXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}(1)	External clock source or oscillator frequency	V_{DD} = 3.3 V	—	32.768	1000	kHz
V_{LXTALH}(2)	OSC32IN input pin high level voltage	—	0.7 V_{DD}	—	V_{DD}	V
V_{LXTALL}(2)	OSC32IN input pin low level voltage	—	V_{SS}	—	0.3 V_{DD}	
$t_{H/L(LXTAL)}$ (2)	OSC32IN high or low time	—	450	—	—	ns
$t_{R/F(LXTAL)}$ (2)	OSC32IN rise or fall time	—	—	—	50	
C_{IN}(2)	OSC32IN input capacitance	—	—	5	—	pF
$Ducy_{(LXTAL)}$ (2)	Duty cycle	—	30	50	70	%

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

4.8. Internal clock characteristics

Table 4-17. High speed internal clock (IRC8M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	High Speed Internal Oscillator (IRC8M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	8	—	MHz
ACC_{IRC8M}	IRC8M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C(1)	-2.5	—	+2.5	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 0 °C ~ +85 °C(1)	-1.8	—	+1.8	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-1.0	—	+1.0	%
	IRC8M oscillator Frequency accuracy, User trimming step(1)	—	—	0.5	—	%
$Ducy_{IRC8M}$(2)	IRC8M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC8M}$(1)	IRC8M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 120 MHz	—	66	—	µA
$t_{SUIRC8M}$(1)	IRC8M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 120 MHz	—	5	—	µs

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

Table 4-18. Low speed internal clock (IRC40K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC40K}(1)	Low Speed Internal oscillator (IRC40K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C	20	40	45	kHz
$I_{DDAIRC40K}$(2)	IRC40K oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 120 MHz T_A = 25 °C	—	0.4	—	µA
$t_{SUIRC40K}$(2)	IRC40K oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 120 MHz T_A = 25 °C	—	110	—	µs

(1). Guaranteed by design, not tested in production.

(2). Based on characterization, not tested in production.

Table 4-19. High speed internal clock (IRC48M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD} = 3.3 V	—	48	—	MHz
ACC_{IRC48M}	IRC48M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C(1)	-4.0	—	+5.0	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 0 °C ~ +85 °C (1)	-3.0	—	+3.0	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-2.0	—	+2.0	%
	IRC48M oscillator Frequency accuracy, User trimming step(1)	—	—	0.12	—	%
D_{IRC48M}(2)	IRC48M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC48M}$(1)	IRC48M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 120 MHz	—	356	—	μA
$t_{SUIRC48M}$(1)	IRC48M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 120 MHz	—	2.7	—	μs

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

4.9. PLL characteristics

Table 4-20. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	1	—	25	MHz
f_{PLLOUT}	PLL output clock frequency	—	16	—	120	MHz
f_{VCO}	PLL VCO output clock frequency	—	32	—	240	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	300	μs
I_{DDA}(1)(3)	Current consumption on V_{DDA}	VCO freq = 240 MHz	—	680	—	μA
$Jitter_{PLL}$(1)(4)	Cycle to cycle Jitter（rms）	System clock	—	35	—	ps
	Cycle to cycle Jitter（peak to peak）		—	371	—	

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

(3). System clock = IRC8M = 8 MHz, PLL clock source = IRC8M/2 = 4 MHz, f_{PLLOUT} = 120 MHz.

(4). Value given with main PLL running.

Table 4-21. PLL1 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	1	—	25	MHz
f_{PLLOUT}	PLL output clock frequency	—	16	—	120	MHz
f_{VCO}	PLL VCO output clock frequency	—	32	—	200	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	300	μs
I_{DDA}(1)(3)	Current consumption on V_{DDA}	VCO freq = 200 MHz	—	520	—	μA
$Jitter_{PLL}$(1)(4)	Cycle to cycle Jitter	System clock	—	371	—	ps

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

(3). System clock = IRC8M = 8 MHz, PLL1 clock source = IRC48M = 48 MHz, f_{PLLOUT} = 120 MHz.

(4). Value given with main PLL running.

Table 4-22. PLL2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	1	—	25	MHz
f_{PLLOUT}	PLL output clock frequency	—	16	—	120	MHz
f_{VCO}	PLL VCO output clock frequency	—	32	—	200	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	300	μs
I_{DDA}(1)(3)	Current consumption on V_{DDA}	VCO freq = 200 MHz	—	520	—	μA
$Jitter_{PLL}$(1)(4)	Cycle to cycle Jitter	System clock	—	371	—	ps

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

(3). System clock = IRC8M = 8 MHz, PLL2 clock source = IRC48M = 48 MHz, f_{PLLOUT} = 120 MHz.

(4). Value given with main PLL running.

4.10. Memory characteristics

Table 4-23. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(2)	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A = -40 °C ~ +85 °C	100	—	—	kcycles
t_{RET}	Data retention time	—	—	20	—	years
t_{PROG}	Word programming time	T_A = -40 °C ~ +85 °C	—	37.5	86	μs
t_{ERASE}	Page erase time	T_A = -40 °C ~ +85 °C	—	45	200/300(3)	ms
$t_{MERASE(256K)}$	Mass erase time	T_A = -40 °C ~ +85 °C	—	1	4.8/8.0(4)	s
$t_{MERASE(512K)}$	Mass erase time	T_A = -40 °C ~ +85 °C	—	4	19.2/32(5)	s
$t_{MERASE(1MB)}$	Mass erase time	T_A = -40 °C ~ +85 °C	—	6	28.8/48(6)	s

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

(3). Max value with <50K cycles is 200 ms and >50K & <100K cycles is 300 ms.

(4). Max value with <50K cycles is 4.8 s and >50K & <100K cycles is 8.0 s.
(5). Max value with <50K cycles is 19.2 s and >50K & <100K cycles is 32 s.
(6). Max value with <50K cycles is 28.8 s and >50K & <100K cycles is 48 s.

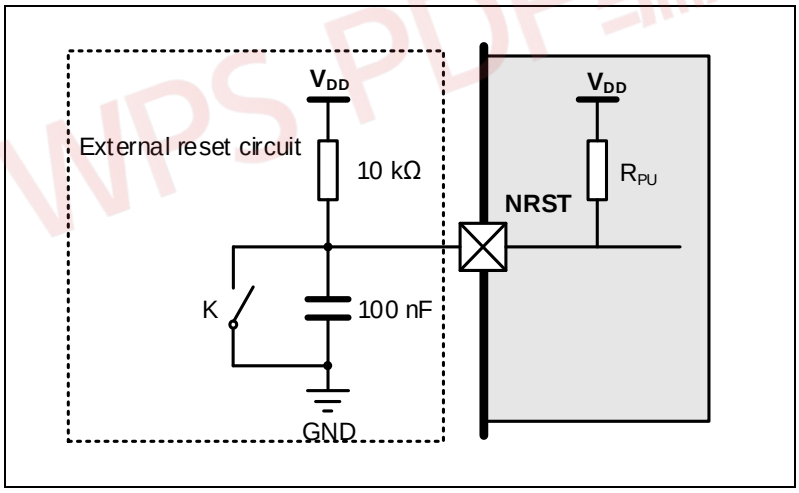
4.11. NRST pin characteristics

Table 4-24. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 2.6 V	-0.5	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.5	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	390	—	mV
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.3 V	-0.5	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.5	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	410	—	mV
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.6 V	-0.5	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.5	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	430	—	mV
R_{pu}(2)	Pull-up equivalent resistor	—	—	40	—	kΩ

(1). Based on characterization, not tested in production.
(2). Guaranteed by design, not tested in production.

Figure 4-4. Recommended external NRST pin circuit



4.12. GPIO characteristics

Table 4-25. I/O port DC characteristics(1) (3)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage		2.6 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	0.3 V_{DD}	V
	5V-tolerant IO Low level input voltage		2.6 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	0.3 V_{DD}	V
V_{IH}	Standard IO Low level input voltage		2.6 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	0.7 V_{DD}	—	—	V
	5V-tolerant IO Low level input voltage		2.6 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	0.7 V_{DD}	—	—	V
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)		V_{DD} = 2.6V	—	—	0.17	V
			V_{DD} = 3.3 V	—	—	0.16	
			V_{DD} = 3.6V	—	—	0.15	
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +20 mA)		V_{DD} = 2.6V	—	—	0.49	V
			V_{DD} = 3.3 V	—	—	0.4	
			V_{DD} = 3.6V	—	—	0.34	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8 mA)		V_{DD} = 2.6V	2.4	—	—	V
			V_{DD} = 3.3 V	3.15	—	—	
			V_{DD} = 3.6V	3.44	—	—	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +20 mA)		V_{DD} = 2.6V	2.02	—	—	V
			V_{DD} = 3.3 V	2.8	—	—	
			V_{DD} = 3.6V	3.15	—	—	
R_{PU}(2)	Internal pull-up resistor	All pins	V_{IN} = V_{SS}	30	40	50	kΩ
		PA10	—	7.5	10	13.5	
R_{PD}(2)	Internal pull-down resistor	All pins	V_{IN} = V_{DD}	30	40	50	kΩ
		PA10	—	7.5	10	13.5	

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

(3). All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current, the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode(maximum load: 30 pF).

Table 4-26. I/O port AC characteristics(1)(2)

GPIOx_MDy[1:0] bit value(3)	Parameter	Conditions	Max	Unit
GPIOx_CTL->MDy[1:0]=10 （IO_Speed = 2MHz）	Maximum frequency(4)	2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	15	MHz
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	10	
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	8	
GPIOx_CTL->MDy[1:0] = 01 （IO_Speed = 10MHz）	Maximum frequency(4)	2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	50	MHz
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	25	
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	15	
GPIOx_CTL->MDy[1:0]=11	Maximum	2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	100	MHz

GPIOx_MDy[1:0] bit value(3)	Parameter	Conditions	Max	Unit
（IO_Speed = 50MHz）	frequency(4)	2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	70	
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	50	
GPIOx_CTL->MDy[1:0]=11 and GPIOx_SPDy=1 （IO_Speed = MAX）	Maximum frequency(4)	2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	120	MHz
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	100	
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	60	

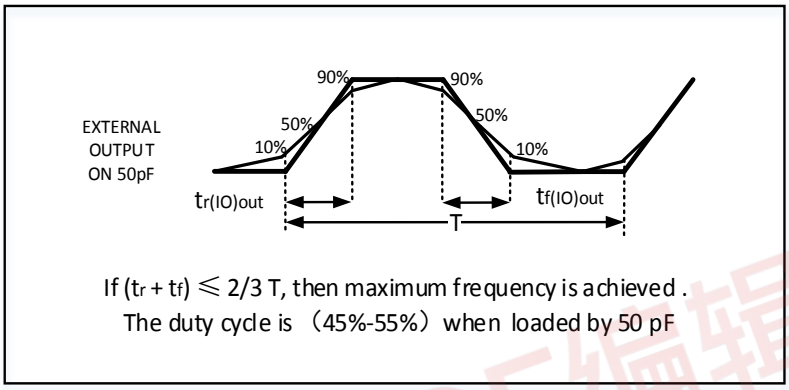
(1). Based on characterization, not tested in production.

(2). Unless otherwise specified, all test results given for T_A = 25 ℃.

(3). The I/O speed is configured using the GPIOx_CTL -> MDy[1:0] bits. Refer to the GD32F 30x user manual which is selected to set the GPIO port output speed.

(4). The maximum frequency is defined in Figure 4-5, and maximum frequency cannot exceed 120 MHz.

Figure 4-5. I/O port AC characteristics definition



4.13. Temperature sensor characteristics

Table 4-27. Temperature sensor characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	—	±1.5	—	℃
Avg_Slope	Average slope	—	4.1	—	mV/℃
V_{25}	Voltage at 25 °C	—	1.45	—	V
t_{S_temp} (2)	ADC sampling time when reading the temperature	—	17.1	—	μs

(1). Based on characterization, not tested in production.

(2). Shortest sampling time can be determined in the application by multiple iterations.

4.14. ADC characteristics

Table 4-28. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	2.6	3.3	3.6	V
V_{IN}(1)	ADC input voltage range	—	0	—	V_{REF+}	V
V_{REF+}(2)	Positive Reference Voltage	—	2.4	—	V_{DDA}	V
V_{REF-}(2)	Negative Reference Voltage	—	—	V_{SSA}	—	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}(1)	ADC clock	—	0.1	—	40	MHz
f_S(1)	Sampling rate	12-bit	0.007	—	2.86	MSPS
		10-bit	0.008	—	3.33	
		8-bit	0.01	—	4	
		6-bit	0.012	—	5	
V_{AIN}(1)	Analog input voltage	16 external; 2 internal	0	—	V_{DDA}	V
R_{AIN}(2)	External input impedance	See ***Equation 1***	—	—	32.9	kΩ
R_{ADC}(2)	Input sampling switch resistance	—	—	—	0.55	kΩ
C_{ADC}(2)	Input sampling capacitance	No pin/pad capacitance included	—	—	5.5	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 40 MHz	—	3.275	—	μs
t_s(2)	Sampling time	f_{ADC} = 40 MHz	0.0375	—	5.99	μs
t_{CONV}(2)	Total conversion time(including sampling time)	12-bit	—	14	—	1/f_{ADC}
		10-bit	—	12	—	
		8-bit	—	10	—	
		6-bit	—	8	—	
t_{SU}(2)	Startup time	—	—	—	1	μs

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

Equation 1: R_{AIN} max formula $R_{AIN} < \frac{T_S}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-29. ADC $R_{AIN\ max}$ for f_{ADC} = 40 MHz

T_s (cycles)	t_s (μs)	$R_{AIN\ max}$ (kΩ)
1.5	0.0375	0.15
7.5	0.1875	2.96
13.5	0.3375	5.77
28.5	0.7125	12.8
41.5	1.0375	18.9
55.5	1.3875	25.4
71.5	1.7875	32.9
239.5	5.9875	N/A

Table 4-30. ADC dynamic accuracy at f_{ADC} = 14 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 14 MHz	—	10.8	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA} = V_{REF+} = 3.3 V	—	66.7	—	dB
SNR	Signal-to-noise ratio	Input Frequency = 20 kHz	—	67.4	—	
THD	Total harmonic distortion	Temperature = 25 ℃	—	-76.3	—	

(1). Based on characterization, not tested in production.

Table 4-31. ADC dynamic accuracy at f_{ADC} = 40 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 40 MHz	—	10	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA} = V_{REF+} = 3.3 V	—	62	—	dB
SNR	Signal-to-noise ratio	Input Frequency = 20 kHz	—	62.2	—	
THD	Total harmonic distortion	Temperature = 25 ℃	—	-68.6	—	

(1). Based on characterization, not tested in production.

Table 4-32. ADC static accuracy at f_{ADC} = 14 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 14 MHz V_{DDA} = V_{REF+} = 3.3 V	±1	—	LSB
DNL	Differential linearity error		±0.9	—	
INL	Integral linearity error		±1	—	

(1). Based on characterization, not tested in production.

4.15. DAC characteristics

Table 4-33. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	2.6	3.3	3.6	V
V_{REF+}(2)	Positive Reference Voltage	—	2.4	—	V_{DDA}	V
V_{REF-}(2)	Negative Reference Voltage	—	—	V_{SSA}	—	V
R_{LOAD}(2)	Load resistance	Resistive load with buffer ON	5	—	—	kΩ
Ro(2)	Impedance output with buffer OFF	—	—	—	15	kΩ
C_{LOAD}(2)	Load capacitance	No pin/pad capacitance included	—	—	50	pF
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	—	0.2	—	—	V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	—	—	—	V_{DDA}-0.2	V
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF	—	—	0.5	—	mV
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF	—	—	—	V_{DDA}-1LSB	V
I_{DDA}(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REF+} = 3.6 V	—	470	—	uA
		With no load, worst code(0xF1C) on the input, V_{REF+} = 3.6 V	—	500	—	uA
$I_{DDVREF+}$(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REF+} = 3.6 V	—	86	—	uA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		With no load, worst code(0xF1C) on the input, V_{REF+} = 3.6 V	—	298	—	uA
DNL(1)	Differential non-linearity error	DAC in 12-bit mode	—	—	±3	LSB
INL(1)	Integral non-linearity	DAC in 12-bit mode	—	—	±4	LSB
Offset(1)	Offset error	DAC in 12-bit mode	—	—	±12	LSB
GE(1)	Gain error	DAC in 12-bit mode	—	—	±0.5	%
$T_{setting}$(1)	Settling time	$C_{LOAD} \leqslant$ 50 pF, $R_{LOAD} \geqslant$ 5 kΩ	—	0.3	1	μs
T_{wakeup}(2)	Wakeup from off state	—	—	5	10	μs
Update rate(2)	Max frequency for a correct DAC_OUT change from code i to i±1LSBs	$C_{LOAD} \leqslant$ 50 pF, $R_{LOAD} \geqslant$ 5 kΩ	—	—	4	MS/s
PSRR(2)	Power supply rejection ratio (to V_{DDA})	—	55	80	—	dB

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

4.16. I2C characteristics

Table 4-34. I2C characteristics(1)(2)(3)

Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{su(SDA)}$	SDA setup time	—	2	—	0.8		0.1	—	ns
$t_{h(SDA)}$	SDA data hold time	—	250	—	250	—	130	—	ns
$t_{r(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	20	300	—	120	ns
$t_{f(SDA/SCL)}$	SDA and SCL fall time	—	4	300	4	300	4	120	ns
$t_{h(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs

(1). Guaranteed by design, not tested in production.

(2). To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz, To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3). The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

4.17. SPI characteristics

Table 4-35. Standard SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	30	MHz
$t_{SCK(H)}$	SCK clock high time	Master mode, f_{PCLKx} = 120 MHz, presc = 8	31.83	33.33	34.83	ns
$t_{SCK(L)}$	SCK clock low time	Master mode, f_{PCLKx} = 120 MHz, presc = 8	31.83	33.33	34.83	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	5	6	ns
$t_{H(MO)}$	Data output hold time	—	3	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	1	—	—	ns
$t_{H(MI)}$	Data input hold time	—	0	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	0	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	1	—	—	ns
$t_{A(SO)}$	Data output access time	—	5	—	9	ns
$t_{DIS(SO)}$	Data output disable time	—	6	—	10	ns
$t_{V(SO)}$	Data output valid time	—	—	10	12	ns
$t_{H(SO)}$	Data output hold time	—	8	—	—	ns
$t_{SU(SI)}$	Data input setup time	—	0	—	—	ns
$t_{H(SI)}$	Data input hold time	—	1	—	—	ns

(1). Based on characterization, not tested in production.

4.18. I2S characteristics

Table 4-36. I2S characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 16 bits, Audio frequency = 96 kHz)	3.075	3.077	3.079	MHz
		Slave mode	0	—	10	
t_H	Clock high time	—	162	—	—	ns
t_L	Clock low time		163	—	—	ns
$t_{V(WS)}$	WS valid time	Master mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Master mode	0	—	—	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Slave mode	2	—	—	ns
$Ducy_{(SCK)}$	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD\_MR)}$	Data input setup time	Master mode	1	—	—	ns
$t_{su(SD\_SR)}$	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD\_MR)}$	Data input hold time	Master receiver	0	—	—	ns
$t_{H(SD\_SR)}$		Slave receiver	1	—	—	ns
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	—	—	12	ns
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	7	—	—	ns
$t_{v(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	—	—	6	ns
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	2	—	—	ns

(1). Guaranteed by design, not tested in production.

(2). Based on characterization, not tested in production

4.19. USART characteristics

Table 4-37. USART characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 120 MHz	—	—	60	MHz
$t_{SCK(H)}$	SCK clock high time	f_{PCLKx} = 120 MHz	7.5	—	—	ns
$t_{SCK(L)}$	SCK clock low time	f_{PCLKx} = 120 MHz	7.5	—	—	ns

(1). Guaranteed by design, not tested in production.

4.20. CAN characteristics

Refer to ***Table 4-25. I/O port DC characteristics***(1) for more details on the input/output alternate function characteristics (CANTX and CANRX).

4.21. USBFS characteristics

Table 4-38. USBFS start up time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USBFS startup time	1	μs

(1). Guaranteed by design, not tested in production.

Table 4-39. USBFS DC electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
Input levels(1)	V_{DD}	USBFS operating voltage	—	3	—	3.6	V
	V_{DI}	Differential input sensitivity	—	0.2	—	—	
	V_{CM}	Differential common mode range	Includes V_{DI} range	0.8	—	2.5	
	V_{SE}	Single ended receiver threshold	—	1.3	—	2.0	
Output levels (2)	V_{OL}	Static output level low	R_L of 1.0 kΩ to 3.6 V	—	0.064	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to VSS	2.8	3.3	3.6	
R_{PD}(2)		PA11, PA12(USB_DM/DP)	V_{IN} = V_{DD}	17	20.574	24	kΩ
		PA9(USB_VBUS)		0.65	—	2.0	
R_{PU}(2)		PA11, PA12(USB_DM/DP)	V_{IN} = V_{SS}	1.5	1.585	2.1	
		PA9(USB_VBUS)		0.25	0.326	0.55	

(1). Guaranteed by design, not tested in production.

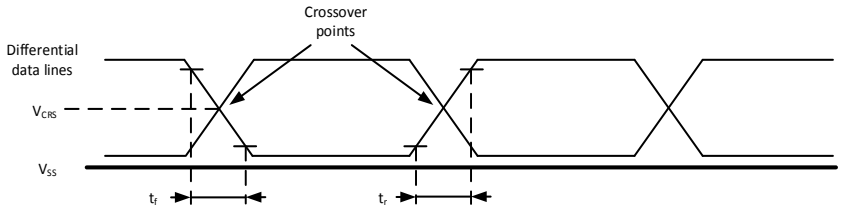
(2). Based on characterization, not tested in production.

Table 4-40. USBFS full speed-electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_R	Rise time	C_L = 50 pF	4	—	20	ns
t_F	Fall time	C_L = 50 pF	4	—	20	ns
t_{RFM}	Rise/fall time matching	t_R / t_F	90	—	110	%
V_{CRS}	Output signal crossover voltage	—	1.3	—	2.0	V

(1). Guaranteed by design, not tested in production.

Figure 4-6. USBFS timings: definition of data signal rise and fall time



4.22. EXMC characteristics

Table 4-41. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	40.5	42.5	ns
$t_{V(NOE\_NE)}$	EXMC_NEx low to EXMC_NOE low	0	—	ns
$t_{w(NOE)}$	EXMC_NOE low time	40.5	42.5	ns
$t_{h(NE\_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{su(DATA\_NE)}$	Data to EXMC_NEx high setup time	32.2	—	ns
$t_{su(DATA\_NOE)}$	Data to EXMC_NOEx high setup time	32.2	—	ns
$t_{h(DATA\_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA\_NE)}$	Data hold time after EXMC_NEx high	0	—	ns
$t_{v(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	7.3	9.3	ns

(1). C_L = 30 pF.
(2). Guaranteed by design, not tested in production.
(3). Based on characterization, not tested in production.
(4). Based on configure: f_{HCLK} = 120 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-42. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	23.9	25.9	ns
$t_{V(NWE\_NE)}$	EXMC_NEx low to EXMC_NWE low	7.3	—	ns
$t_{w(NWE)}$	EXMC_NWE low time	7.3	9.3	ns
$t_{h(NE\_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	7.3	9.3	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	7.3	9.3	ns
$t_{h(AD\_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	15.6	—	ns
$t_{h(A\_NWE)}$	Address hold time after EXMC_NWE high	7.3	—	ns
$t_{h(BL\_NWE)}$	EXMC_BL hold time after EXMC_NWE high	7.3	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	23.9	25.9	ns
$t_{v(DATA\_NADV)}$	EXMC_NADV high to DATA valid	7.3	—	ns
$t_{h(DATA\_NWE)}$	Data hold time after EXMC_NWE high	7.3	9.3	ns

(1). C_L = 30 pF.
(2). Guaranteed by design, not tested in production.
(3). Based on characterization, not tested in production.
(4). Based on configure: f_{HCLK} = 120 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-43. Asynchronous multiplexed PSRAM/NOR read timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	57.1	59.1	ns
$t_{V(NOE\_NE)}$	EXMC_NEx low to EXMC_NOE low	23.9	—	ns
$t_{w(NOE)}$	EXMC_NOE low time	32.2	34.2	ns
$t_{h(NE\_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{v(A\_NOE)}$	Address hold time after EXMC_NOE high	0	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{h(BL\_NOE)}$	EXMC_BL hold time after EXMC_NOE high	0	—	ns
$t_{su(DATA\_NE)}$	Data to EXMC_NEx high setup time	33.2	—	ns
$t_{su(DATA\_NOE)}$	Data to EXMC_NOEx high setup time	33.2	—	ns
$t_{h(DATA\_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA\_NE)}$	Data hold time after EXMC_NEx high	0	—	ns
$t_{v(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	7.3	9.3	ns
$T_{h(AD\_NADV)}$	EXMC_AD(adress) valid hold time after EXMC_NADV high	7.3	9.3	ns

(1). C_L = 30 pF.

(2). Guaranteed by design, not tested in production.

(3). Based on characterization, not tested in production.

(4). Based on configure: f_{HCLK} = 120 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-44. Asynchronous multiplexed PSRAM/NOR write timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	40.5	42.5	ns
$t_{V(NWE\_NE)}$	EXMC_NEx low to EXMC_NWE low	7.3	—	ns
$t_{w(NWE)}$	EXMC_NWE low time	23.9	25.9	ns
$t_{h(NE\_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	7.3	—	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	7.3	9.3	ns
$t_{h(AD\_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	7.3	—	ns
$t_{h(A\_NWE)}$	Address hold time after EXMC_NWE high	7.3	—	ns
$t_{h(BL\_NWE)}$	EXMC_BL hold time after EXMC_NWE high	7.3	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{v(DATA\_NADV)}$	EXMC_NADV high to DATA valid	7.3	—	ns
$t_{h(DATA\_NWE)}$	Data hold time after EXMC_NWE high	7.3	—	ns

(1). C_L = 30 pF.

(2). Guaranteed by design, not tested in production.

(3). Based on characterization, not tested in production.

(4). Based on configure: f_{HCLK} = 120 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-45. Synchronous multiplexed PSRAM/NOR read timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	33.2	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	15.6	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	15.6	—	ns
$t_{d(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	15.6	—	ns
$t_{d(CLKL-ADV)}$	EXMC_CLK low to EXMC_AD valid	0	—	ns
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns

(1). C_L = 30 pF.

(2). Guaranteed by design, not tested in production.

(3). Based on characterization, not tested in production.

(4). Based on configure: f_{HCLK} = 120 MHz, BurstAccessMode = Enable; Memory Type = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); Data Latency = 1.

Table 4-46. Synchronous multiplexed PSRAM write timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	33.2	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	15.6	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	15.6	—	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	15.6	—	ns
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1). C_L = 30 pF.

(2). Guaranteed by design, not tested in production.

(3). Based on characterization, not tested in production.

(4). Based on configure: f_{HCLK} = 120 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-47. Synchronous non-multiplexed PSRAM/NOR read timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	33.2	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	15.6	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	15.6	—	ns
$t_{d(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	15.6	—	ns

(1). C_L = 30 pF.

(2). Guaranteed by design, not tested in production.

(3). Based on characterization, not tested in production.

(4). Based on configure: HCLK=120 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-48. Synchronous non-multiplexed PSRAM write timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	33.2	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	15.6	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	15.6	—	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	15.6	—	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1). C_L = 30 pF.

(2). Guaranteed by design, not tested in production.

(3). Based on characterization, not tested in production.

(4). Based on configure: HCLK = 120 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

4.23. TIMER characteristics

Table 4-49. TIMER characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 120 MHz	8.4	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}/2$	MHz
		$f_{TIMERxCLK}$ = 120 MHz	0	60	MHz
RES	Timer resolution	—	—	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 120 MHz	0.0084	546	μs
t_{MAX_COUNT}	Maximum possible count	—	—	65536x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 120 MHz	—	35.7	s

(1). Guaranteed by design, not tested in production.

4.24. WDGT characteristics

Table 4-50. FWDGT min/max timeout period at 40 kHz (IRC40K) (1)

Prescaler divider	PR[2:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.1	409.6	ms
1/8	001	0.2	819.2	
1/16	010	0.4	1638.4	
1/32	011	0.8	3276.8	
1/64	100	1.6	6553.6	
1/128	101	3.2	13107.2	
1/256	110 or 111	6.4	26214.4	

(1). Guaranteed by design, not tested in production.

Table 4-51. WWDGT min-max timeout value at 60 MHz (f_{PCLK1}) (1)

Prescaler divider	PSC[2:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	68.27	μs	4.37	ms
1/2	01	136.53		8.74	
1/4	10	273.07		17.48	
1/8	11	546.13		34.95	

(1). Guaranteed by design, not tested in production.

4.25. Parameter condition

Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25 ℃.

5. Package information

5.1. LQFP144 package outline dimensions

Figure 5-1. LQFP144 package outline

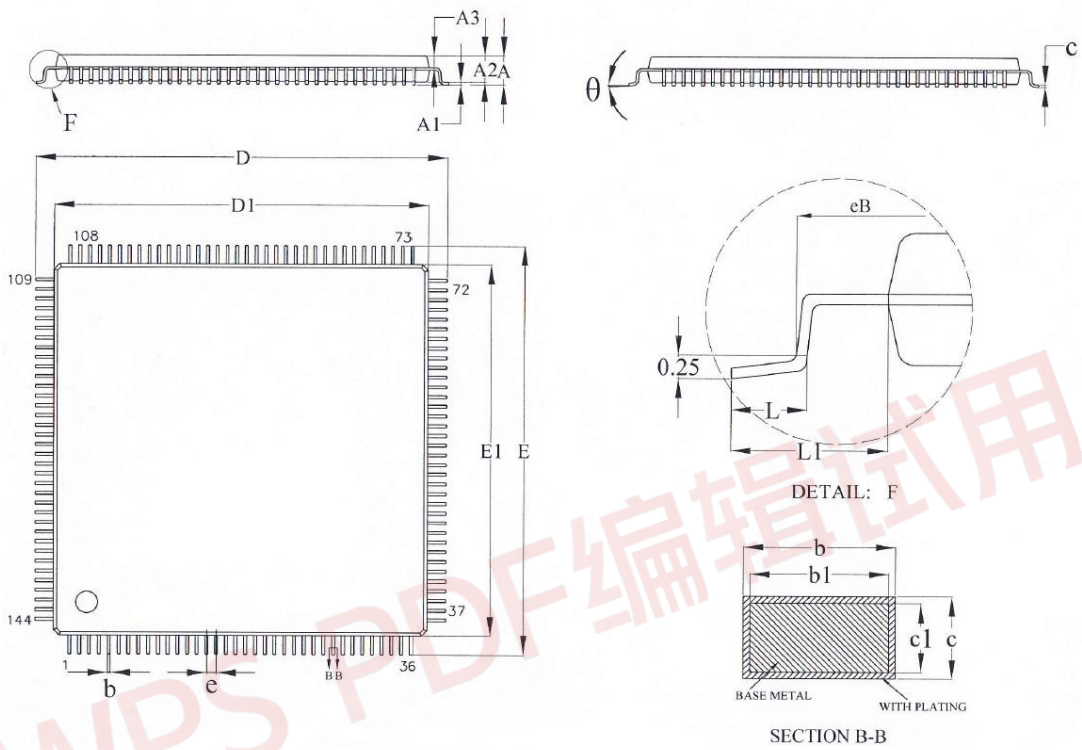


Table 5-1. LQFP144 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
D	21.80	22.0	22.20
D1	19.90	20.0	20.10
E	21.80	22.0	22.20
E1	19.90	20.0	20.10
θ	0°	3.5°	7°
c	0.13	—	0.17
c1	0.12	0.13	0.14
L	0.45	—	0.75
L1	—	1.0 REF	—
b	0.18	—	0.26
b1	0.17	0.20	0.23
e	—	0.50 BSC	—

(Original dimensions are in millimeters)

5.2. LQFP100 package outline dimensions

Figure 5-2. LQFP100 package outline

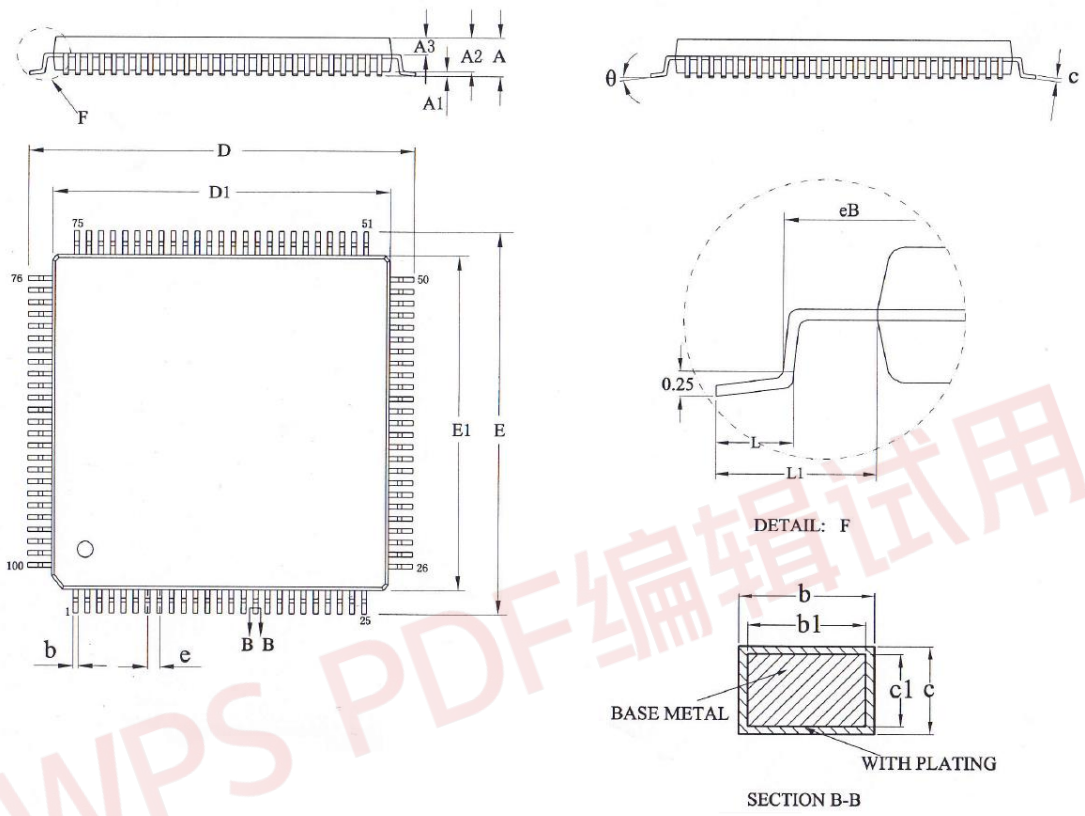


Table 5-2. LQFP100 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
D	15.80	16.0	16.20
D1	13.90	14.0	14.10
E	15.80	16.0	16.20
E1	13.90	14.0	14.10
θ	0°	3.5°	7°
c	0.13	—	0.17
c1	0.12	0.13	0.14
L	0.45	0.6	0.75
L1	—	1.0 REF	—
b	0.18	0.20	0.26
b1	0.17	0.20	0.23

Symbol	Min	Typ	Max
eB	15.05	—	15.35
e	—	0.50 BSC	—

(Original dimensions are in millimeters)

5.3. LQFP64 package outline dimensions

Figure 5-3. LQFP64 package outline

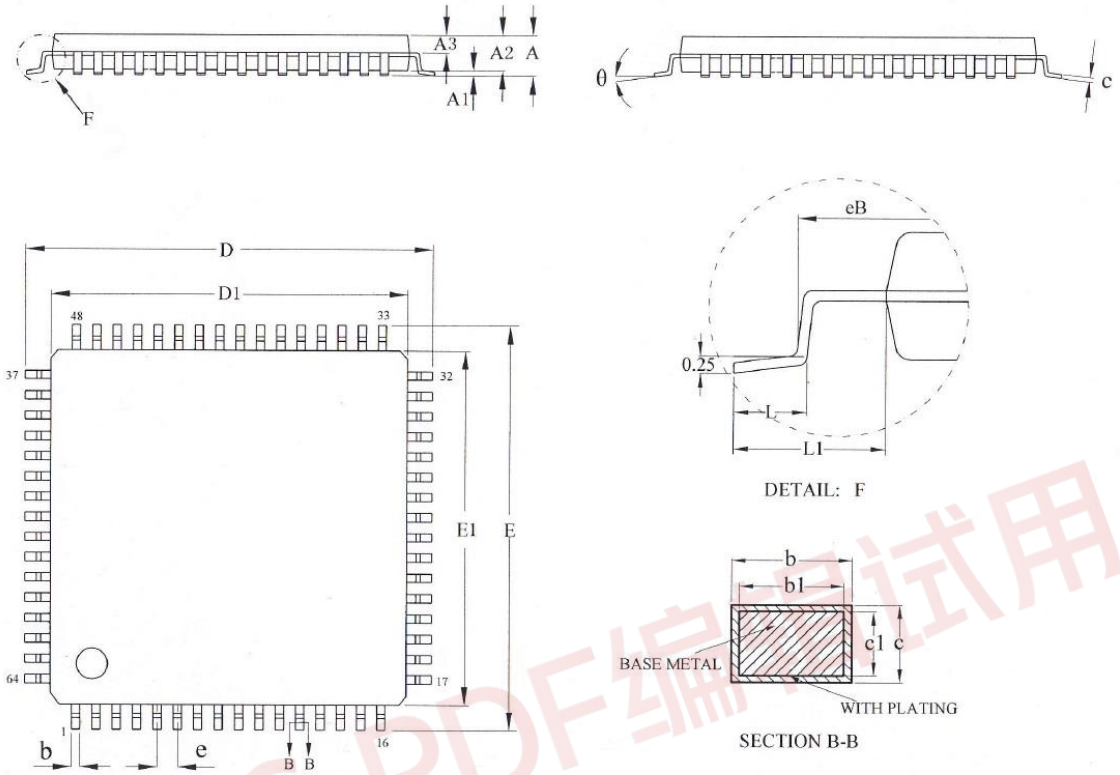


Table 5-3. LQFP64 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
θ	0°	3.5°	7°
c	0.13	—	0.17
L	0.45	0.60	0.75
L1	—	1.00 REF	—
b	0.17	0.20	0.27
e	—	0.50 BSC	—
eB	11.25	—	11.45

(Original dimensions are in millimeters)

6. Ordering information

Table 6-1. Part ordering code for GD32F307xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F307RCT6	256	LQFP64	Green	Industrial -40°C to +85°C
GD32F307RET6	512	LQFP64	Green	Industrial -40°C to +85°C
GD32F307RGT6	1024	LQFP64	Green	Industrial -40°C to +85°C
GD32F307VCT6	256	LQFP100	Green	Industrial -40°C to +85°C
GD32F307VET6	512	LQFP100	Green	Industrial -40°C to +85°C
GD32F307VGT6	1024	LQFP100	Green	Industrial -40°C to +85°C
GD32F307ZCT6	256	LQFP144	Green	Industrial -40°C to +85°C
GD32F307ZET6	512	LQFP144	Green	Industrial -40°C to +85°C
GD32F307ZGT6	1024	LQFP144	Green	Industrial -40°C to +85°C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.20, 2017
1.1	Repair history accumulation error	Jan.24, 2018
1.2	Repair history accumulation error	Dec.16, 2018
1.3	Add functional description of PD0 and PD1 to the packages below 100pin. Update electrical characteristics and package information.	Mar.6.2020

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MachXO2™ Family Data Sheet

DS1035 Version 3.3, March 2017

MachXO2 Family Data Sheet Introduction

May 2016 Data Sheet DS1035

Features

- **Flexible Logic Architecture**
  - Six devices with 256 to 6864 LUT4s and 18 to 334 I/Os
- **Ultra Low Power Devices**
  - Advanced 65 nm low power process
  - As low as 22 µW standby power
  - Programmable low swing differential I/Os
  - Stand-by mode and other power saving options
- **Embedded and Distributed Memory**
  - Up to 240 kbits sysMEM™ Embedded Block RAM
  - Up to 54 kbits Distributed RAM
  - Dedicated FIFO control logic
- **On-Chip User Flash Memory**
  - Up to 256 kbits of User Flash Memory
  - 100,000 write cycles
  - Accessible through WISHBONE, SPI, I^2C and JTAG interfaces
  - Can be used as soft processor PROM or as Flash memory
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated gearing logic
  - 7:1 Gearing for Display I/Os
  - Generic DDR, DDRX2, DDRX4
  - Dedicated DDR/DDR2/LPDDR memory with DQS support
- **High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - PCI
    - LVDS, Bus-LVDS, MLVDS, RSDS, LVPECL
    - SSTL 25/18
    - HSTL 18
    - Schmitt trigger inputs, up to 0.5 V hysteresis
  - I/Os support hot socketing
  - On-chip differential termination
  - Programmable pull-up or pull-down mode
- **Flexible On-Chip Clocking**
  - Eight primary clocks
  - Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
  - Up to two analog PLLs per device with fractional-n frequency synthesis
    - Wide input frequency range (7 MHz to 400 MHz)
- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - Single-chip, secure solution
  - Programmable through JTAG, SPI or I^2C
  - Supports background programming of non-volatile memory
  - Optional dual boot with external SPI memory
- **TransFR™ Reconfiguration**
  - In-field logic update while system operates
- **Enhanced System Level Support**
  - On-chip hardened functions: SPI, I^2C, timer/counter
  - On-chip oscillator with 5.5% accuracy
  - Unique TraceID for system tracking
  - One Time Programmable (OTP) mode
  - Single power supply with extended operating range
  - IEEE Standard 1149.1 boundary scan
  - IEEE 1532 compliant in-system programming
- **Broad Range of Package Options**
  - TQFP, WLCSP, ucBGA, csBGA, caBGA, ftBGA, fpBGA, QFN package options
  - Small footprint package options
    - As small as 2.5 mm x 2.5 mm
  - Density migration supported
  - Advanced halogen-free packaging

Table 1-1. MachXO2™ Family Selection Guide

		XO2-256	XO2-640	XO2-640U[1]	XO2-1200	XO2-1200U[1]	XO2-2000	XO2-2000U[1]	XO2-4000	XO2-7000
LUTs		256	640	640	1280	1280	2112	2112	4320	6864
Distributed RAM (kbits)		2	5	5	10	10	16	16	34	54
EBR SRAM (kbits)		0	18	64	64	74	74	92	92	240
Number of EBR SRAM Blocks (9 kbits/block)		0	2	7	7	8	8	10	10	26
UFM (kbits)		0	24	64	64	80	80	96	96	256
Device Options:	HC[2]	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	HE[3]						Yes	Yes	Yes	Yes
	ZE[4]	Yes	Yes		Yes		Yes		Yes	Yes
Number of PLLs		0	0	1	1	1	1	2	2	2
Hardened Functions:	I2C	2	2	2	2	2	2	2	2	2
	SPI	1	1	1	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1	1	1	1
Packages						**IO**				
25-ball WLCSP[5] (2.5 mm x 2.5 mm, 0.4 mm)					18					
32 QFN[6] (5 mm x 5 mm, 0.5 mm)		21			21					
48 QFN[8, 9] (7 mm x 7 mm, 0.5 mm)		40	40							
49-ball WLCSP[5] (3.2 mm x 3.2 mm, 0.4 mm)							38			
64-ball ucBGA (4 mm x 4 mm, 0.4 mm)		44								
84 QFN[7] (7 mm x 7 mm, 0.5 mm)									68	
100-pin TQFP (14 mm x 14 mm)		55	78		79		79			
132-ball csBGA (8 mm x 8 mm, 0.5 mm)		55	79		104		104		104	
144-pin TQFP (20 mm x 20 mm)				107	107		111		114	114
184-ball csBGA[7] (8 mm x 8 mm, 0.5 mm)									150	
256-ball caBGA (14 mm x 14 mm, 0.8 mm)							206		206	206
256-ball ftBGA (17 mm x 17 mm, 1.0 mm)						206	206		206	206
332-ball caBGA (17 mm x 17 mm, 0.8 mm)									274	278
484-ball ftBGA (23 mm x 23 mm, 1.0 mm)								278	278	334

1. Ultra high I/O device.
2. High performance with regulator – VCC = 2.5 V, 3.3 V
3. High performance without regulator – V_{CC} = 1.2 V
4. Low power without regulator – V_{CC} = 1.2 V
5. WLCSP package only available for ZE devices.
6. 32 QFN package only available for HC and ZE devices.
7. 184 csBGA package only available for HE devices.
8. 48-pin QFN information is ‘Advanced’.
9. 48 QFN package only available for HC devices.

Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I^2C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external V_{CC} supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V_{CC} supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I^2C port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

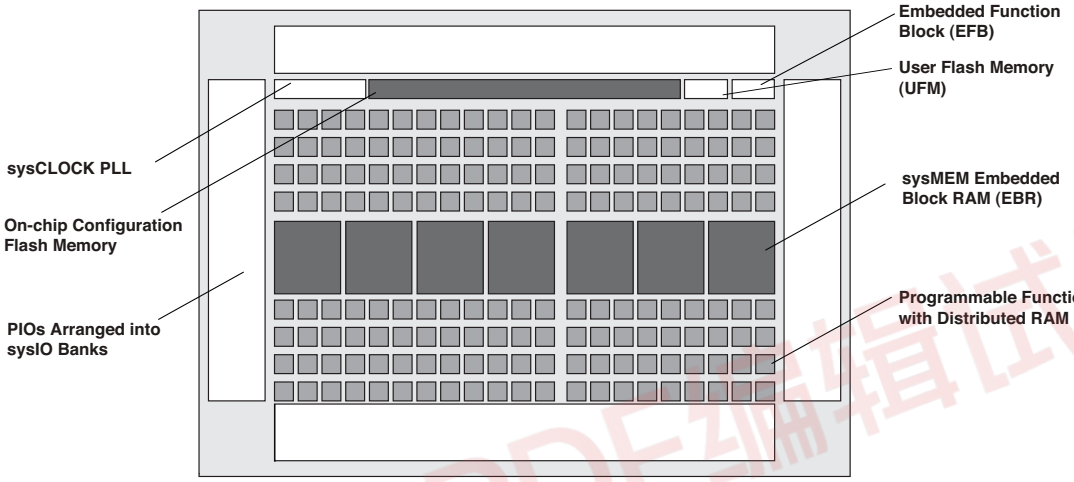
Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

Architecture Overview

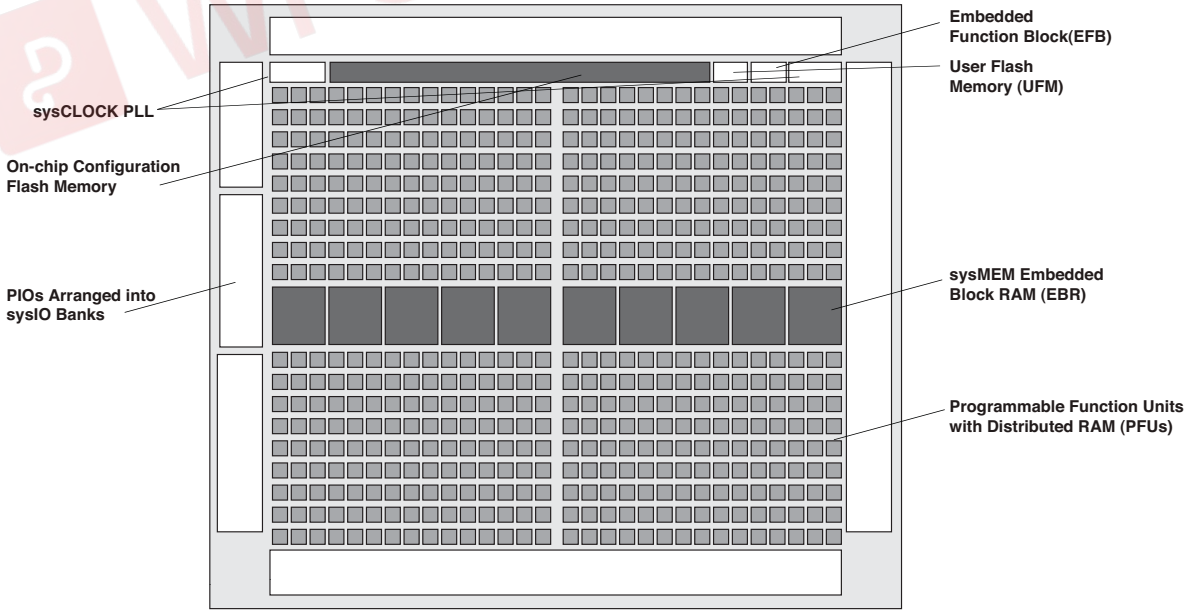
The MachXO2 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.

Figure 2-1. Top View of the MachXO2-1200 Device



Note: MachXO2-256, and MachXO2-640/U are similar to MachXO2-1200. MachXO2-256 has a lower LUT count and no PLL or EBR blocks. MachXO2-640 has no PLL, a lower LUT count and two EBR blocks. MachXO2-640U has a lower LUT count, one PLL and seven EBR blocks.

Figure 2-2. Top View of the MachXO2-4000 Device



Note: MachXO2-1200U, MachXO2-2000/U and MachXO2-7000 are similar to MachXO2-4000. MachXO2-1200U and MachXO2-2000 have a lower LUT count, one PLL, and eight EBR blocks. MachXO2-2000U has a lower LUT count, two PLLs, and 10 EBR blocks. MachXO2-7000 has a higher LUT count, two PLLs, and 26 EBR blocks.

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2-640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

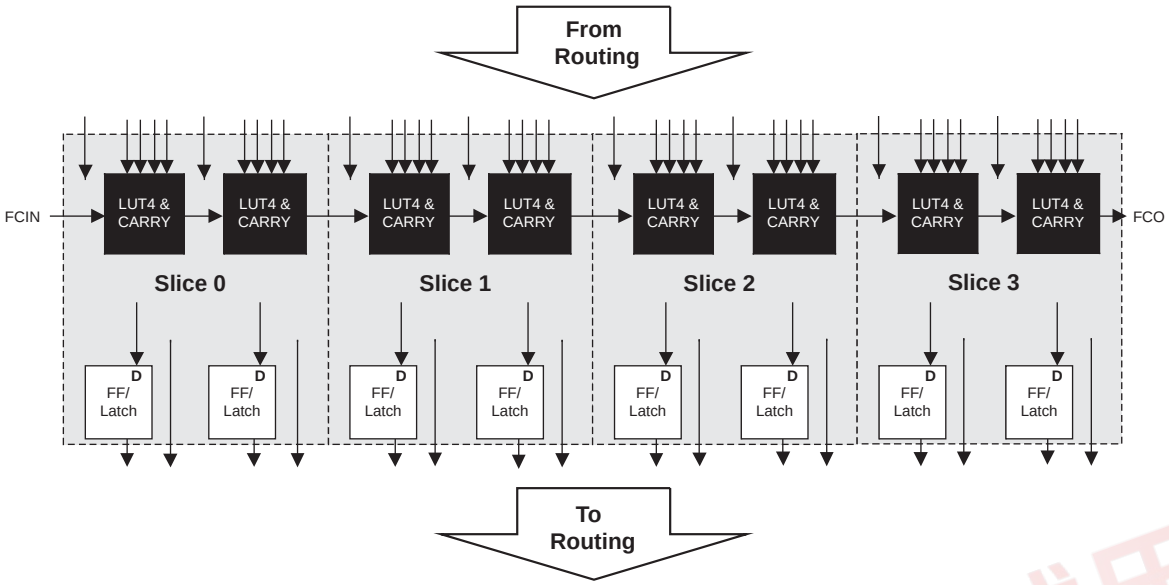
MachXO2 devices provide commonly used hardened functions such as SPI controller, I^2C controller and timer/counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I^2C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

PFU Blocks

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Block Diagram



Slices

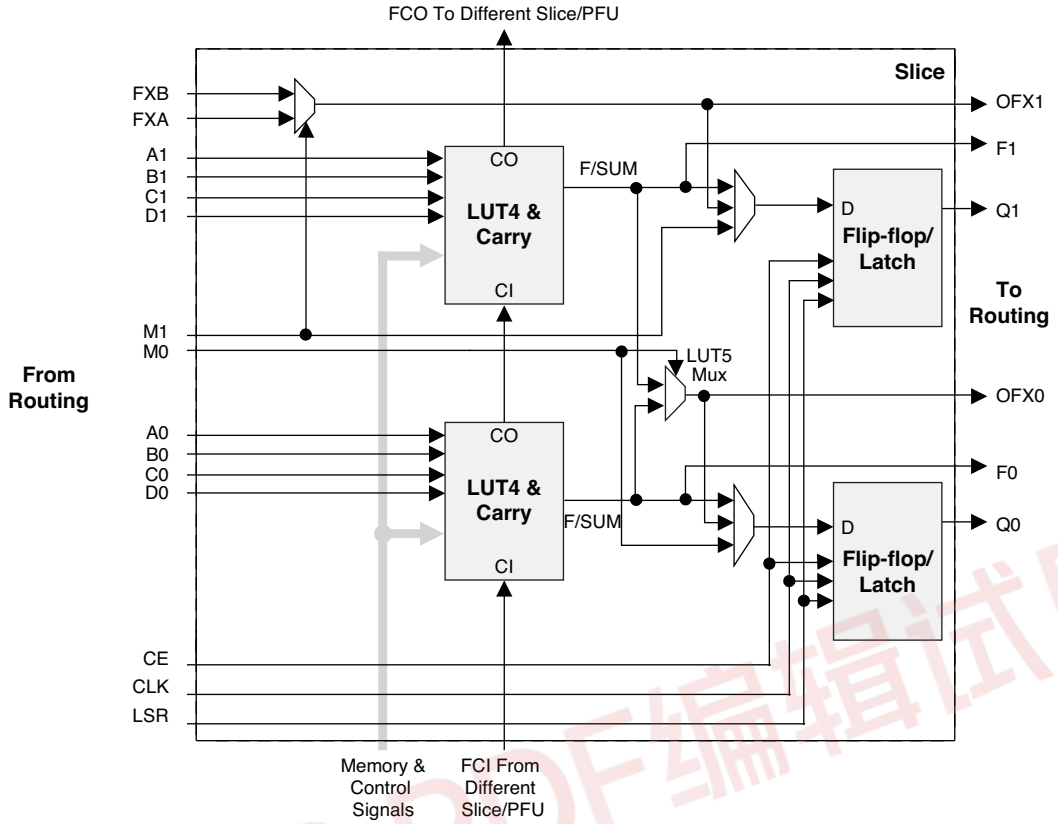
Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU Block	
	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.

Figure 2-4. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multi-purpose input
Input	Control signal	CE	Clock enable
Input	Control signal	LSR	Local set/reset
Input	Control signal	CLK	System clock
Input	Inter-PFU signal	FCIN	Fast carry in[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Fast carry out[1]

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO2 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO2 devices, please see TN1201, Memory Usage Guide for MachXO2 Devices.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

Routing

There are many resources provided in the MachXO2 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Each MachXO2 device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

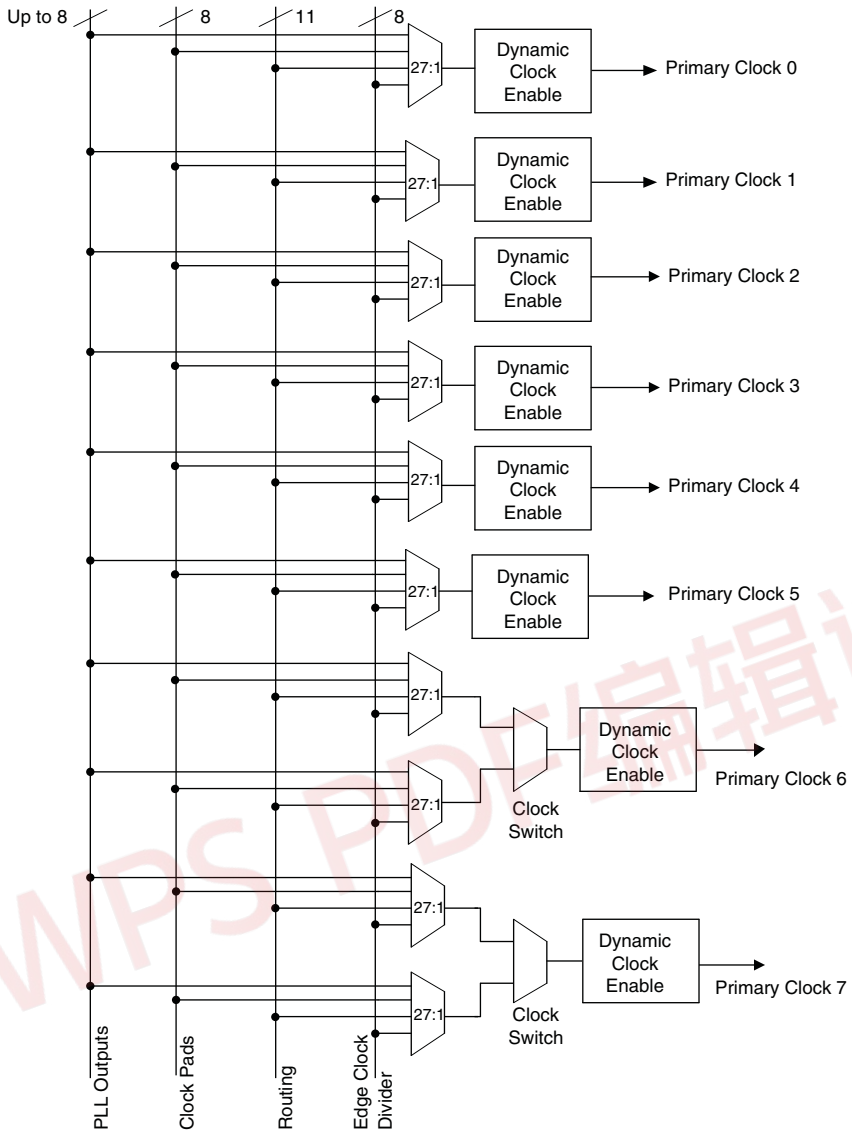
The MachXO2 architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO2-640U, MachXO2-1200/U and higher density devices have two edge clocks each on the top and bottom edges. Lower density devices have no edge clocks. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO2 devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO2 External Switching Characteristics table.

The primary clock signals for the MachXO2-256 and MachXO2-640 are generated from eight 17:1 muxes The available clock sources include eight I/O sources and 9 routing inputs. Primary clock signals for the MachXO2-640U, MachXO2-1200/U and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.

Figure 2-5. Primary Clocks for MachXO2 Devices

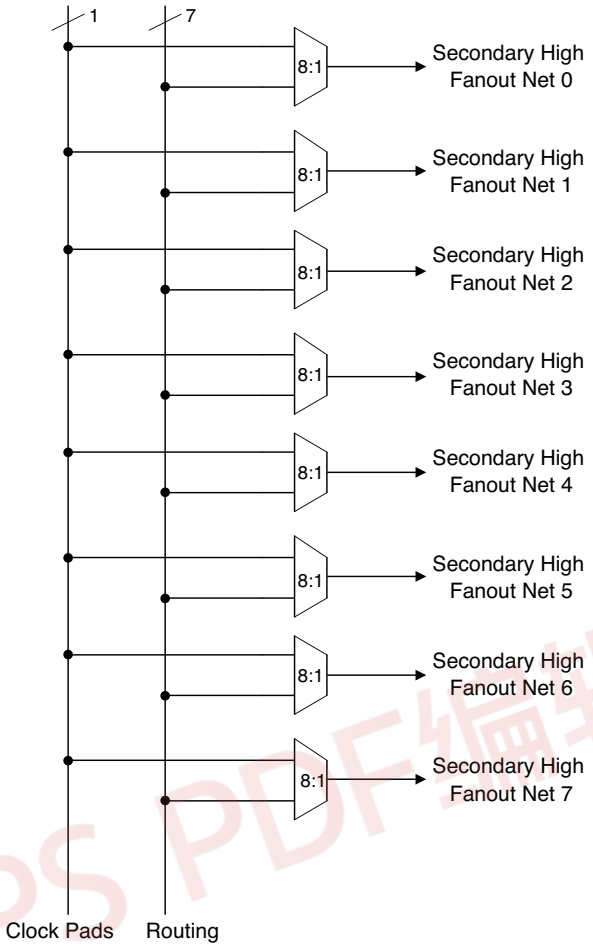


Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO2 External Switching Characteristics table.

Figure 2-6. Secondary High Fanout Nets for MachXO2 Devices



sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The MachXO2-640U, MachXO2-1200/U and larger devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO2 sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO2 clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.

This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the t_{LOCK} parameter has been satisfied.

The MachXO2 also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO2 PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the t_{LOCK} parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

For more details on the PLL and the WISHBONE interface, see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

Figure 2-7. PLL Diagram

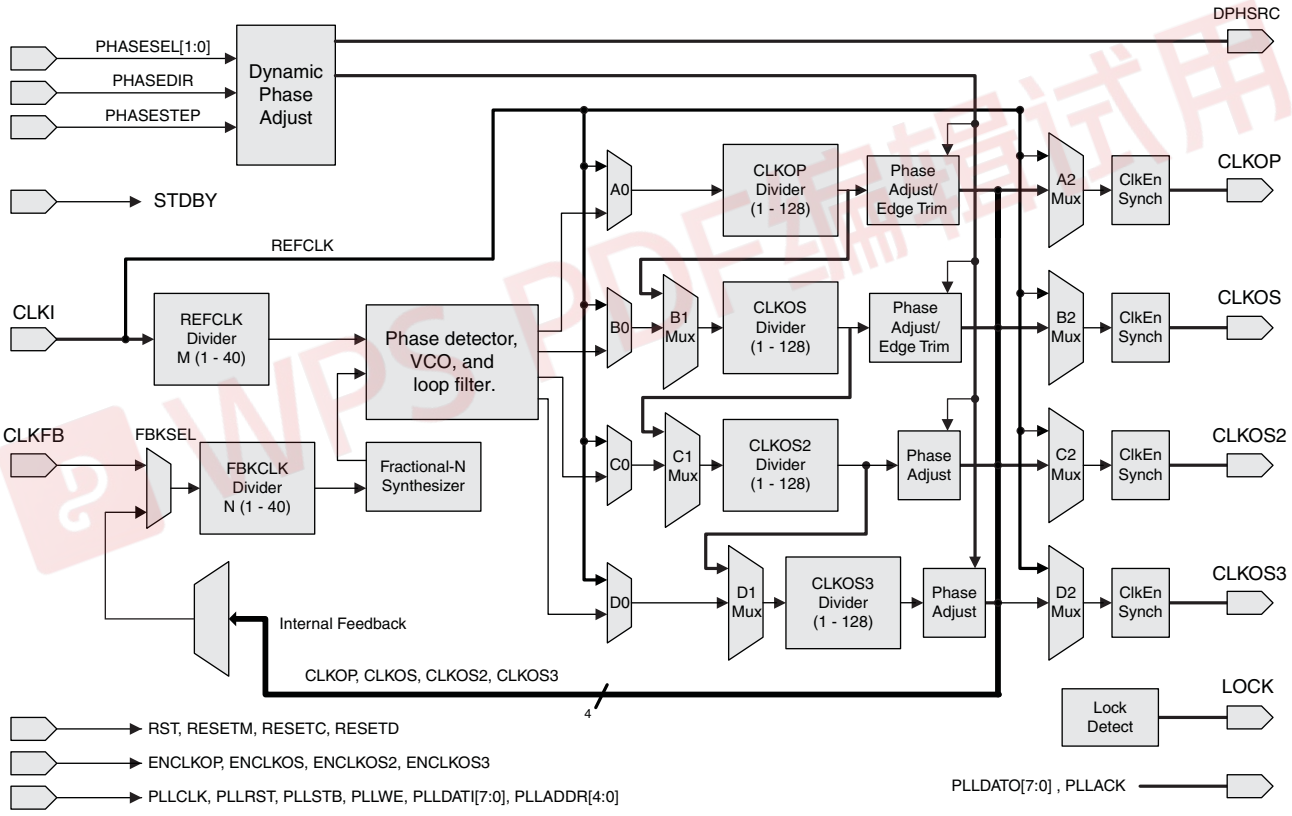


Table 2-4 provides signal descriptions of the PLL block.

Table 2-4. PLL Signal Descriptions

Port Name	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	I	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	I	Dynamic Phase step – toggle shifts VCO phase adjust by one step.

Table 2-4. PLL Signal Descriptions (Continued)

Port Name	I/O	Description
CLKOP	O	Primary PLL output clock (with phase shift adjustment)
CLKOS	O	Secondary PLL output clock (with phase shift adjust)
CLKOS2	O	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	O	Secondary PLL output clock3 (with phase shift adjust)
LOCK	O	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feedback signals.
DPHSRC	O	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset - includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	O	PLL data bus data output
PLLACK	O	PLL data bus acknowledge signal

sysMEM Embedded Block RAM Memory

The MachXO2-640/U and larger devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO2 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

Figure 2-8. sysMEM Memory Primitives

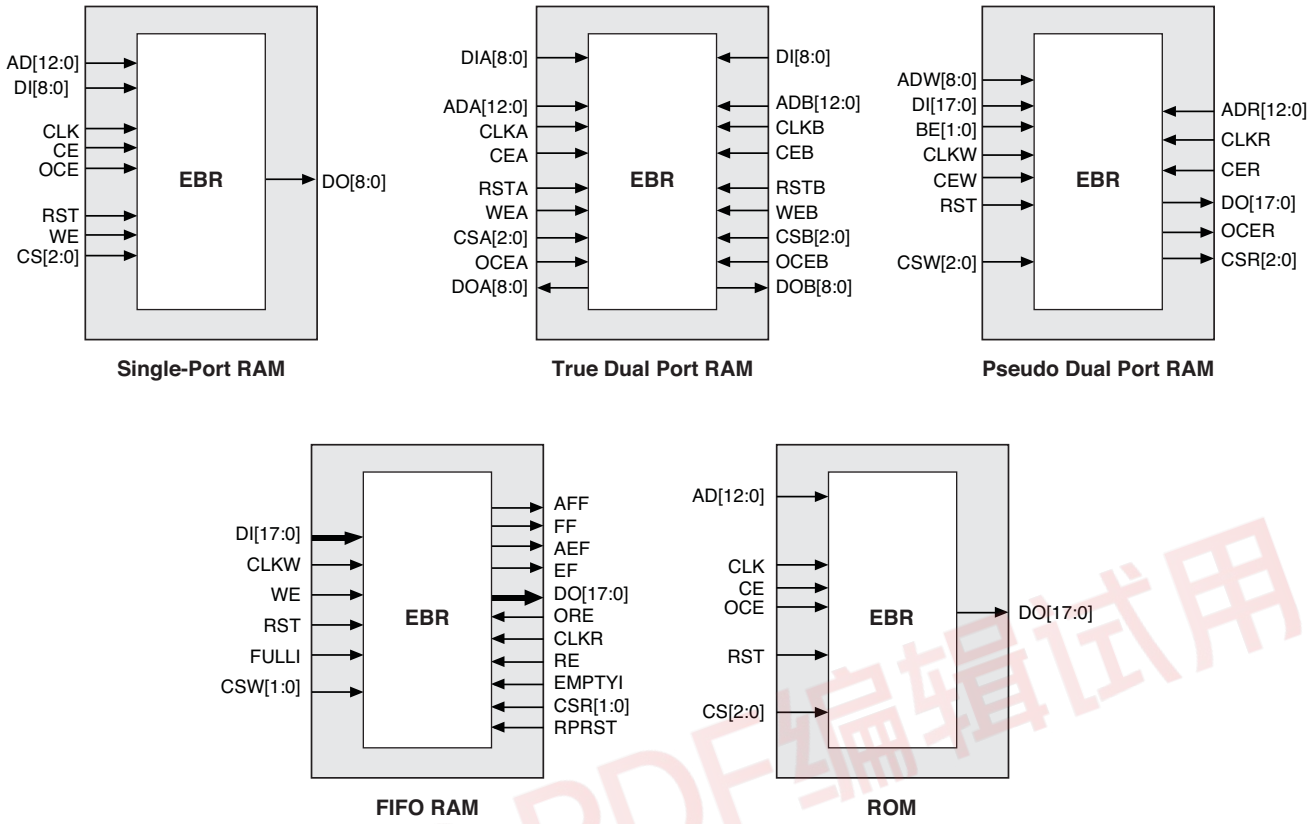


Table 2-6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE[1]	Output Clock Enable	Active High
RST	Reset	Active High
BE[1]	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	—
DI	Data In	—
DO	Data Out	—
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	—
FF	FIFO RAM Full Flag	—
AEF	FIFO RAM Almost Empty Flag	—
EF	FIFO RAM Empty Flag	—
RPRST	FIFO RAM Read Pointer Reset	—

1. Optional signals.
2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.

3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

Table 2-7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

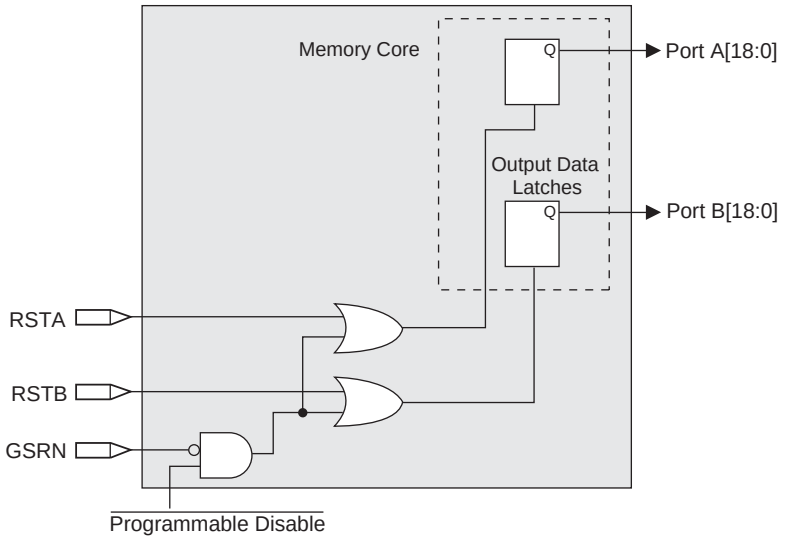
N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

Figure 2-9. Memory Core Reset

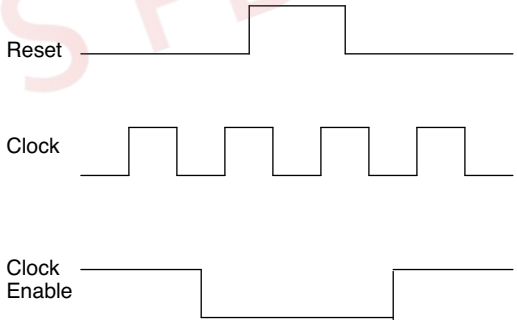


For further information on the sysMEM EBR block, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-10. The reset timing rules apply to the RPReset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For more details refer to TN1201, Memory Usage Guide for MachXO2 Devices.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

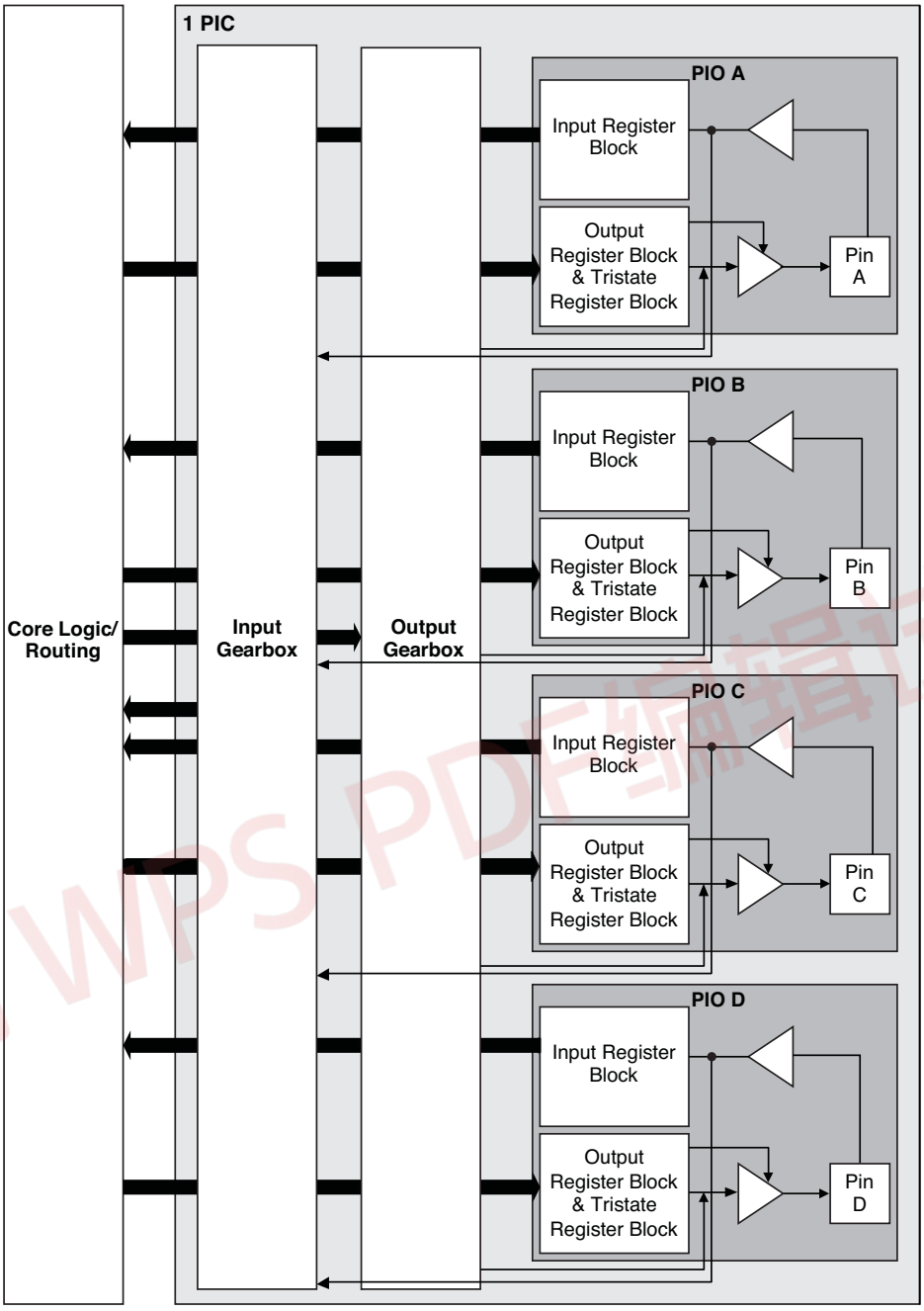
Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO2 devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO2 devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

The MachXO2-640U, MachXO2-1200/U and higher density devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these higher density devices have on-chip differential termination and also provide PCI support.

Figure 2-11. Group of Four Programmable I/O Cells



Notes:
1. Input gearbox is available only in PIC on the bottom edge of MachXO2-640U, MachXO2-1200/U and larger devices.
2. Output gearbox is available only in PIC on the top edge of MachXO2-640U, MachXO2-1200/U and larger devices.

PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Table 2-8. PIO Signal List

Pin Name	I/O Type	Description
CE	Input	Clock Enable
D	Input	Pin input from sysIO buffer.
INDD	Output	Register bypassed input.
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysIO Buffer
TQ	Output	Tri-state output signals to sysIO Buffer
DQSR90[1]	Input	DQS shift 90-degree read clock
DQSW90[1]	Input	DQS shift 90-degree write clock
DDRCLKPOL[1]	Input	DDR input register polarity control signal from DQS
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

1. Available in PIO on right edge only.

Input Register Block

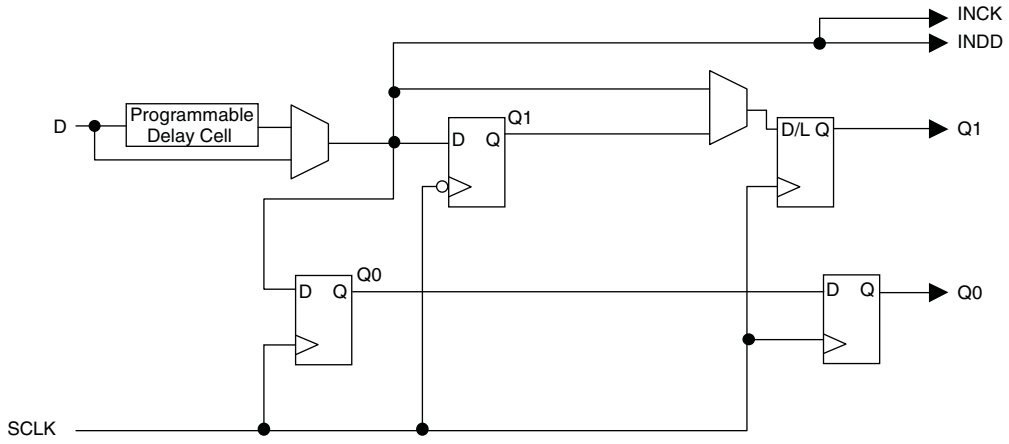
The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition to this functionality, the input register blocks for the PIOs on the right edge include built-in logic to interface to DDR memory.

Figure 2-12 shows the input register block for the PIOs located on the left, top and bottom edges. Figure 2-13 shows the input register block for the PIOs on the right edge.

Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

Figure 2-12. MachXO2 Input Register Block Diagram (PIO on Left, Top and Bottom Edges)



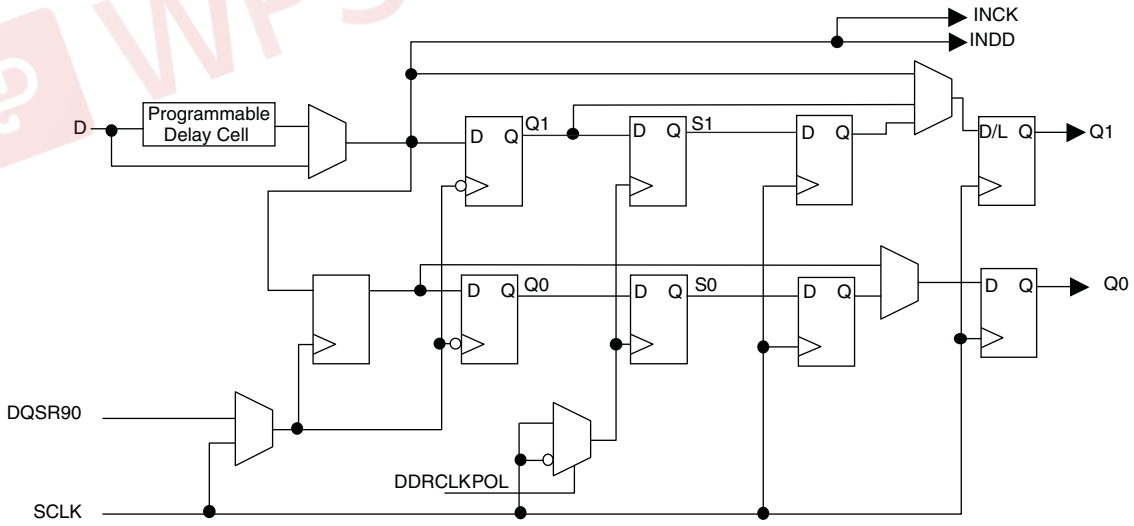
Right Edge

The input register block on the right edge is a superset of the same block on the top, bottom, and left edges. In addition to the modes described above, the input register block on the right edge also supports DDR memory mode.

In DDR memory mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (DQSR90) in the DDR Memory mode creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the DQS domain. The DQSR90 and DDRCLKPOL signals are generated in the DQS read-write block.

Figure 2-13. MachXO2 Input Register Block Diagram (PIO on Right Edge)



Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

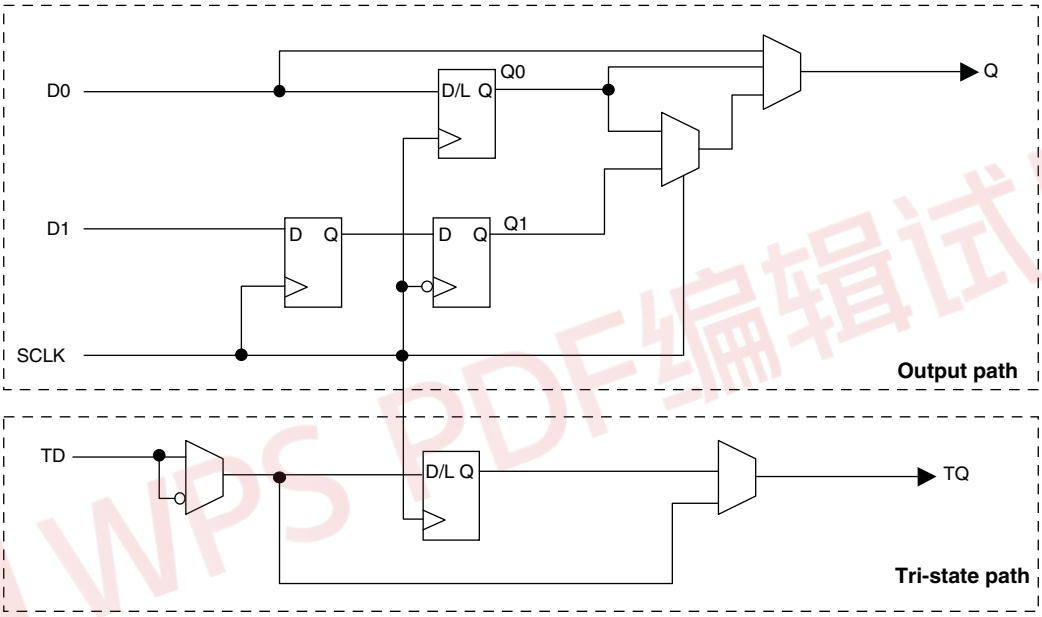
Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-14 shows the output register block on the left, top and bottom edges.

Figure 2-14. MachXO2 Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)



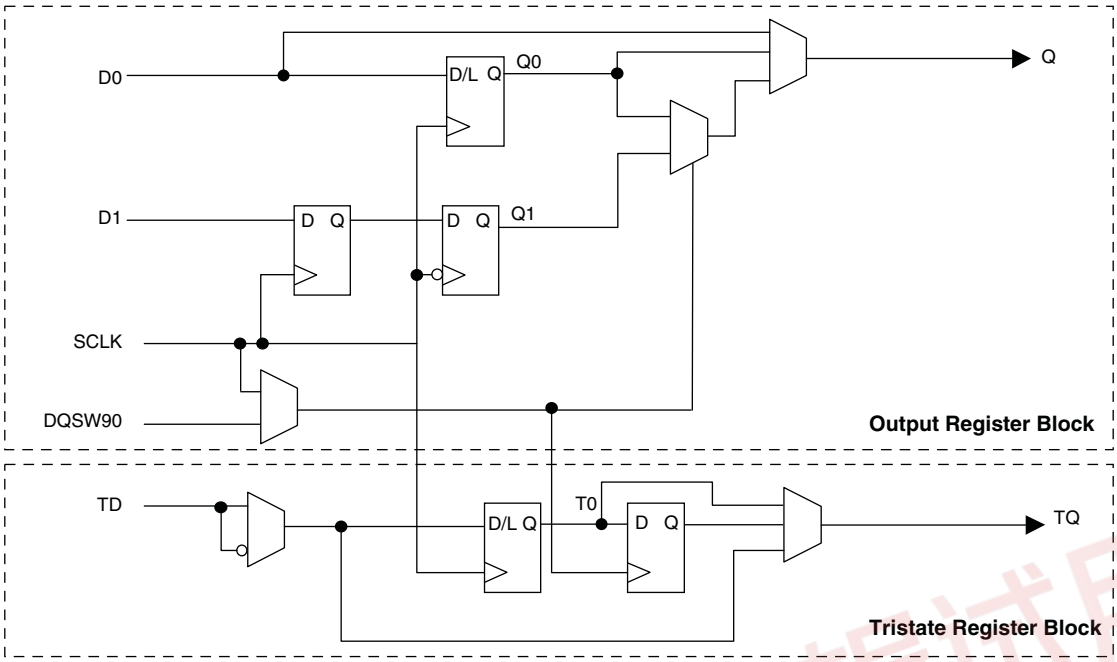
Right Edge

The output register block on the right edge is a superset of the output register on left, top and bottom edges of the device. In addition to supporting SDR and Generic DDR modes, the output register blocks for PIOs on the right edge include additional logic to support DDR-memory interfaces. Operation of this block is similar to that of the output register block on other edges.

In DDR memory mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the DQSW90 signal is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-15 shows the output register block on the right edge.

Figure 2-15. MachXO2 Output Register Block Diagram (PIO on the Right Edges)



Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

The tri-state register blocks on the right edge contain an additional register for DDR memory operation. In DDR memory mode, the register TS input is fed into another register that is clocked using the DQSW90 signal. The output of this register is used as a tri-state control.

Input Gearbox

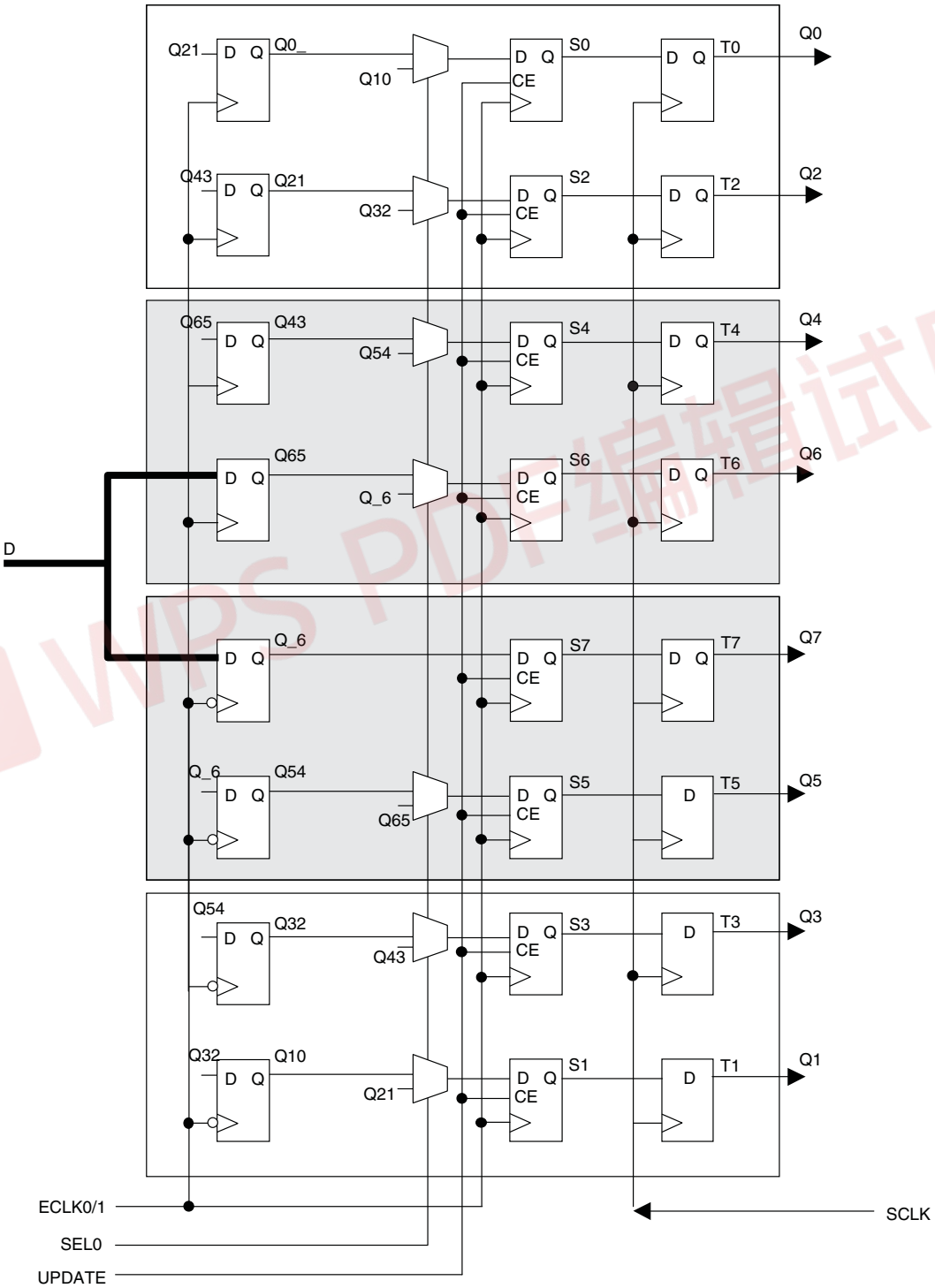
Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

Table 2-9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-16 shows a block diagram of the input gearbox.

Figure 2-16. Input Gearbox



More information on the input gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.

Output Gearbox

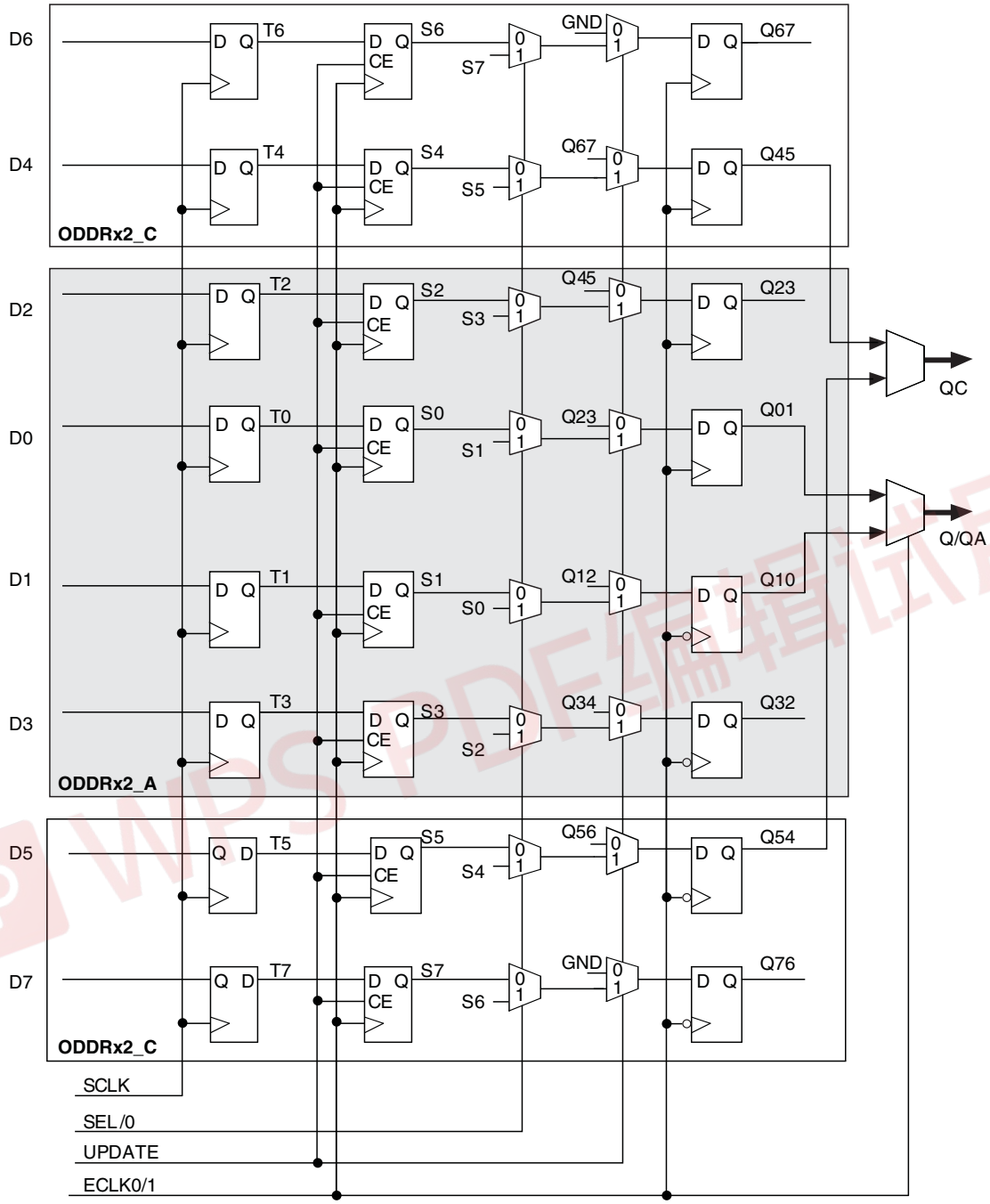
Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

Table 2-10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDRX4(8:1): D[7:0]		
GDDRX2(4:1)(IOL-A): D[3:0]		
GDDRX2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-17 shows the output gearbox block diagram.

Figure 2-17. Output Gearbox



More information on the output gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.

DDR Memory Support

Certain PICs on the right edge of MachXO2-640U, MachXO2-1200/U and larger devices, have additional circuitry to allow the implementation of DDR memory interfaces. There are two groups of 14 or 12 PIOs each on the right edge with additional circuitry to implement DDR memory interfaces. This capability allows the implementation of up to 16-bit wide memory interfaces. One PIO from each group contains a control element, the DQS Read/Write Block, to facilitate the generation of clock and control signals (DQSR90, DQSW90, DDRCLKPOL and DATAVALID). These clock and control signals are distributed to the other PIO in the group through dedicated low skew routing.

DQS Read Write Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Read Write block provides the required clock alignment for DDR memory interfaces. DQSR90 and DQSW90 signals are generated by the DQS Read Write block from the DQS input.

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the read cycle) is unknown. The MachXO2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This circuit changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each read cycle for the correct clock polarity. Prior to the read operation in DDR memories, DQS is in tri-state (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit in the DQS Read Write block detects the first DQS rising edge after the preamble state and generates the DDRCLKPOL signal. This signal is used to control the polarity of the clock to the synchronizing registers.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration signals (6-bit bus) from a DLL on the right edge of the device. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, PCI, SSTL, HSTL, LVDS, BLVDS, MLVDS and LVPECL.

Each bank is capable of supporting multiple I/O standards. In the MachXO2 devices, single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS and PCI), differential (LVDS) and referenced input buffers (SSTL and HSTL) are powered using I/O supply voltage (V_{CCIO}). Each sysIO bank has its own V_{CCIO}. In addition, each bank has a voltage reference, V_{REF}, which allows the use of referenced input buffers independent of the bank V_{CCIO}.

MachXO2-256 and MachXO2-640 devices contain single-ended ratioed input buffers and single-ended output buffers with complementary outputs on all the I/O banks. Note that the single-ended input buffers on these devices do not contain PCI clamps. In addition to the single-ended I/O buffers these two devices also have differential and referenced input buffers on all I/Os. The I/Os are arranged in pairs, the two pads in the pair are described as "T" and "C", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 devices contain three types of sysIO buffer pairs.

1. **Left and Right sysIO Buffer Pairs**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential and referenced input buffers.

2. **Bottom sysIO Buffer Pairs**
   The sysIO buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential and referenced input buffers. Only the I/Os on the bottom banks have programmable PCI clamps and differential input termination. The PCI clamp is enabled after V_{CC} and V_{CCIO} are at valid operating levels and the device has been configured.

3. **Top sysIO Buffer Pairs**
   The sysIO buffer pairs in the top bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential and referenced I/O buffers. Half of the sysIO buffer pairs on the top edge have true differential outputs. The sysIO buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver. The referenced input buffer can also be configured as a differential input buffer.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCIO0} have reached V_{PORUP} level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-down to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to V_{CCIO} as the default functionality). The I/O pins will maintain the blank configuration until V_{CC} and V_{CCIO} (for I/O banks containing configuration I/Os) have reached V_{PORUP} levels at which time the I/Os will take on the user-configured settings only after a proper download/configuration.

Supported Standards

The MachXO2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL, and PCI. The buffer supports the LVTTL, PCI, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO2-640U, MachXO2-1200/U and higher devices support on-chip LVDS output buffers on approximately 50% of the I/Os on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO2 devices. PCI support is provided in the bottom bank of theMachXO2-640U, MachXO2-1200/U and higher density devices. Table 2-11 summarizes the I/O characteristics of the MachXO2 PLDs.

Tables 2-11 and 2-12 show the I/O standards (together with their supply and reference voltages) supported by the MachXO2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1202, MachXO2 sysIO Usage Guide.

Table 2-11. I/O Support Device by Device

	MachXO2-256, MachXO2-640	MachXO2-640U, MachXO2-1200	MachXO2-1200U MachXO2-2000/U, MachXO2-4000, MachXO2-7000
Number of I/O Banks	4	4	6
Type of Input Buffers	Single-ended (all I/O banks) Differential Receivers (all I/O banks)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)
Types of Output Buffers	Single-ended buffers with complementary outputs (all I/O banks)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)
Differential Output Emulation Capability	All I/O banks	All I/O banks	All I/O banks
PCI Clamp Support	No	Clamp on bottom side only	Clamp on bottom side only

Table 2-12. Supported Input Standards

	VCCIO (Typ.)				
Input Standard	**3.3 V**	**2.5 V**	**1.8 V**	**1.5**	**1.2 V**
Single-Ended Interfaces					
LVTTL	✓	✓[2]	✓[2]	✓[2]	
LVCMOS33	✓	✓[2]	✓[2]	✓[2]	
LVCMOS25	✓[2]	✓	✓[2]	✓[2]	
LVCMOS18	✓[2]	✓[2]	✓	✓[2]	
LVCMOS15	✓[2]	✓[2]	✓[2]	✓	✓[2]
LVCMOS12	✓[2]	✓[2]	✓[2]	✓[2]	✓
PCI[1]	✓				
SSTL18 (Class I, Class II)	✓	✓	✓		
SSTL25 (Class I, Class II)	✓	✓			
HSTL18 (Class I, Class II)	✓	✓	✓		
Differential Interfaces					
LVDS	✓	✓			
BLVDS, MVDS, LVPECL, RSDS	✓	✓			
MIPI[3]	✓	✓			
Differential SSTL18 Class I, II	✓	✓	✓		
Differential SSTL25 Class I, II	✓	✓			
Differential HSTL18 Class I, II	✓	✓	✓		

1. Bottom banks of MachXO2-640U, MachXO2-1200/U and higher density devices only.
2. Reduced functionality. Refer to TN1202, MachXO2 sysIO Usage Guide for more detail.
3. These interfaces can be emulated with external resistors in all devices.

Table 2-13. Supported Output Standards

Output Standard	V_{CCIO} (Typ.)
Single-Ended Interfaces	
LVTTL	3.3
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8
LVCMOS15	1.5
LVCMOS12	1.2
LVCMOS33, Open Drain	—
LVCMOS25, Open Drain	—
LVCMOS18, Open Drain	—
LVCMOS15, Open Drain	—
LVCMOS12, Open Drain	—
PCI33	3.3
SSTL25 (Class I)	2.5
SSTL18 (Class I)	1.8
HSTL18(Class I)	1.8
Differential Interfaces	
LVDS[1, 2]	2.5, 3.3
BLVDS, MLVDS, RSDS [2]	2.5
LVPECL[2]	3.3
MIPI[2]	2.5
Differential SSTL18	1.8
Differential SSTL25	2.5
Differential HSTL18	1.8

1. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.

sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO2-1200U, MachXO2-2000/U and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO2-1200 and lower density devices have four banks (one bank per side). Figures 2-18 and 2-19 show the sysIO banks and their associated supplies for all devices.

Figure 2-18. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 Banks

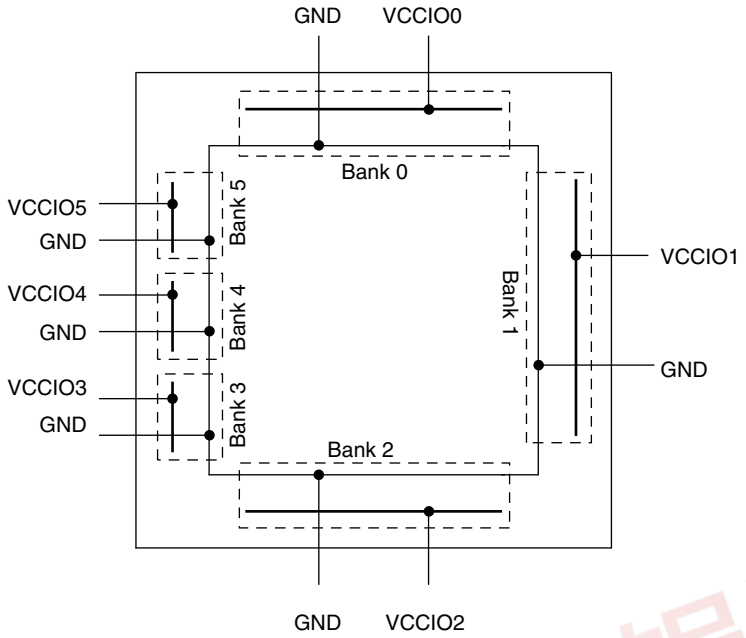
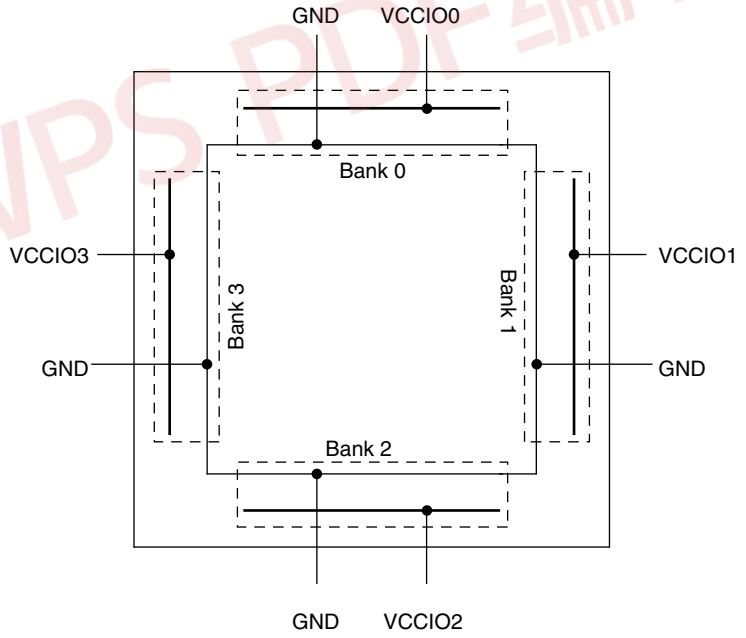


Figure 2-19. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks



Hot Socketing

The MachXO2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO2 ideal for many multiple power supply and hot-swap applications.

On-chip Oscillator

Every MachXO2 device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
2. During configuration, users select a different master clock frequency.
3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-14 lists all the available MCLK frequencies.

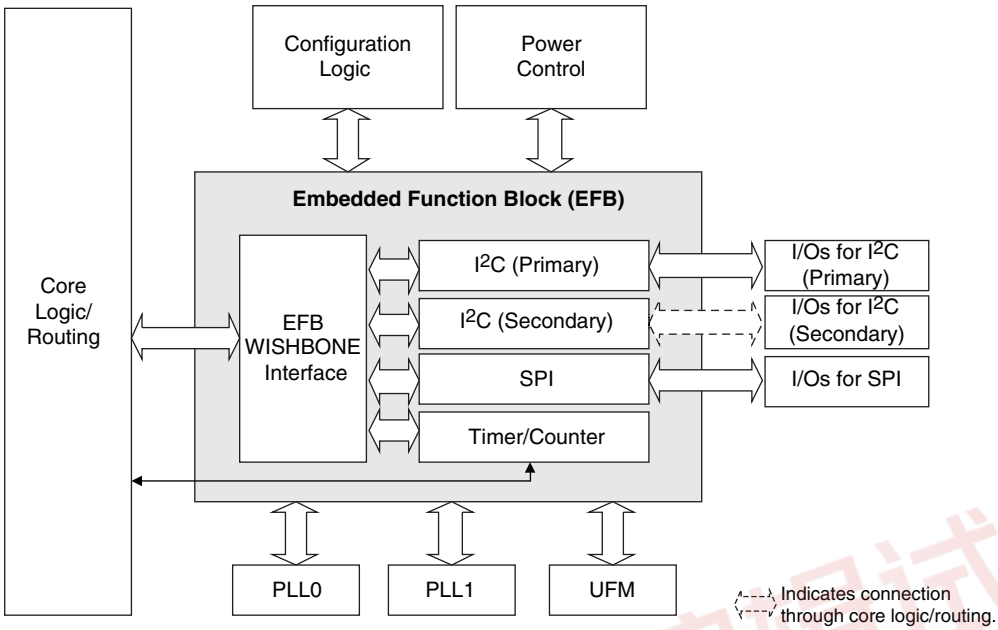
Table 2-14. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

Embedded Hardened IP Functions and User Flash Memory

All MachXO2 devices provide embedded hardened functions such as SPI, I^2C and Timer/Counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2-20.

Figure 2-20. Embedded Function Block Interface



Hardened I²C IP Core

Every MachXO2 device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I²C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface

Figure 2-21. I²C Core Block Diagram

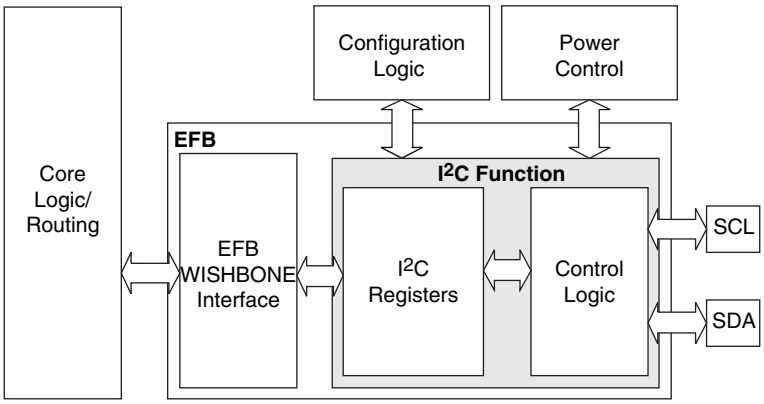


Table 2-15 describes the signals interfacing with the I²C cores.

Table 2-15. I²C Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I²C core. The signal is an output if the I²C core is in master mode. The signal is an input if the I²C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device.
i2c_sda	Bi-directional	Bi-directional data line of the I²C core. The signal is an output when data is transmitted from the I²C core. The signal is an input when data is received into the I²C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device.
i2c_irqo	Output	Interrupt request output signal of the I²C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I²C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.

Hardened SPI IP Core

Every MachXO2 device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO2 devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface

There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology (Appendix B)
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices

Figure 2-22. SPI Core Block Diagram

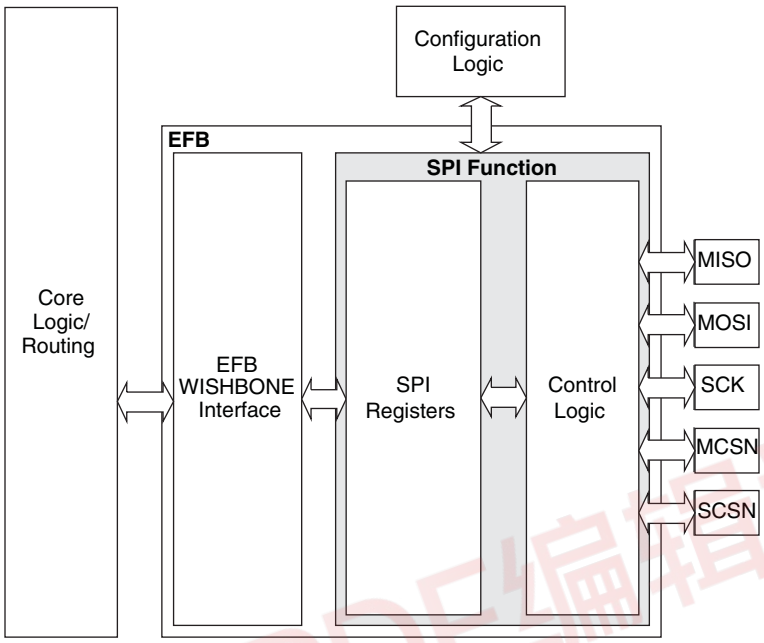


Table 2-16 describes the signals interfacing with the SPI cores.

Table 2-16. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	O	Master	SPI master chip-select output
spi_csn[1..7]	O	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	O	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
ufm_sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the User Flash Memory (UFM).
cfg_stdby	O	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.
cfg_wake	O	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.

Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  - — Watchdog timer
  - — Clear timer on compare match
  - — Fast PWM
  - — Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

Figure 2-23. Timer/Counter Block Diagram

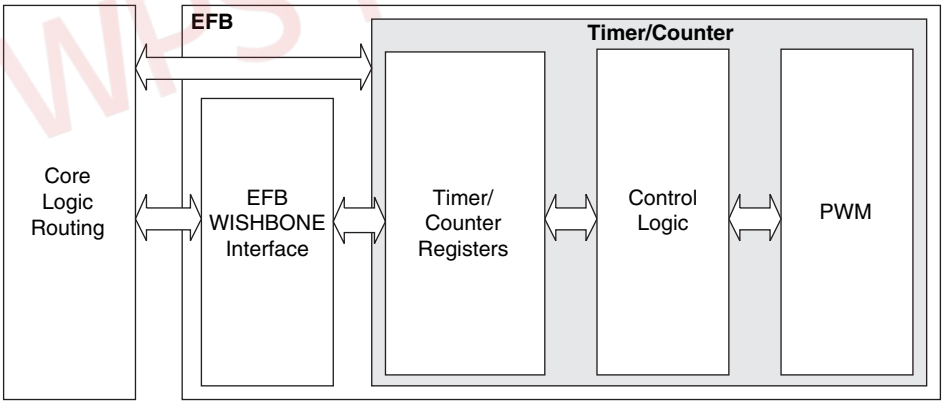


Table 2-17. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	O	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	O	Timer counter output signal

For more details on these embedded functions, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

User Flash Memory (UFM)

MachXO2-640/U and higher density devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I^2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

Standby Mode and Power Saving Options

MachXO2 devices are available in three options for maximum flexibility: ZE, HC and HE devices. The ZE devices have ultra low static and dynamic power consumption. These devices use a 1.2 V core voltage that further reduces power consumption. The HC and HE devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the HE devices operate at 1.2 V V_{CC}.

MachXO2 devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO2 devices support an ultra low power Stand-by mode. While most of these features are available in all three device types, these features are mainly intended for use with MachXO2 ZE devices to manage power consumption.

In the stand-by mode the MachXO2 devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I^2C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO2 devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

Table 2-18. MachXO2 Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe V_{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1198, Power Estimation and Management for MachXO2 Devices.

Power On Reset

MachXO2 devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the V_{PORUP} level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices), V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators (HC devices), V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time ($t_{REFRESH}$) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tristate. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min) they should not shut down the bandgap or POR circuit.

Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I^2C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

1. Internal Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I^2C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, MachXO2 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

TransFR (Transparent Field Reconfiguration)
TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

When implementing background programming of the on-chip Flash, care must be taken for the operation of the PLL. For devices that have two PLLs (XO2-2000U, -4000 and -7000), the system must put the RPLL (Right-side PLL) in reset state during the background Flash programming. More detailed description can be found in TN1204, MachXO2 Programming and Configuration Usage Guide.

Security and One-Time Programmable Mode (OTP)
For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO2 devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile Flash memory spaces. The device can be in one of two modes:

1. Unlocked – Readback of the SRAM configuration and non-volatile Flash memory spaces is allowed.

2. Permanently Locked – The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Dual Boot
MachXO2 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the on-chip Flash. The golden image MUST reside in an external SPI Flash. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Soft Error Detection
The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1206, MachXO2 Soft Error Detection Usage Guide.

TraceID

Each MachXO2 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I^2C, or JTAG interfaces.

Density Shifting

The MachXO2 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO2 migration files.

MachXO2 Family Data Sheet DC and Switching Characteristics

March 2017 Data Sheet DS1035

Absolute Maximum Ratings[1, 2, 3]

	MachXO2 ZE/HE (1.2 V)	MachXO2 HC (2.5 V / 3.3 V)
Supply Voltage V_{CC}	–0.5 V to 1.32 V	–0.5 V to 3.75 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied[4, 5]	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied[4]	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T_J)	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to (V_{IHMAX} + 2) volts is permitted for a duration of <20 ns.
5. The dual function I^2C pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.

Recommended Operating Conditions[1]

Symbol	Parameter	Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V / 3.3 V Devices	2.375	3.6	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	1.14	3.6	V
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature Industrial Operation	–40	100	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

Power Supply Ramp Rates[1]

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.01	—	100	V/ms

1. Assumes monotonic ramp rates.

Power-On-Reset Voltage Levels[1, 2, 3, 4, 5]

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and V_{CCIO0})	0.9	—	1.06	V
$V_{PORUPEXT}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	—	2.1	V
$V_{PORDNBG}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CCINT})	0.75	—	0.93	V
$V_{PORDNBGEXT}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	—	1.33	V
$V_{PORDNSRAM}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CCINT})	—	0.6	—	V
$V_{PORDNSRAMEXT}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	—	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.
3. Note that V_{PORUP} (min.) and $V_{PORDNBG}$ (max.) are in different process corners. For any given process corner $V_{PORDNBG}$ (max.) is always 12.0 mV below V_{PORUP} (min.).
4. $V_{PORUPEXT}$ is for HC devices only. In these devices a separate POR circuit monitors the external V_{CC} power supply.
5. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

Programming/Erase Specifications

Symbol	Parameter	Min.	Max.[1]	Units
$N_{PROGCYC}$	Flash Programming cycles per $t_{RETENTION}$	—	10,000	Cycles
	Flash functional programming cycles	—	100,000	
$t_{RETENTION}$	Data retention at 100 °C junction temperature	10	—	Years
	Data retention at 85 °C junction temperature	20	—	

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Max.	Units
I_{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/–1000	µA

1. Insensitive to sequence of V_{CC} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO}.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

ESD Performance

Please refer to the MachXO2 Product Family Qualification Summary for complete qualification data, including ESD performance.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4]	Input or I/O Leakage	Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX)	—	—	+175	µA
		Clamp OFF and $V_{IN} = V_{CCIO}$	–10	—	10	µA
		Clamp OFF and V_{CCIO} –0.97 V < V_{IN} < V_{CCIO}	–175	—	—	µA
		Clamp OFF and 0 V < V_{IN} < V_{CCIO} –0.97 V	—	—	10	µA
		Clamp OFF and V_{IN} = GND	—	—	10	µA
		Clamp ON and 0 V < V_{IN} < V_{CCIO}	—	—	10	µA
I_{PU}	I/O Active Pull-up Current	0 < V_{IN} < 0.7 V_{CCIO}	–30	—	-309	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) < V_{IN} < V_{CCIO}	30	—	305	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	–30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	305	µA
I_{BHHO}	Bus Hold High Overdrive current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	–309	µA
V_{BHT}[3]	Bus Hold Trip Points		V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	3	5	9	pF
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	3	5.5	7	pF
V_{HYST}	Hysteresis for Schmitt Trigger Inputs[5]	V_{CCIO} = 3.3 V, Hysteresis = Large	—	450	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Large	—	250	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Large	—	125	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Large	—	100	—	mV
		V_{CCIO} = 3.3 V, Hysteresis = Small	—	250	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Small	—	150	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Small	—	60	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Small	—	40	—	mV

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. When V_{IH} is higher than V_{CCIO}, a transient current typically of 30 ns in duration or less with a peak current of 6 mA can occur on the high-to-low transition. For true LVDS output pins in MachXO2-640U, MachXO2-1200/U and larger devices, V_{IH} must be less than or equal to V_{CCIO}.
5. With bus keeper circuit turned on. For more details, refer to TN1202, MachXO2 sysIO Usage Guide.

Static Supply Current – ZE Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO2-256ZE	18	µA
		LCMXO2-640ZE	28	µA
		LCMXO2-1200ZE	56	µA
		LCMXO2-2000ZE	80	µA
		LCMXO2-4000ZE	124	µA
		LCMXO2-7000ZE	189	µA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	1	µA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off. To estimate the impact of turning each of these items on, please refer to the following table or for more detail with your specific design use the Power Calculator tool.
3. Frequency = 0 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Static Power Consumption Contribution of Different Components – ZE Devices

The table below can be used for approximating static power consumption. For a more accurate power analysis for your design please use the Power Calculator tool.

Symbol	Parameter	Typ.	Units
I_{DCBG}	Bandgap DC power contribution	101	µA
I_{DCPOR}	POR DC power contribution	38	µA
$I_{DCIOBANKCONTROLLER}$	DC power contribution per I/O bank controller	143	µA

Static Supply Current – HC/HE Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO2-256HC	1.15	mA
		LCMXO2-640HC	1.84	mA
		LCMXO2-640UHC	3.48	mA
		LCMXO2-1200HC	3.49	mA
		LCMXO2-1200UHC	4.80	mA
		LCMXO2-2000HC	4.80	mA
		LCMXO2-2000UHC	8.44	mA
		LCMXO2-4000HC	8.45	mA
		LCMXO2-7000HC	12.87	mA
		LCMXO2-2000HE	1.39	mA
		LCMXO2-4000HE	2.55	mA
		LCMXO2-7000HE	4.06	mA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
3. Frequency = 0 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Programming and Erase Flash Supply Current – HC/HE Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO2-256HC	14.6	mA
		LCMXO2-640HC	16.1	mA
		LCMXO2-640UHC	18.8	mA
		LCMXO2-1200HC	18.8	mA
		LCMXO2-1200UHC	22.1	mA
		LCMXO2-2000HC	22.1	mA
		LCMXO2-2000UHC	26.8	mA
		LCMXO2-4000HC	26.8	mA
		LCMXO2-7000HC	33.2	mA
		LCMXO2-2000HE	18.3	mA
		LCMXO2-2000UHE	20.4	mA
		LCMXO2-4000HE	20.4	mA
		LCMXO2-7000HE	23.9	mA
I_{CCIO}	Bank Power Supply[6]	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. T_J = 25 °C, power supplies at nominal voltage.
6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

Programming and Erase Flash Supply Current – ZE Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO2-256ZE	13	mA
		LCMXO2-640ZE	14	mA
		LCMXO2-1200ZE	15	mA
		LCMXO2-2000ZE	17	mA
		LCMXO2-4000ZE	18	mA
		LCMXO2-7000ZE	20	mA
I_{CCIO}	Bank Power Supply[6]	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. TJ = 25 °C, power supplies at nominal voltage.
6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.6	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.6	—	—	—
PCI[3]	3.135	3.3	3.6	—	—	—
SSTL25	2.375	2.5	2.625	1.15	1.25	1.35
SSTL18	1.71	1.8	1.89	0.833	0.9	0.969
HSTL18	1.71	1.8	1.89	0.816	0.9	1.08
LVCMOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVCMOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVCMOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVCMOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVCMOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVCMOS12R33[4]	3.135	3.3	3.6	0.45	0.6	0.75
LVCMOS12R25[4]	2.375	2.5	2.625	0.45	0.6	0.75
LVCMOS10R33[4]	3.135	3.3	3.6	0.35	0.5	0.65
LVCMOS10R25[4]	2.375	2.5	2.625	0.35	0.5	0.65
LVDS25[1, 2]	2.375	2.5	2.625	—	—	—
LVDS33[1, 2]	3.135	3.3	3.6	—	—	—
LVPECL[1]	3.135	3.3	3.6	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—
RSDS[1]	2.375	2.5	2.625	—	—	—
SSTL18D	1.71	1.8	1.89	—	—	—
SSTL25D	2.375	2.5	2.625	—	—	—
HSTL18D	1.71	1.8	1.89	—	—	—

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
3. Input on the bottom bank of the MachXO2-640U, MachXO2-1200/U and larger devices only.
4. Supported only for inputs and BIDIs for all ZE devices, and –6 speed grade for HE and HC devices.

sysIO Single-Ended DC Electrical Characteristics[1, 2]

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max.[4] (mA)	I_{OH} Max.[4] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3 LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
							16	–16
							24	–24
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
							16	–16
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.5	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.2	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} – 0.4	4	–2
							8	–6
					0.2	V_{CCIO} – 0.2	0.1	–0.1
PCI	–0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	–0.5
SSTL25 Class I	–0.3	V_{REF} – 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	8	8
SSTL25 Class II	–0.3	V_{REF} – 0.18	V_{REF} + 0.18	3.6	NA	NA	NA	NA
SSTL18 Class I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	3.6	0.40	V_{CCIO} - 0.40	8	8
SSTL18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	3.6	NA	NA	NA	NA
HSTL18 Class I	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	V_{CCIO} - 0.40	8	8
HSTL18 Class II	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS25R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS12R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max.[4] (mA)	I_{OH} Max.[4] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS10R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain

1. MachXO2 devices allow LVCMOS inputs to be placed in I/O banks where V_{CCIO} is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO2 devices do not meet the relevant JEDEC specification are documented in the table below.
2. MachXO2 devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1202, MachXO2 sysIO Usage Guide.
3. The dual function I^2C pins SCL and SDA are limited to a V_{IL} min of –0.25 V or to –0.3 V with a duration of <10 ns.
4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive VCCIO or GND pad connections, or between the last VCCIO or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n * 8 mA. “n” is the number of I/O pads between the two consecutive bank VCCIO or GND connections or between the last VCCIO and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

Input Standard	V_{CCIO} (V)	V_{IL} Max. (V)
LVCMOS 33	1.5	0.685
LVCMOS 25	1.5	0.687
LVCMOS 18	1.5	0.655

sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of MachXO2-640U, MachXO2-1200/U and higher density devices in the MachXO2 PLD family.

LVDS

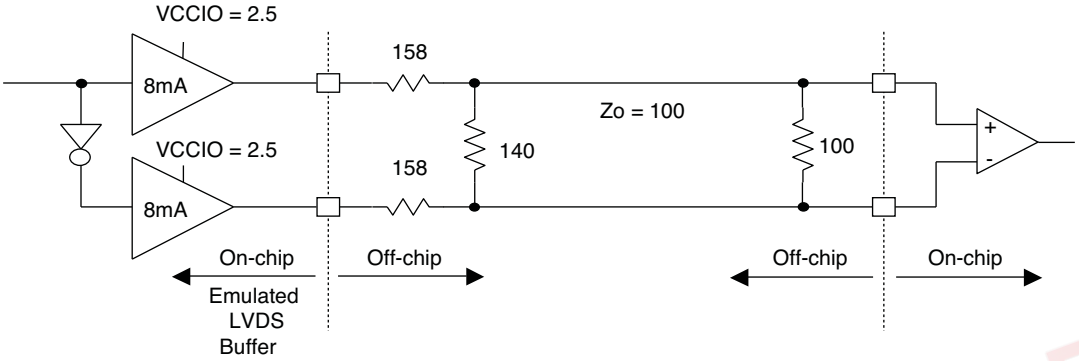
Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO} = 3.3 V	0	—	2.605	V
		V_{CCIO} = 2.5 V	0	—	2.05	V
V_{THD}	Differential Input Threshold		±100	—		mV
V_{CM}	Input Common Mode Voltage	V_{CCIO} = 3.3 V	0.05	—	2.6	V
		V_{CCIO} = 2.5 V	0.05	—	2.0	V
I_{IN}	Input current	Power on	—	—	±10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.375	—	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.90	1.025	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.395	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0 V driver outputs shorted	—	—	24	mA

LVDS Emulation

MachXO2 devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

Figure 3-1. LVDS Using External Resistors (LVDS25E)



Note: All resistors are ±1%.

Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	158	Ohms
R_P	Driver parallel resistor	140	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	6.03	mA

BLVDS

The MachXO2 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

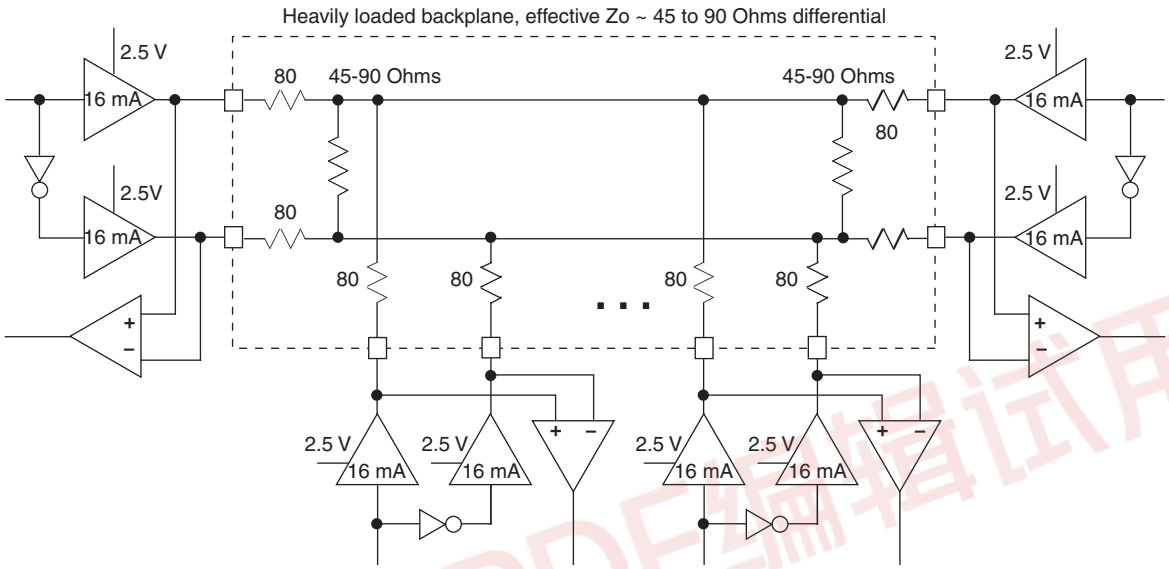


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	20	20	Ohms
R_S	Driver series resistance	80	80	Ohms
R_{TLEFT}	Left end termination	45	90	Ohms
R_{TRIGHT}	Right end termination	45	90	Ohms
V_{OH}	Output high voltage	1.376	1.480	V
V_{OL}	Output low voltage	1.124	1.020	V
V_{OD}	Output differential voltage	0.253	0.459	V
V_{CM}	Output common mode voltage	1.250	1.250	V
I_{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.

LVPECL

The MachXO2 family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

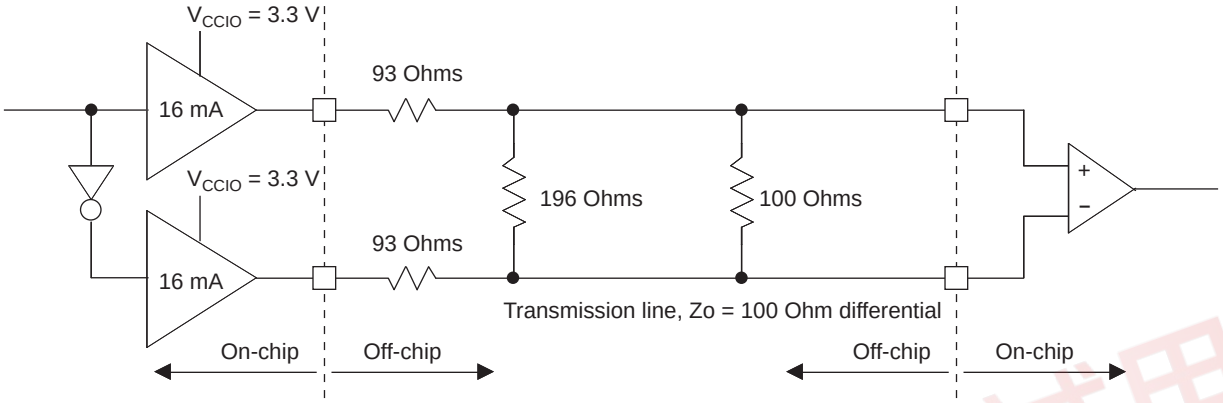


Table 3-3. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	93	Ohms
R_P	Driver parallel resistor	196	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	2.05	V
V_{OL}	Output low voltage	1.25	V
V_{OD}	Output differential voltage	0.80	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	12.11	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

RSDS

The MachXO2 family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

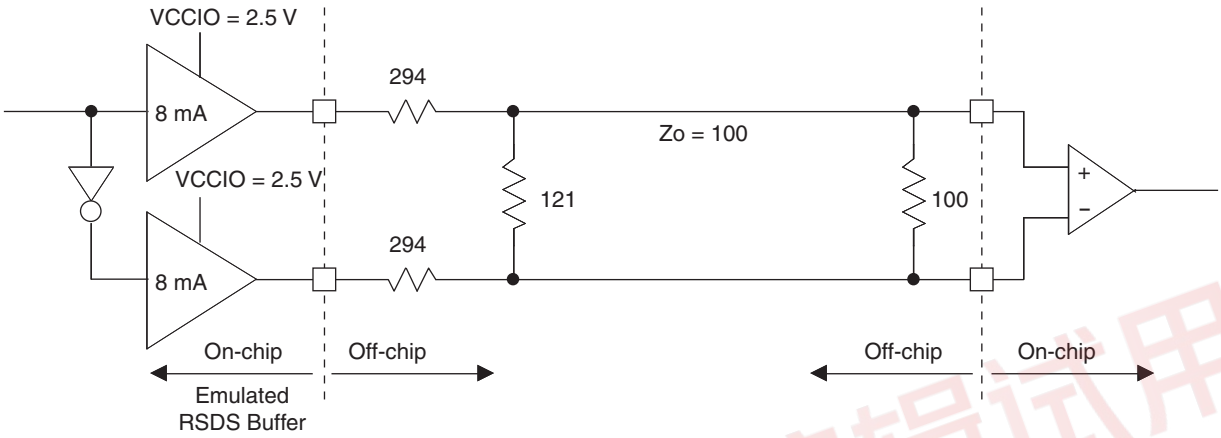


Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	294	Ohms
R_P	Driver parallel resistor	121	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	Ohms
I_{DC}	DC output current	3.66	mA

Typical Building Block Function Performance – HC/HE Devices[1]

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	-6 Timing	Units
Basic Functions		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

Register-to-Register Performance

Function	-6 Timing	Units
Basic Functions		
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

Typical Building Block Function Performance – ZE Devices[1]

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–3 Timing	Units
Basic Functions		
16-bit decoder	13.9	ns
4:1 MUX	10.9	ns
16:1 MUX	12.0	ns

Register-to-Register Performance

Function	–3 Timing	Units
Basic Functions		
16:1 MUX	191	MHz
16-bit adder	134	MHz
16-bit counter	148	MHz
64-bit counter	77	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	90	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	214	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
LVDS25	400	MHz
LVDS25E	150	MHz
RSDS25	150	MHz
RSDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
SSTL25_I	150	MHz
SSTL25_II	150	MHz
SSTL25D_I	150	MHz
SSTL25D_II	150	MHz
SSTL18_I	150	MHz
SSTL18_II	150	MHz
SSTL18D_I	150	MHz
SSTL18D_II	150	MHz
HSTL18_I	150	MHz
HSTL18_II	150	MHz
HSTL18D_I	150	MHz
HSTL18D_II	150	MHz
PCI33	134	MHz
LVTTL33	150	MHz
LVTTL33D	150	MHz
LVCMOS33	150	MHz
LVCMOS33D	150	MHz
LVCMOS25	150	MHz
LVCMOS25D	150	MHz
LVCMOS25R33	150	MHz
LVCMOS18	150	MHz
LVCMOS18D	150	MHz
LVCMOS18R33	150	MHz
LVCMOS18R25	150	MHz
LVCMOS15	150	MHz
LVCMOS15D	150	MHz
LVCMOS15R33	150	MHz
LVCMOS15R25	150	MHz
LVCMOS12	91	MHz
LVCMOS12D	91	MHz

MachXO2 External Switching Characteristics – HC/HE Devices[1, 2, 3, 4, 5, 6, 7]

Over Recommended Operating Conditions

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f_{MAX_PRI}[8]	Frequency for Primary Clock Tree	All MachXO2 devices	—	388	—	323	—	269	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	0.5	—	0.6	—	0.7	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO2-256HC-HE	—	912	—	939	—	975	ps
		MachXO2-640HC-HE	—	844	—	871	—	908	ps
		MachXO2-1200HC-HE	—	868	—	902	—	951	ps
		MachXO2-2000HC-HE	—	867	—	897	—	941	ps
		MachXO2-4000HC-HE	—	865	—	892	—	931	ps
		MachXO2-7000HC-HE	—	902	—	942	—	989	ps
Edge Clock									
f_{MAX_EDGE}[8]	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	400	—	333	—	278	MHz
Pin-LUT-Pin Propagation Delay									
t_{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	—	6.72	—	6.96	—	7.24	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t_{CO}	Clock to Output – PIO Output Register	MachXO2-256HC-HE	—	7.13	—	7.30	—	7.57	ns
		MachXO2-640HC-HE	—	7.15	—	7.30	—	7.57	ns
		MachXO2-1200HC-HE	—	7.44	—	7.64	—	7.94	ns
		MachXO2-2000HC-HE	—	7.46	—	7.66	—	7.96	ns
		MachXO2-4000HC-HE	—	7.51	—	7.71	—	8.01	ns
		MachXO2-7000HC-HE	—	7.54	—	7.75	—	8.06	ns
t_{SU}	Clock to Data Setup – PIO Input Register	MachXO2-256HC-HE	–0.06	—	–0.06	—	–0.06	—	ns
		MachXO2-640HC-HE	–0.06	—	–0.06	—	–0.06	—	ns
		MachXO2-1200HC-HE	–0.17	—	–0.17	—	–0.17	—	ns
		MachXO2-2000HC-HE	–0.20	—	–0.20	—	–0.20	—	ns
		MachXO2-4000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-7000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	MachXO2-256HC-HE	1.75	—	1.95	—	2.16	—	ns
		MachXO2-640HC-HE	1.75	—	1.95	—	2.16	—	ns
		MachXO2-1200HC-HE	1.88	—	2.12	—	2.36	—	ns
		MachXO2-2000HC-HE	1.89	—	2.13	—	2.37	—	ns
		MachXO2-4000HC-HE	1.94	—	2.18	—	2.43	—	ns
		MachXO2-7000HC-HE	1.98	—	2.23	—	2.49	—	ns

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-256HC-HE	1.42	—	1.59	—	1.96	—	ns
		MachXO2-640HC-HE	1.41	—	1.58	—	1.96	—	ns
		MachXO2-1200HC-HE	1.63	—	1.79	—	2.17	—	ns
		MachXO2-2000HC-HE	1.61	—	1.76	—	2.13	—	ns
		MachXO2-4000HC-HE	1.66	—	1.81	—	2.19	—	ns
		MachXO2-7000HC-HE	1.53	—	1.67	—	2.03	—	ns
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-256HC-HE	–0.24	—	–0.24	—	–0.24	—	ns
		MachXO2-640HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-1200HC-HE	–0.24	—	–0.24	—	–0.24	—	ns
		MachXO2-2000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000HC-HE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-7000HC-HE	–0.21	—	–0.21	—	–0.21	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices	—	388	—	323	—	269	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
t_{COE}	Clock to Output – PIO Output Register	MachXO2-1200HC-HE	—	7.53	—	7.76	—	8.10	ns
		MachXO2-2000HC-HE	—	7.53	—	7.76	—	8.10	ns
		MachXO2-4000HC-HE	—	7.45	—	7.68	—	8.00	ns
		MachXO2-7000HC-HE	—	7.53	—	7.76	—	8.10	ns
t_{SUE}	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
		MachXO2-2000HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
		MachXO2-4000HC-HE	–0.16	—	–0.16	—	–0.16	—	ns
		MachXO2-7000HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
t_{HE}	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	1.97	—	2.24	—	2.52	—	ns
		MachXO2-2000HC-HE	1.97	—	2.24	—	2.52	—	ns
		MachXO2-4000HC-HE	1.89	—	2.16	—	2.43	—	ns
		MachXO2-7000HC-HE	1.97	—	2.24	—	2.52	—	ns
t_{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	1.56	—	1.69	—	2.05	—	ns
		MachXO2-2000HC-HE	1.56	—	1.69	—	2.05	—	ns
		MachXO2-4000HC-HE	1.74	—	1.88	—	2.25	—	ns
		MachXO2-7000HC-HE	1.66	—	1.81	—	2.17	—	ns
t_{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-2000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000HC-HE	–0.34	—	–0.34	—	–0.34	—	ns
		MachXO2-7000HC-HE	–0.29	—	–0.29	—	–0.29	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t_{COPLL}	Clock to Output – PIO Output Register	MachXO2-1200HC-HE	—	5.97	—	6.00	—	6.13	ns
		MachXO2-2000HC-HE	—	5.98	—	6.01	—	6.14	ns
		MachXO2-4000HC-HE	—	5.99	—	6.02	—	6.16	ns
		MachXO2-7000HC-HE	—	6.02	—	6.06	—	6.20	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	0.36	—	0.36	—	0.65	—	ns
		MachXO2-2000HC-HE	0.36	—	0.36	—	0.63	—	ns
		MachXO2-4000HC-HE	0.35	—	0.35	—	0.62	—	ns
		MachXO2-7000HC-HE	0.34	—	0.34	—	0.59	—	ns

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HPLL}	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	0.41	—	0.48	—	0.55	—	ns
		MachXO2-2000HC-HE	0.42	—	0.49	—	0.56	—	ns
		MachXO2-4000HC-HE	0.43	—	0.50	—	0.58	—	ns
		MachXO2-7000HC-HE	0.46	—	0.54	—	0.62	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	2.88	—	3.19	—	3.72	—	ns
		MachXO2-2000HC-HE	2.87	—	3.18	—	3.70	—	ns
		MachXO2-4000HC-HE	2.96	—	3.28	—	3.81	—	ns
		MachXO2-7000HC-HE	3.05	—	3.35	—	3.87	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-2000HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-4000HC-HE	–0.87	—	–0.87	—	–0.87	—	ns
		MachXO2-7000HC-HE	–0.91	—	–0.91	—	–0.91	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.317	—	0.344	—	0.368	UI
t_{DVE}	Input Data Hold After CLK		0.742	—	0.702	—	0.668	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	All MachXO2 devices, all sides	0.566	—	0.560	—	0.538	—	ns
t_{HO}	Input Data Hold After CLK		0.778	—	0.879	—	1.090	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.316	—	0.342	—	0.364	UI
t_{DVE}	Input Data Hold After CLK		0.710	—	0.675	—	0.679	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.233	—	0.219	—	0.198	—	ns
t_{HO}	Input Data Hold After CLK		0.287	—	0.287	—	0.344	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only.[11]	—	0.290	—	0.320	—	0.345	UI
t_{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	0.703	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only.[11]	0.233	—	0.219	—	0.198	—	ns
t_{HO}	Input Data Hold After ECLK		0.287	—	0.287	—	0.344	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1)[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only.[11]	—	0.290	—	0.320	—	0.345	UI
t_{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	0.703	—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	All MachXO2 devices, all sides.	—	0.520	—	0.550	—	0.580	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.520	—	0.550	—	0.580	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK frequency		—	150	—	125	—	104	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	All MachXO2 devices, all sides.	1.210	—	1.510	—	1.870	—	ns
t_{DVA}	Output Data Valid After CLK Output		1.210	—	1.510	—	1.870	—	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		—	150	—	125	—	104	MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.535	—	0.670	—	0.830	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	0.830	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.455	—	0.570	—	0.710	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.455	—	0.570	—	0.710	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[9, 12]									
t_{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.160	—	0.180	—	0.200	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.160	—	0.180	—	0.200	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.369	—	0.395	—	0.421	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.529	—	0.530	—	0.527	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM LPDDR Serial Data Speed		—	280	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	140	—	125	—	104	MHz
f_{LPDDR}	LPDDR Data Transfer Rate		0	280	0	250	0	208	Mbps
DDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.350	—	0.387	—	0.414	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.545	—	0.538	—	0.532	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	150	—	125	—	104	MHz
f_{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps
DDR2[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.360	—	0.378	—	0.406	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.555	—	0.549	—	0.542	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	150	—	125	—	104	MHz
f_{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
7. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps (–6), 113 ps (–5), 120 ps (–4).
8. This number for general purpose usage. Duty cycle tolerance is +/– 10%.
9. Duty cycle is +/–5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32 QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

MachXO2 External Switching Characteristics – ZE Devices[1, 2, 3, 4, 5, 6, 7]

Over Recommended Operating Conditions

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f_{MAX_PRI}[8]	Frequency for Primary Clock Tree	All MachXO2 devices	—	150	—	125	—	104	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	1.00	—	1.20	—	1.40	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO2-256ZE	—	1250	—	1272	—	1296	ps
		MachXO2-640ZE	—	1161	—	1183	—	1206	ps
		MachXO2-1200ZE	—	1213	—	1267	—	1322	ps
		MachXO2-2000ZE	—	1204	—	1250	—	1296	ps
		MachXO2-4000ZE	—	1195	—	1233	—	1269	ps
		MachXO2-7000ZE	—	1243	—	1268	—	1296	ps
Edge Clock									
f_{MAX_EDGE}[8]	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	210	—	175	—	146	MHz
Pin-LUT-Pin Propagation Delay									
t_{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	—	9.35	—	9.78	—	10.21	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t_{CO}	Clock to Output – PIO Output Register	MachXO2-256ZE	—	10.46	—	10.86	—	11.25	ns
		MachXO2-640ZE	—	10.52	—	10.92	—	11.32	ns
		MachXO2-1200ZE	—	11.24	—	11.68	—	12.12	ns
		MachXO2-2000ZE	—	11.27	—	11.71	—	12.16	ns
		MachXO2-4000ZE	—	11.28	—	11.78	—	12.28	ns
		MachXO2-7000ZE	—	11.22	—	11.76	—	12.30	ns
t_{SU}	Clock to Data Setup – PIO Input Register	MachXO2-256ZE	–0.21	—	–0.21	—	–0.21	—	ns
		MachXO2-640ZE	–0.22	—	–0.22	—	–0.22	—	ns
		MachXO2-1200ZE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-2000ZE	–0.27	—	–0.27	—	–0.27	—	ns
		MachXO2-4000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-7000ZE	–0.33	—	–0.33	—	–0.33	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	MachXO2-256ZE	3.96	—	4.25	—	4.65	—	ns
		MachXO2-640ZE	4.01	—	4.31	—	4.71	—	ns
		MachXO2-1200ZE	3.95	—	4.29	—	4.73	—	ns
		MachXO2-2000ZE	3.94	—	4.29	—	4.74	—	ns
		MachXO2-4000ZE	3.96	—	4.36	—	4.87	—	ns
		MachXO2-7000ZE	3.93	—	4.37	—	4.91	—	ns

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-256ZE	2.62	—	2.91	—	3.14	—	ns
		MachXO2-640ZE	2.56	—	2.85	—	3.08	—	ns
		MachXO2-1200ZE	2.30	—	2.57	—	2.79	—	ns
		MachXO2-2000ZE	2.25	—	2.50	—	2.70	—	ns
		MachXO2-4000ZE	2.39	—	2.60	—	2.76	—	ns
		MachXO2-7000ZE	2.17	—	2.33	—	2.43	—	ns
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-256ZE	–0.44	—	–0.44	—	–0.44	—	ns
		MachXO2-640ZE	–0.43	—	–0.43	—	–0.43	—	ns
		MachXO2-1200ZE	–0.28	—	–0.28	—	–0.28	—	ns
		MachXO2-2000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-4000ZE	–0.34	—	–0.34	—	–0.34	—	ns
		MachXO2-7000ZE	–0.21	—	–0.21	—	–0.21	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices	—	150	—	125	—	104	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
t_{COE}	Clock to Output – PIO Output Register	MachXO2-1200ZE	—	11.10	—	11.51	—	11.91	ns
		MachXO2-2000ZE	—	11.10	—	11.51	—	11.91	ns
		MachXO2-4000ZE	—	10.89	—	11.28	—	11.67	ns
		MachXO2-7000ZE	—	11.10	—	11.51	—	11.91	ns
t_{SUE}	Clock to Data Setup – PIO Input Register	MachXO2-1200ZE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-2000ZE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000ZE	–0.15	—	–0.15	—	–0.15	—	ns
		MachXO2-7000ZE	–0.23	—	–0.23	—	–0.23	—	ns
t_{HE}	Clock to Data Hold – PIO Input Register	MachXO2-1200ZE	3.81	—	4.11	—	4.52	—	ns
		MachXO2-2000ZE	3.81	—	4.11	—	4.52	—	ns
		MachXO2-4000ZE	3.60	—	3.89	—	4.28	—	ns
		MachXO2-7000ZE	3.81	—	4.11	—	4.52	—	ns
t_{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200ZE	2.78	—	3.11	—	3.40	—	ns
		MachXO2-2000ZE	2.78	—	3.11	—	3.40	—	ns
		MachXO2-4000ZE	3.11	—	3.48	—	3.79	—	ns
		MachXO2-7000ZE	2.94	—	3.30	—	3.60	—	ns
t_{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200ZE	–0.29	—	-0.29	—	–0.29	—	ns
		MachXO2-2000ZE	–0.29	—	-0.29	—	–0.29	—	ns
		MachXO2-4000ZE	–0.46	—	-0.46	—	–0.46	—	ns
		MachXO2-7000ZE	–0.37	—	-0.37	—	–0.37	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t_{COPLL}	Clock to Output – PIO Output Register	MachXO2-1200ZE	—	7.95	—	8.07	—	8.19	ns
		MachXO2-2000ZE	—	7.97	—	8.10	—	8.22	ns
		MachXO2-4000ZE	—	7.98	—	8.10	—	8.23	ns
		MachXO2-7000ZE	—	8.02	—	8.14	—	8.26	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO2-1200ZE	0.85	—	0.85	—	0.89	—	ns
		MachXO2-2000ZE	0.84	—	0.84	—	0.86	—	ns
		MachXO2-4000ZE	0.84	—	0.84	—	0.85	—	ns
		MachXO2-7000ZE	0.83	—	0.83	—	0.81	—	ns

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HPLL}	Clock to Data Hold – PIO Input Register	MachXO2-1200ZE	0.66	—	0.68	—	0.80	—	ns
		MachXO2-2000ZE	0.68	—	0.70	—	0.83	—	ns
		MachXO2-4000ZE	0.68	—	0.71	—	0.84	—	ns
		MachXO2-7000ZE	0.73	—	0.74	—	0.87	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200ZE	5.14	—	5.69	—	6.20	—	ns
		MachXO2-2000ZE	5.11	—	5.67	—	6.17	—	ns
		MachXO2-4000ZE	5.27	—	5.84	—	6.35	—	ns
		MachXO2-7000ZE	5.15	—	5.71	—	6.23	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200ZE	–1.36	—	–1.36	—	–1.36	—	ns
		MachXO2-2000ZE	–1.35	—	–1.35	—	–1.35	—	ns
		MachXO2-4000ZE	–1.43	—	–1.43	—	–1.43	—	ns
		MachXO2-7000ZE	–1.41	—	–1.41	—	–1.41	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.382	—	0.401	—	0.417	UI
t_{DVE}	Input Data Hold After CLK		0.670	—	0.684	—	0.693	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	All MachXO2 devices, all sides	1.319	—	1.412	—	1.462	—	ns
t_{HO}	Input Data Hold After CLK		0.717	—	1.010	—	1.340	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.361	—	0.346	—	0.334	UI
t_{DVE}	Input Data Hold After CLK		0.602	—	0.625	—	0.648	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.472	—	0.672	—	0.865	—	ns
t_{HO}	Input Data Hold After CLK		0.363	—	0.501	—	0.743	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input - GDDRX4_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.307	—	0.316	—	0.326	UI
t_{DVE}	Input Data Hold After ECLK		0.662	—	0.650	—	0.649	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.434	—	0.535	—	0.630	—	ns
t_{HO}	Input Data Hold After ECLK		0.385	—	0.395	—	0.463	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz
7:1 LVDS Inputs – GDDR71_RX.ECLK.7.1[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.307	—	0.316	—	0.326	UI
t_{DVE}	Input Data Hold After ECLK		0.662	—	0.650	—	0.649	—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	210	—	176	—	146	MHz
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	60	—	50	—	42	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	All MachXO2 devices, all sides	—	0.850	—	0.910	—	0.970	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.850	—	0.910	—	0.970	ns
f_{DATA}	DDRX1 Output Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK frequency		—	70	—	58	—	49	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	All MachXO2 devices, all sides	2.720	—	3.380	—	4.140	—	ns
t_{DVA}	Output Data Valid After CLK Output		2.720	—	3.380	—	4.140	—	ns
f_{DATA}	DDRX1 Output Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		—	70	—	58	—	49	MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	—	0.270	—	0.300	—	0.330	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.270	—	0.300	—	0.330	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	1.445	—	1.760	—	2.140	—	ns
t_{DVA}	Output Data Valid After CLK Output		1.445	—	1.760	—	2.140	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	—	0.270	—	0.300	—	0.330	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.270	—	0.300	—	0.330	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	0.873	—	1.067	—	1.319	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.873	—	1.067	—	1.319	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[9, 12]									
t_{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.240	—	0.270	—	0.300	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.240	—	0.270	—	0.300	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	420	—	352	—	292	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	210	—	176	—	146	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	60	—	50	—	42	MHz

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.349	—	0.381	—	0.396	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.630	—	0.613	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM LPDDR Serial Data Speed		—	120	—	110	—	96	Mbps
f_{SCLK}	SCLK Frequency		—	60	—	55	—	48	MHz
f_{LPDDR}	LPDDR Data Transfer Rate		0	120	0	110	0	96	Mbps
DDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.347	—	0.374	—	0.393	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.637	—	0.616	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f_{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f_{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps
DDR2[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.372	—	0.394	—	0.410	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.690	—	0.658	—	0.618	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f_{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f_{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
7. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 167 ps (–3), 182 ps (–2), 195 ps (–1).
8. This number for general purpose usage. Duty cycle tolerance is +/–10%.
9. Duty cycle is +/– 5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

Figure 3-5. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms

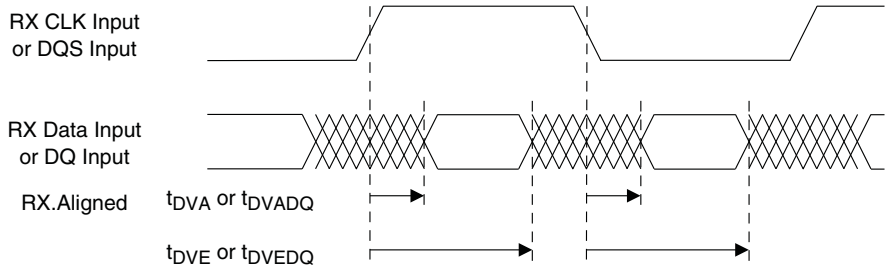


Figure 3-6. Receiver RX.CLK.Centered Waveforms

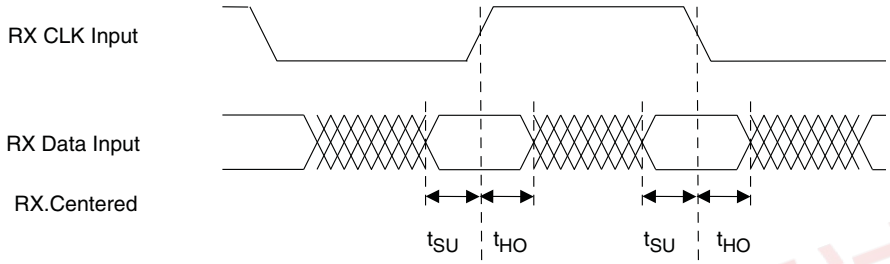


Figure 3-7. Transmitter TX.CLK.Aligned Waveforms

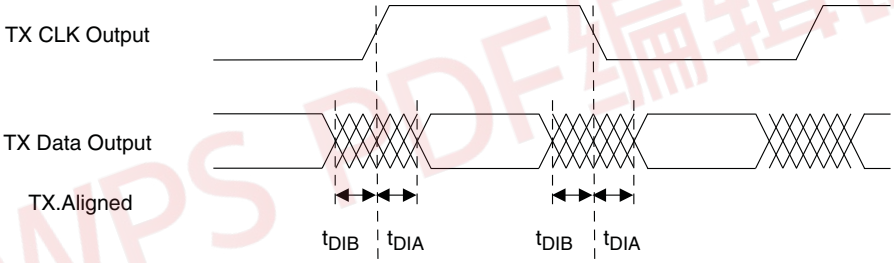


Figure 3-8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms

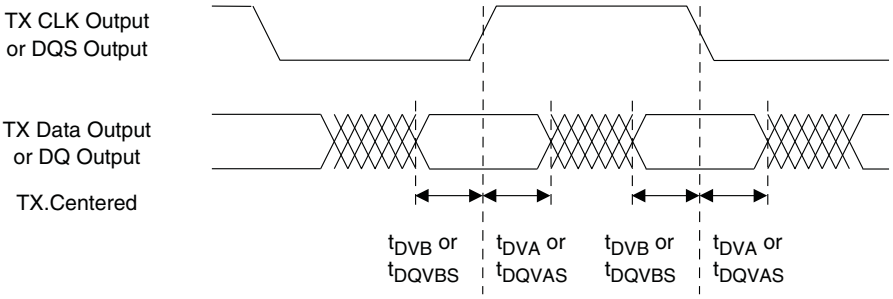


Figure 3-9. GDDR71 Video Timing Waveforms

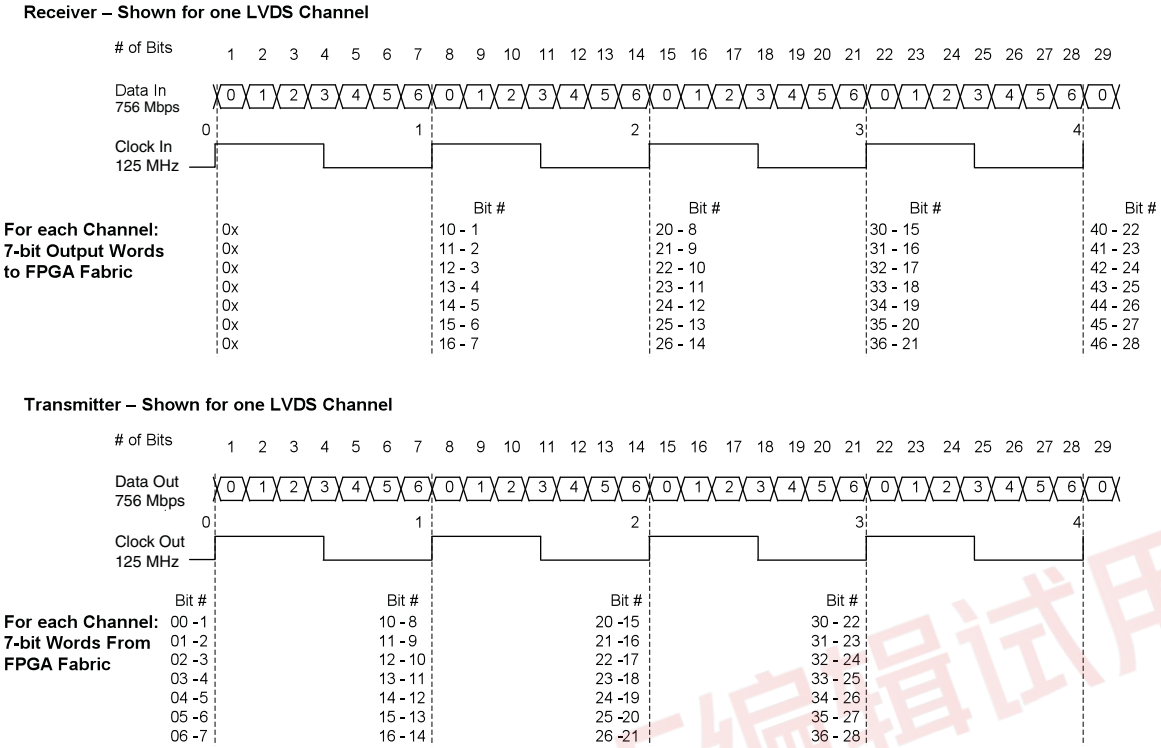


Figure 3-10. Receiver GDDR71_RX. Waveforms

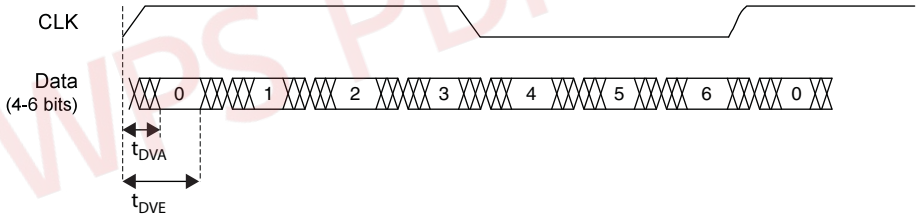
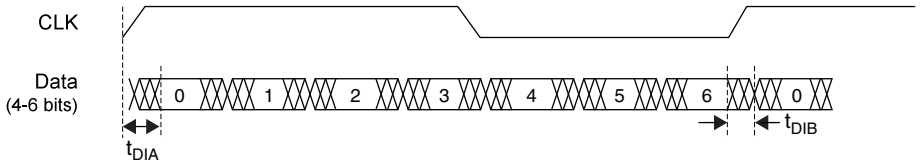


Figure 3-11. Transmitter GDDR71_TX. Waveforms



sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)		1.5625	400	MHz
f_{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f_{VCO}	PLL VCO Frequency		200	800	MHz
f_{PFD}	Phase Detector Input Frequency		7	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Without duty trim selected[3]	45	55	%
t_{DT_TRIM}[7]	Edge Duty Trim Accuracy		–75	75	%
t_{PH}[4]	Output Phase Accuracy		–6	6	%
t_{OPJIT}[1, 8]	Output Clock Period Jitter	f_{OUT} > 100 MHz	—	150	ps p-p
		f_{OUT} < 100 MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} > 100 MHz	—	180	ps p-p
		f_{OUT} < 100 MHz	—	0.009	UIPP
	Output Clock Phase Jitter	f_{PFD} > 100 MHz	—	160	ps p-p
		f_{PFD} < 100 MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	230	ps p-p
		f_{OUT} < 100 MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	230	ps p-p
		f_{OUT} < 100 MHz	—	0.12	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	–120	120	ps
t_W	Output Clock Pulse Width	At 90% or 10%[3]	0.9	—	ns
t_{LOCK}[2, 5]	PLL Lock-in Time		—	15	ms
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[6]	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{STABLE}[5]	STANDBY High to PLL Stable		—	15	ms
t_{RST}	RST/RESETM Pulse Width		1	—	ns
t_{RSTREC}	RST Recovery Time		1	—	ns
t_{RST_DIV}	RESETC/D Pulse Width		10	—	ns
t_{RSTREC_DIV}	RESETC/D Recovery Time		1	—	ns
$t_{ROTATE-SETUP}$	PHASESTEP Setup Time		10	—	ns

sysCLOCK PLL Timing (Continued)

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
t_{ROTATE_WD}	PHASESTEP Pulse Width		4	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide for more details.
5. At minimum $f_{PFD.}$ As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

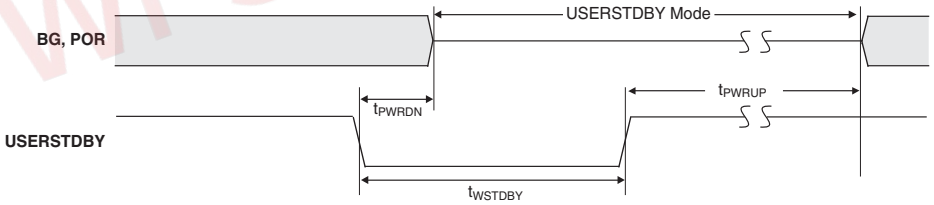
MachXO2 Oscillator Output Frequency

Symbol	Parameter	Min.	Typ.	Max	Units
f_{MAX}	Oscillator Output Frequency (Commercial Grade Devices, 0 to 85°C)	125.685	133	140.315	MHz
	Oscillator Output Frequency (Industrial Grade Devices, –40 °C to 100 °C)	124.355	133	141.645	MHz
t_{DT}	Output Clock Duty Cycle	43	50	57	%
t_{OPJIT}[1]	Output Clock Period Jitter	0.01	0.012	0.02	UIPP
$t_{STABLEOSC}$	STDBY Low to Oscillator Stable	0.01	0.05	0.1	µs

1. Output Clock Period Jitter specified at 133 MHz. The values for lower frequencies will be smaller UIPP. The typical value for 133 MHz is 95 ps and for 2.08 MHz the typical value is 1.54 ns.

MachXO2 Standby Mode Timing – HC/HE Devices

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	USERSTDBY High to Stop	All	—	—	9	ns
t_{PWRUP}	USERSTDBY Low to Power Up	LCMXO2-256		—		µs
		LCMXO2-640		—		µs
		LCMXO2-640U		—		µs
		LCMXO2-1200	20	—	50	µs
		LCMXO2-1200U		—		µs
		LCMXO2-2000		—		µs
		LCMXO2-2000U		—		µs
		LCMXO2-4000		—		µs
		LCMXO2-7000		—		µs
t_{WSTDBY}	USERSTDBY Pulse Width	All	18	—	—	ns



MachXO2 Standby Mode Timing – ZE Devices

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	USERSTDBY High to Stop	All	—	—	13	ns
t_{PWRUP}	USERSTDBY Low to Power Up	LCMXO2-256		—		µs
		LCMXO2-640		—		µs
		LCMXO2-1200	20	—	50	µs
		LCMXO2-2000		—		µs
		LCMXO2-4000		—		µs
		LCMXO2-7000		—		µs
t_{WSTDBY}	USERSTDBY Pulse Width	All	19	—	—	ns
$t_{BNDGAPSTBL}$	USERSTDBY High to Bandgap Stable	All	—	—	15	ns

Flash Download Time[1, 2]

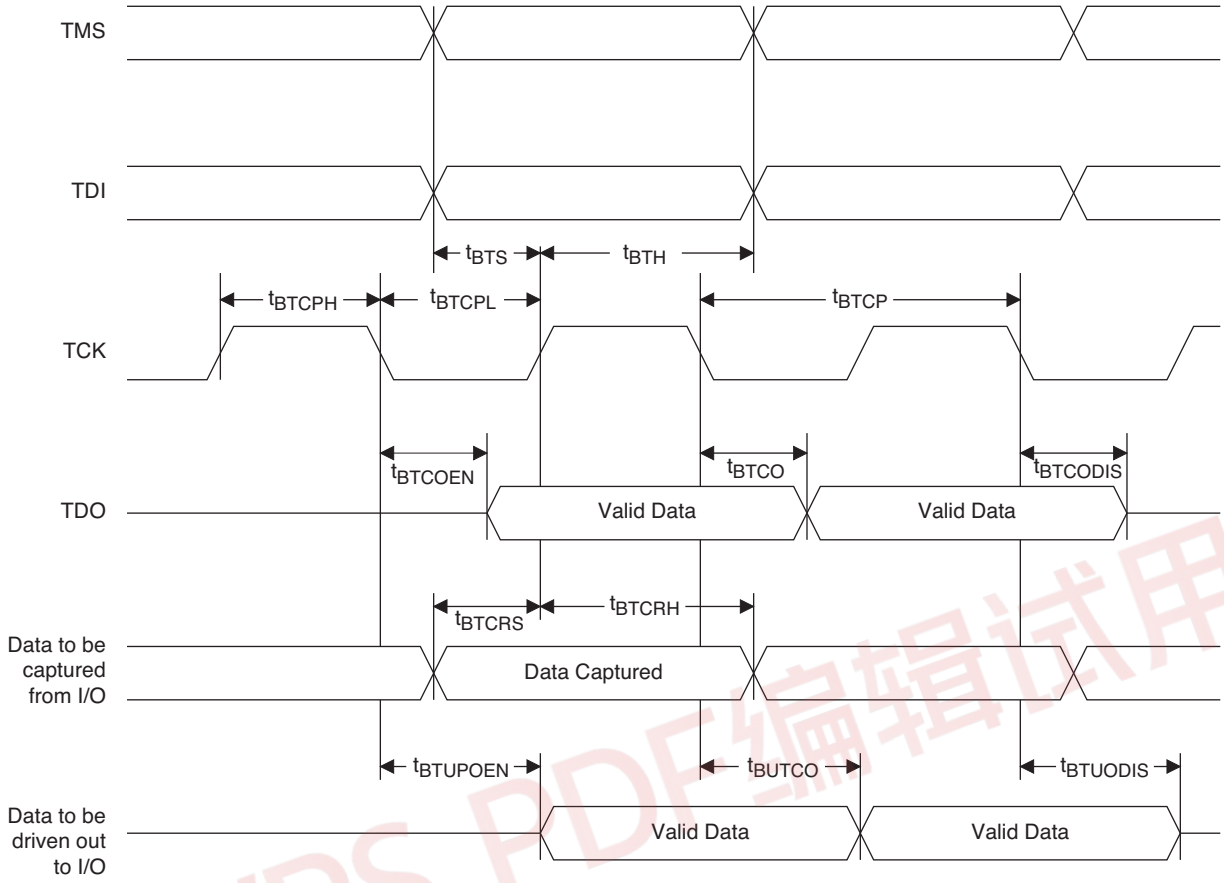
Symbol	Parameter	Device	Typ.	Units
$t_{REFRESH}$	POR to Device I/O Active	LCMXO2-256	0.6	ms
		LCMXO2-640	1.0	ms
		LCMXO2-640U	1.9	ms
		LCMXO2-1200	1.9	ms
		LCMXO2-1200U	1.4	ms
		LCMXO2-2000	1.4	ms
		LCMXO2-2000U	2.4	ms
		LCMXO2-4000	2.4	ms
		LCMXO2-7000	3.8	ms

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.
2. The Flash download time is measured starting from the maximum voltage of POR trip point.

JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	20	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-12. JTAG Port Timing Waveforms



sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Modes					
t_{PRGM}	PROGRAMN low pulse accept		55	—	ns
t_{PRGMJ}	PROGRAMN low pulse rejection		—	25	ns
t_{INITL}	INITN low time	LCMXO2-256	—	30	µs
		LCMXO2-640	—	35	µs
		LCMXO2-640U/ LCMXO2-1200	—	55	µs
		LCMXO2-1200U/ LCMXO2-2000	—	70	µs
		LCMXO2-2000U/ LCMXO2-4000	—	105	µs
		LCMXO2-7000	—	130	µs
$t_{DPPINIT}$	PROGRAMN low to INITN low		—	150	ns
$t_{DPPDONE}$	PROGRAMN low to DONE low		—	150	ns
t_{IODISS}	PROGRAMN low to I/O disable		—	120	ns
Slave SPI					
f_{MAX}	CCLK clock frequency		—	66	MHz
t_{CCLKH}	CCLK clock pulse width high		7.5	—	ns
t_{CCLKL}	CCLK clock pulse width low		7.5	—	ns
t_{STSU}	CCLK setup time		2	—	ns
t_{STH}	CCLK hold time		0	—	ns
t_{STCO}	CCLK falling edge to valid output		—	10	ns
t_{STOZ}	CCLK falling edge to valid disable		—	10	ns
t_{STOV}	CCLK falling edge to valid enable		—	10	ns
t_{SCS}	Chip select high time		25	—	ns
t_{SCSS}	Chip select setup time		3	—	ns
t_{SCSH}	Chip select hold time		3	—	ns
Master SPI					
f_{MAX}	MCLK clock frequency		—	133	MHz
t_{MCLKH}	MCLK clock pulse width high		3.75	—	ns
t_{MCLKL}	MCLK clock pulse width low		3.75	—	ns
t_{STSU}	MCLK setup time		5	—	ns
t_{STH}	MCLK hold time		1	—	ns
t_{CSSPI}	INITN high to chip select low		100	200	ns
t_{MCLK}	INITN high to first MCLK edge		0.75	1	µs

I²C Port Timing Specifications[1, 2]

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCL clock frequency	—	400	kHz

1. MachXO2 supports the following modes:
   • Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
   • Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
2. Refer to the I²C specification for timing requirements.

SPI Port Timing Specifications[1]

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCK clock frequency	—	45	MHz

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

Switching Test Conditions

Figure 3-13 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-5.

Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards

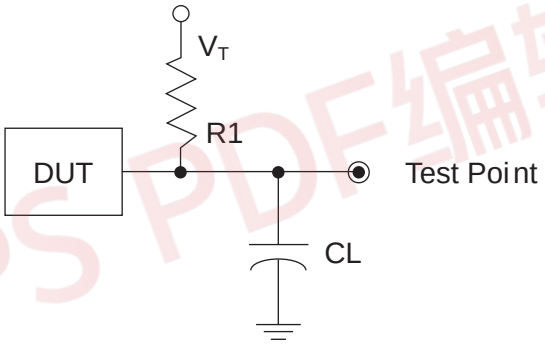


Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R1	CL	Timing Ref.	VT
LVTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5 V	V_{OL}
LVTTL and LVCMOS 3.3 (Z -> L)			1.5 V	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVTTL + LVCMOS (H -> Z)			V_{OH} – 0.15 V	V_{OL}
LVTTL + LVCMOS (L -> Z)			V_{OL} – 0.15 V	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the group to which the pad is connected. Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic. During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.
NC	—	No connect.
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together. For QFN 48 package, the exposed die pad is the device ground.
VCC	—	V_{CC} – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIOx	—	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.
PLL and Clock Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)		
[LOC]_GPLL[T, C]_IN	—	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.
Test and Programming (Dual function pins used for test access port and during sysCONFIG™)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
JTAGENB	I	Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then: If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O. If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.
Configuration (Dual function pins used during sysCONFIG)		
PROGRAMN	I	Initiates configuration sequence when asserted low. During configuration, or when reserved as PROGRAMN in user mode, this pin always has an active pull-up.

Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, or when reserved as INITn in user mode, this pin has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress. During configuration, or when reserved as DONE in user mode, this pin has an active pull-up.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.
SCL	I/O	Slave I^2C clock input and master I^2C clock output.
SDA	I/O	Slave I^2C data input and master I^2C data output.

Pinout Information Summary

	MachXO2-256					MachXO2-640			MachXO2-640U
	32 QFN[1]	48 QFN[3]	64 ucBGA	100 TQFP	132 csBGA	48 QFN[3]	100 TQFP	132 csBGA	144 TQFP
General Purpose I/O per Bank									
Bank 0	8	10	9	13	13	10	18	19	27
Bank 1	2	10	12	14	14	10	20	20	26
Bank 2	9	10	11	14	14	10	20	20	28
Bank 3	2	10	12	14	14	10	20	20	26
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Single Ended I/O	21	40	44	55	55	40	78	79	107
Differential I/O per Bank									
Bank 0	4	5	5	7	7	5	9	10	14
Bank 1	1	5	6	7	7	5	10	10	13
Bank 2	4	5	5	7	7	5	10	10	14
Bank 3	1	5	6	7	7	5	10	10	13
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Differential I/O	10	20	22	28	28	20	39	40	54
Dual Function I/O	22	25	27	29	29	25	29	29	33
High-speed Differential I/O									
Bank 0	0	0	0	0	0	0	0	0	7
Gearboxes									
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	0	0	0	0	0	0	0	0	7
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	0	0	0	0	0	0	0	0	7
DQS Groups									
Bank 1	0	0	0	0	0	0	0	0	2
VCCIO Pins									
Bank 0	2	2	2	2	2	2	2	2	3
Bank 1	1	1	2	2	2	1	2	2	3
Bank 2	2	2	2	2	2	2	2	2	3
Bank 3	1	1	2	2	2	1	2	2	3
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
VCC	2	2	2	2	2	2	2	2	4
GND[2]	2	1	8	8	8	1	8	10	12
NC	0	0	1	26	58	0	3	32	8
Reserved for Configuration	1	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	32	49	64	100	132	49	100	132	144

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.
2. For 48 QFN package, exposed die pad is the device ground.
3. 48-pin QFN information is 'Advanced'.

	MachXO2-1200					MachXO2-1200U
	100 TQFP	132 csBGA	144 TQFP	25 WLCSP	32 QFN[1]	256 ftBGA
General Purpose I/O per Bank						
Bank 0	18	25	27	11	9	50
Bank 1	21	26	26	0	2	52
Bank 2	20	28	28	7	9	52
Bank 3	20	25	26	0	2	16
Bank 4	0	0	0	0	0	16
Bank 5	0	0	0	0	0	20
Total General Purpose Single Ended I/O	79	104	107	18	22	206
Differential I/O per Bank						
Bank 0	9	13	14	5	4	25
Bank 1	10	13	13	0	1	26
Bank 2	10	14	14	2	4	26
Bank 3	10	12	13	0	1	8
Bank 4	0	0	0	0	0	8
Bank 5	0	0	0	0	0	10
Total General Purpose Differential I/O	39	52	54	7	10	103
Dual Function I/O	31	33	33	18	22	33
High-speed Differential I/O						
Bank 0	4	7	7	0	0	14
Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	4	7	7	0	0	14
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	5	7	7	0	2	14
DQS Groups						
Bank 1	1	2	2	0	0	2
VCCIO Pins						
Bank 0	2	3	3	1	2	4
Bank 1	2	3	3	0	1	4
Bank 2	2	3	3	1	2	4
Bank 3	3	3	3	0	1	1
Bank 4	0	0	0	0	0	2
Bank 5	0	0	0	0	0	1
VCC	2	4	4	2	2	8
GND	8	10	12	2	2	24
NC	1	1	8	0	0	1
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	100	132	144	25	32	256

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.

	MachXO2-2000						MachXO2-2000U
	49 WLCSP	100 TQFP	132 csBGA	144 TQFP	256 caBGA	256 ftBGA	484 ftBGA
General Purpose I/O per Bank							
Bank 0	19	18	25	27	50	50	70
Bank 1	0	21	26	28	52	52	68
Bank 2	13	20	28	28	52	52	72
Bank 3	0	6	7	8	16	16	24
Bank 4	0	6	8	10	16	16	16
Bank 5	6	8	10	10	20	20	28
Total General Purpose Single-Ended I/O	38	79	104	111	206	206	278
Differential I/O per Bank							
Bank 0	7	9	13	14	25	25	35
Bank 1	0	10	13	14	26	26	34
Bank 2	6	10	14	14	26	26	36
Bank 3	0	3	3	4	8	8	12
Bank 4	0	3	4	5	8	8	8
Bank 5	3	4	5	5	10	10	14
Total General Purpose Differential I/O	16	39	52	56	103	103	139
Dual Function I/O	24	31	33	33	33	33	37
High-speed Differential I/O							
Bank 0	5	4	8	9	14	14	18
Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	4	8	9	14	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	10	14	14	14	14	18
DQS Groups							
Bank 1	0	1	2	2	2	2	2
VCCIO Pins							
Bank 0	2	2	3	3	4	4	10
Bank 1	0	2	3	3	4	4	10
Bank 2	1	2	3	3	4	4	10
Bank 3	0	1	1	1	1	1	3
Bank 4	0	1	1	1	2	2	4
Bank 5	1	1	1	1	1	1	3
VCC	2	2	4	4	8	8	12
GND	4	8	10	12	24	24	48
NC	0	1	1	4	1	1	105
Reserved for Configuration	1	1	1	1	v	1	1
Total Count of Bonded Pins	39	100	132	144	256	256	484

	MachXO2-4000							
	84 QFN	132 csBGA	144 TQFP	184 csBGA	256 caBGA	256 ftBGA	332 caBGA	484 fpBGA
General Purpose I/O per Bank								
Bank 0	27	25	27	37	50	50	68	70
Bank 1	10	26	29	37	52	52	68	68
Bank 2	22	28	29	39	52	52	70	72
Bank 3	0	7	9	10	16	16	24	24
Bank 4	9	8	10	12	16	16	16	16
Bank 5	0	10	10	15	20	20	28	28
Total General Purpose Single Ended I/O	68	104	114	150	206	206	274	278
Differential I/O per Bank								
Bank 0	13	13	14	18	25	25	34	35
Bank 1	4	13	14	18	26	26	34	34
Bank 2	11	14	14	19	26	26	35	36
Bank 3	0	3	4	4	8	8	12	12
Bank 4	4	4	5	6	8	8	8	8
Bank 5	0	5	5	7	10	10	14	14
Total General Purpose Differential I/O	32	52	56	72	103	103	137	139
Dual Function I/O	28	37	37	37	37	37	37	37
High-speed Differential I/O								
Bank 0	8	8	9	8	18	18	18	18
Gearboxes								
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	8	8	9	9	18	18	18	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	11	14	14	12	18	18	18	18
DQS Groups								
Bank 1	1	2	2	2	2	2	2	2
VCCIO Pins								
Bank 0	3	3	3	3	4	4	4	10
Bank 1	1	3	3	3	4	4	4	10
Bank 2	2	3	3	3	4	4	4	10
Bank 3	1	1	1	1	1	1	2	3
Bank 4	1	1	1	1	2	2	1	4
Bank 5	1	1	1	1	1	1	2	3
VCC	4	4	4	4	8	8	8	12
GND	4	10	12	16	24	24	27	48
NC	1	1	1	1	1	1	5	105
Reserved for configuration	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	84	132	144	184	256	256	332	484

	MachXO2-7000					
	144 TQFP	**256 caBGA**	**256 ftBGA**	**332 caBGA**	**400 caBGA**	**484 fpBGA**
General Purpose I/O per Bank						
Bank 0	27	50	50	68	83	82
Bank 1	29	52	52	70	84	84
Bank 2	29	52	52	70	84	84
Bank 3	9	16	16	24	28	28
Bank 4	10	16	16	16	24	24
Bank 5	10	20	20	30	32	32
Total General Purpose Single Ended I/O	114	206	206	278	335	334
Differential I/O per Bank						
Bank 0	14	25	25	34	42	41
Bank 1	14	26	26	35	42	42
Bank 2	14	26	26	35	42	42
Bank 3	4	8	8	12	14	14
Bank 4	5	8	8	8	12	12
Bank 5	5	10	10	15	16	16
Total General Purpose Differential I/O	56	103	103	139	168	167
Dual Function I/O	37	37	37	37	37	37
High-speed Differential I/O						
Bank 0	9	20	20	21	21	21
Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	9	20	20	21	21	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	14	20	20	21	21	21
DQS Groups						
Bank 1	2	2	2	2	2	2
VCCIO Pins						
Bank 0	3	4	4	4	5	10
Bank 1	3	4	4	4	5	10
Bank 2	3	4	4	4	5	10
Bank 3	1	1	1	2	2	3
Bank 4	1	2	2	1	2	4
Bank 5	1	1	1	2	2	3
VCC	4	8	8	8	10	12
GND	12	24	24	27	33	48
NC	1	1	1	1	0	49
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	144	256	256	332	400	484

For Further Information

For further information regarding logic signal connections for various packages please refer to the MachXO2 Device Pinout Files.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Users must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1198, Power Estimation and Management for MachXO2 Devices
- The Power Calculator tool is included with the Lattice design tools, or as a standalone download from www.latticesemi.com/software

MachXO2 Family Data Sheet Ordering Information

March 2017 Data Sheet DS1035

MachXO2 Part Number Description

LCMXO2 – XXXX X X X – X XXXXXX X XX XX

Device Family
MachXO2 PLD

Logic Capacity
256 = 256 LUTs
640 = 640 LUTs
1200 = 1280 LUTs
2000 = 2112 LUTs
4000 = 4320 LUTs
7000 = 6864 LUTs

I/O Count
Blank = Standard Device
U = Ultra High I/O Device

Power/Performance
Z = Low Power
H = High Performance

Supply Voltage
C = 2.5 V / 3.3 V
E = 1.2 V

Speed
1 = Slowest
2
3 = Fastest
} Low Power

4 = Slowest
5
6 = Fastest
} High Performance

Device Status
Blank = Production Device
ES = Engineering Sample
R1 = Production Release 1 Device
1K = WLCSP Package, 1,000 parts per reel

Shipping Method
Blank = Trays
TR = Tape and Reel

Grade
C = Commercial
I = Industrial

Package
UWG25 = 25-Ball Halogen-Free WLCSP (0.4 mm Pitch)
SG32 = 32-Pin Halogen-Free QFN (0.5 mm Pitch)
SG48 = 48-Pin Halogen-Free QFN (0.5 mm Pitch)
UWG49 = 49-ball Halogen-Free WLCSP (0.4 mm Pitch)
UMG64 = 64-Ball Halogen-Free ucBGA (0.4 mm Pitch)
QN84 = 84-Pin Halogen-Free QFN (0.5 mm Pitch)
TG100 = 100-Pin Halogen-Free TQFP
TG144 = 144-Pin Halogen-Free TQFP
MG132 = 132-Ball Halogen-Free csBGA (0.5 mm Pitch)
MG184 = 184-Ball Halogen-Free csBGA (0.5 mm Pitch)
BG256 = 256-Ball Halogen-Free caBGA (0.8 mm Pitch)
FTG256 = 256-Ball Halogen-Free ftBGA (1.0 mm Pitch)
BG332 = 332-Ball Halogen-Free caBGA (0.8 mm Pitch)
FG484 = 484-Ball Halogen-Free fpBGA (1.0 mm Pitch)

* 48-pin QFN information is 'Advanced'.

Ordering Information

MachXO2 devices have top-side markings, for commercial and industrial grades, as shown below:

Notes:

1. Markings are abbreviated for small packages.

2. See PCN 05A-12 for information regarding a change to the top-side mark logo.

Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32C	256	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-256ZE-2SG32C	256	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-256ZE-3SG32C	256	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-256ZE-1UMG64C	256	1.2 V	–1	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-2UMG64C	256	1.2 V	–2	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-3UMG64C	256	1.2 V	–3	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-1TG100C	256	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-2TG100C	256	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-3TG100C	256	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-1MG132C	256	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-2MG132C	256	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-3MG132C	256	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100C	640	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-2TG100C	640	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-3TG100C	640	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-1MG132C	640	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-2MG132C	640	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-3MG132C	640	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1SG32C	1280	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-2SG32C	1280	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-3SG32C	1280	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-1TG100C	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100C	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100C	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132C	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132C	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132C	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144C	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144C	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144C	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1TG100C	2112	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-2TG100C	2112	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-3TG100C	2112	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-1MG132C	2112	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-2MG132C	2112	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-3MG132C	2112	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-1TG144C	2112	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-2TG144C	2112	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-3TG144C	2112	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-1BG256C	2112	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-2BG256C	2112	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-3BG256C	2112	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-1FTG256C	2112	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-2000ZE-2FTG256C	2112	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-2000ZE-3FTG256C	2112	1.2 V	–3	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000ZE-1QN84C	4320	1.2 V	–1	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-2QN84C	4320	1.2 V	–2	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-3QN84C	4320	1.2 V	–3	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-1MG132C	4320	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-2MG132C	4320	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-3MG132C	4320	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-1TG144C	4320	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-2TG144C	4320	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-3TG144C	4320	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-1BG256C	4320	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-2BG256C	4320	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-3BG256C	4320	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-1FTG256C	4320	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-2FTG256C	4320	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-3FTG256C	4320	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-1BG332C	4320	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-2BG332C	4320	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-3BG332C	4320	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-1FG484C	4320	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-4000ZE-2FG484C	4320	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-4000ZE-3FG484C	4320	1.2 V	–3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144C	6864	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-2TG144C	6864	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-3TG144C	6864	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-1BG256C	6864	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-2BG256C	6864	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-3BG256C	6864	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-1FTG256C	6864	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-2FTG256C	6864	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-3FTG256C	6864	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-1BG332C	6864	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-2BG332C	6864	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-3BG332C	6864	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-1FG484C	6864	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-2FG484C	6864	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-3FG484C	6864	1.2 V	–3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100CR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100CR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100CR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132CR1[1]	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132CR1[1]	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132CR1[1]	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144CR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144CR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144CR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200ZE-speed package CR1” are the same as the “LCMXO2-1200ZE-speed package C” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32C	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	COM
LCMXO2-256HC-5SG32C	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	COM
LCMXO2-256HC-6SG32C	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	COM
LCMXO2-256HC-4SG48C	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	COM
LCMXO2-256HC-5SG48C	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	COM
LCMXO2-256HC-6SG48C	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	COM
LCMXO2-256HC-4UMG64C	256	2.5 V / 3.3 V	–4	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-5UMG64C	256	2.5 V / 3.3 V	–5	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-6UMG64C	256	2.5 V / 3.3 V	–6	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-4TG100C	256	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-256HC-5TG100C	256	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-256HC-6TG100C	256	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-256HC-4MG132C	256	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-256HC-5MG132C	256	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-256HC-6MG132C	256	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48C	640	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	COM
LCMXO2-640HC-5SG48C	640	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	COM
LCMXO2-640HC-6SG48C	640	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	COM
LCMXO2-640HC-4TG100C	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-640HC-5TG100C	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-640HC-6TG100C	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-640HC-4MG132C	640	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-640HC-5MG132C	640	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-640HC-6MG132C	640	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144C	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-5TG144C	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-6TG144C	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32C	1280	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	COM
LCMXO2-1200HC-5SG32C	1280	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	COM
LCMXO2-1200HC-6SG32C	1280	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	COM
LCMXO2-1200HC-4TG100C	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100C	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100C	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132C	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132C	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132C	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144C	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144C	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144C	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256C	1280	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-1200UHC-5FTG256C	1280	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-1200UHC-6FTG256C	1280	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100C	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-5TG100C	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-6TG100C	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-4MG132C	2112	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-5MG132C	2112	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-6MG132C	2112	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-4TG144C	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-5TG144C	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-6TG144C	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-4BG256C	2112	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-5BG256C	2112	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-6BG256C	2112	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-4FTG256C	2112	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HC-5FTG256C	2112	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HC-6FTG256C	2112	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484C	2112	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-5FG484C	2112	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-6FG484C	2112	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84C	4320	2.5 V / 3.3 V	–4	Halogen-Free QFN	84	COM
LCMXO2-4000HC-5QN84C	4320	2.5 V / 3.3 V	–5	Halogen-Free QFN	84	COM
LCMXO2-4000HC-6QN84C	4320	2.5 V / 3.3 V	–6	Halogen-Free QFN	84	COM
LCMXO2-4000HC-4MG132C	4320	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-5MG132C	4320	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-6MG132C	4320	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-4TG144C	4320	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-5TG144C	4320	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-6TG144C	4320	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-4BG256C	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-5BG256C	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-6BG256C	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-4FTG256C	4320	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-5FTG256C	4320	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-6FTG256C	4320	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-4BG332C	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-5BG332C	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-6BG332C	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-4FG484C	4320	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-5FG484C	4320	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-6FG484C	4320	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144C	6864	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-5TG144C	6864	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-6TG144C	6864	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-4BG256C	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-5BG256C	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-6BG256C	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-4FTG256C	6864	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-5FTG256C	6864	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-6FTG256C	6864	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-4BG332C	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-5BG332C	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-6BG332C	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-4FG400C	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-5FG400C	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-6FG400C	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-4FG484C	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-5FG484C	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-6FG484C	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100CR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100CR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100CR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132CR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132CR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132CR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144CR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144CR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144CR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200HC-speed package CR1” are the same as the “LCMXO2-1200HC-speed package C” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100C	2112	1.2 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-5TG100C	2112	1.2 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-6TG100C	2112	1.2 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-4TG144C	2112	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-5TG144C	2112	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-6TG144C	2112	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-4MG132C	2112	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-5MG132C	2112	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-6MG132C	2112	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-4BG256C	2112	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-5BG256C	2112	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-6BG256C	2112	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-4FTG256C	2112	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-5FTG256C	2112	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-6FTG256C	2112	1.2 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484C	2112	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-5FG484C	2112	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-6FG484C	2112	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4TG144C	4320	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-5TG144C	4320	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-6TG144C	4320	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-4MG132C	4320	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-5MG132C	4320	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-6MG132C	4320	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-4BG256C	4320	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4MG184C	4320	1.2 V	–4	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5MG184C	4320	1.2 V	–5	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-6MG184C	4320	1.2 V	–6	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5BG256C	4320	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-6BG256C	4320	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4FTG256C	4320	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-5FTG256C	4320	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-6FTG256C	4320	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-4BG332C	4320	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-5BG332C	4320	1.2 V	–5	Halogen-Free caBGA	332	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-6BG332C	4320	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-4FG484C	4320	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-5FG484C	4320	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-6FG484C	4320	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144C	6864	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-5TG144C	6864	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-6TG144C	6864	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-4BG256C	6864	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-5BG256C	6864	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-6BG256C	6864	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-4FTG256C	6864	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-5FTG256C	6864	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-6FTG256C	6864	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-4BG332C	6864	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-5BG332C	6864	1.2 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-6BG332C	6864	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-4FG484C	6864	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-5FG484C	6864	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-6FG484C	6864	1.2 V	–6	Halogen-Free fpBGA	484	COM

Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32I	256	1.2 V	–1	Halogen-Free QFN	32	IND
LCMXO2-256ZE-2SG32I	256	1.2 V	–2	Halogen-Free QFN	32	IND
LCMXO2-256ZE-3SG32I	256	1.2 V	–3	Halogen-Free QFN	32	IND
LCMXO2-256ZE-1UMG64I	256	1.2 V	–1	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-2UMG64I	256	1.2 V	–2	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-3UMG64I	256	1.2 V	–3	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-1TG100I	256	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-2TG100I	256	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-3TG100I	256	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-1MG132I	256	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-2MG132I	256	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-3MG132I	256	1.2 V	–3	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100I	640	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-2TG100I	640	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-3TG100I	640	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-1MG132I	640	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-2MG132I	640	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-3MG132I	640	1.2 V	–3	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1UWG25ITR[1]	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR50[3]	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR1K[2]	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1SG32I	1280	1.2 V	–1	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-2SG32I	1280	1.2 V	–2	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-3SG32I	1280	1.2 V	–3	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-1TG100I	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100I	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100I	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132I	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132I	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132I	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144I	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144I	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144I	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1UWG49ITR[1]	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR50[3]	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR1K[2]	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1TG100I	2112	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-2TG100I	2112	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-3TG100I	2112	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-1MG132I	2112	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-2MG132I	2112	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-3MG132I	2112	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-1TG144I	2112	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-2TG144I	2112	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-3TG144I	2112	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-1BG256I	2112	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-2BG256I	2112	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-3BG256I	2112	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-1FTG256I	2112	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-2FTG256I	2112	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-3FTG256I	2112	1.2 V	–3	Halogen-Free ftBGA	256	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000ZE-1QN84I	4320	1.2 V	–1	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-2QN84I	4320	1.2 V	–2	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-3QN84I	4320	1.2 V	–3	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-1MG132I	4320	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-2MG132I	4320	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-3MG132I	4320	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-1TG144I	4320	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-2TG144I	4320	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-3TG144I	4320	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-1BG256I	4320	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-2BG256I	4320	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-3BG256I	4320	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-1FTG256I	4320	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-2FTG256I	4320	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-3FTG256I	4320	1.2 V	–3	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-1BG332I	4320	1.2 V	–1	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-2BG332I	4320	1.2 V	–2	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-3BG332I	4320	1.2 V	–3	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-1FG484I	4320	1.2 V	–1	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-2FG484I	4320	1.2 V	–2	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-3FG484I	4320	1.2 V	–3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144I	6864	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-2TG144I	6864	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-3TG144I	6864	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-1BG256I	6864	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-2BG256I	6864	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-3BG256I	6864	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-1FTG256I	6864	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-2FTG256I	6864	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-3FTG256I	6864	1.2 V	–3	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-1BG332I	6864	1.2 V	–1	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-2BG332I	6864	1.2 V	–2	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-3BG332I	6864	1.2 V	–3	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-1FG484I	6864	1.2 V	–1	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-2FG484I	6864	1.2 V	–2	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-3FG484I	6864	1.2 V	–3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100IR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100IR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100IR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132IR1[1]	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132IR1[1]	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132IR1[1]	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144IR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144IR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144IR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200ZE-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32I	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	IND
LCMXO2-256HC-5SG32I	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	IND
LCMXO2-256HC-6SG32I	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	IND
LCMXO2-256HC-4SG48I	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	IND
LCMXO2-256HC-5SG48I	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	IND
LCMXO2-256HC-6SG48I	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	IND
LCMXO2-256HC-4UMG64I	256	2.5 V / 3.3 V	–4	Halogen-Free ucBGA	64	IND
LCMXO2-256HC-5UMG64I	256	2.5 V / 3.3 V	–5	Halogen-Free ucBGA	64	IND
LCMXO2-256HC-6UMG64I	256	2.5 V / 3.3 V	–6	Halogen-Free ucBGA	64	IND
LCMXO2-256HC-4TG100I	256	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-256HC-5TG100I	256	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-256HC-6TG100I	256	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-256HC-4MG132I	256	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-256HC-5MG132I	256	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-256HC-6MG132I	256	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48I	640	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	IND
LCMXO2-640HC-5SG48I	640	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	IND
LCMXO2-640HC-6SG48I	640	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	IND
LCMXO2-640HC-4TG100I	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-640HC-5TG100I	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-640HC-6TG100I	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-640HC-4MG132I	640	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-640HC-5MG132I	640	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-640HC-6MG132I	640	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144I	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-640UHC-5TG144I	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-640UHC-6TG144I	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32I	1280	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	IND
LCMXO2-1200HC-5SG32I	1280	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	IND
LCMXO2-1200HC-6SG32I	1280	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	IND
LCMXO2-1200HC-4TG100I	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100I	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100I	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132I	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132I	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132I	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144I	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144I	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144I	1280	2.5 V/ 3.3 V	–6	Halogen-Free TQFP	144	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256I	1280	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-5FTG256I	1280	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-6FTG256I	1280	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100I	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-5TG100I	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-6TG100I	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-4MG132I	2112	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-5MG132I	2112	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-6MG132I	2112	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-4TG144I	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-5TG144I	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-6TG144I	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-4BG256I	2112	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-5BG256I	2112	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-6BG256I	2112	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-4FTG256I	2112	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-5FTG256I	2112	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-6FTG256I	2112	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484I	2112	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-5FG484I	2112	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-6FG484I	2112	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84I	4320	2.5 V / 3.3 V	–4	Halogen-Free QFN	84	IND
LCMXO2-4000HC-5QN84I	4320	2.5 V / 3.3 V	–5	Halogen-Free QFN	84	IND
LCMXO2-4000HC-6QN84I	4320	2.5 V / 3.3 V	–6	Halogen-Free QFN	84	IND
LCMXO2-4000HC-4TG144I	4320	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-5TG144I	4320	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-6TG144I	4320	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-4MG132I	4320	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-5MG132I	4320	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-6MG132I	4320	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-4BG256I	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-5BG256I	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-6BG256I	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-4FTG256I	4320	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-5FTG256I	4320	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-6FTG256I	4320	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-4BG332I	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-5BG332I	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-6BG332I	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-4FG484I	4320	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-5FG484I	4320	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-6FG484I	4320	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144I	6864	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-5TG144I	6864	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-6TG144I	6864	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-4BG256I	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-5BG256I	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-6BG256I	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-4FTG256I	6864	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-5FTG256I	6864	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-6FTG256I	6864	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-4BG332I	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-5BG332I	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-6BG332I	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-4FG400I	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-5FG400I	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-6FG400I	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-4FG484I	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-5FG484I	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-6FG484I	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100IR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100IR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100IR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132IR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132IR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132IR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144IR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144IR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144IR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200HC-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High Performance Industrial Grade Devices Without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100I	2112	1.2 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-5TG100I	2112	1.2 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-6TG100I	2112	1.2 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-4MG132I	2112	1.2 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-5MG132I	2112	1.2 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-6MG132I	2112	1.2 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-4TG144I	2112	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-5TG144I	2112	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-6TG144I	2112	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-4BG256I	2112	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-5BG256I	2112	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-6BG256I	2112	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-4FTG256I	2112	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-5FTG256I	2112	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-6FTG256I	2112	1.2 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484I	2112	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-5FG484I	2112	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-6FG484I	2112	1.2 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4MG132I	4320	1.2 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-5MG132I	4320	1.2 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-6MG132I	4320	1.2 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-4TG144I	4320	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-5TG144I	4320	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-6TG144I	4320	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-4MG184I	4320	1.2 V	–4	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-5MG184I	4320	1.2 V	–5	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-6MG184I	4320	1.2 V	–6	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-4BG256I	4320	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-5BG256I	4320	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-6BG256I	4320	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-4FTG256I	4320	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-5FTG256I	4320	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-6FTG256I	4320	1.2 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-4BG332I	4320	1.2 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-5BG332I	4320	1.2 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-6BG332I	4320	1.2 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-4FG484I	4320	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-5FG484I	4320	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-6FG484I	4320	1.2 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144I	6864	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-5TG144I	6864	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-6TG144I	6864	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-4BG256I	6864	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-5BG256I	6864	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-6BG256I	6864	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-4FTG256I	6864	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-5FTG256I	6864	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-6FTG256I	6864	1.2 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-4BG332I	6864	1.2 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-5BG332I	6864	1.2 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-6BG332I	6864	1.2 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-4FG484I	6864	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-5FG484I	6864	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-6FG484I	6864	1.2 V	–6	Halogen-Free fpBGA	484	IND

R1 Device Specifications

The LCMXO2-1200ZE/HC "R1" devices have the same specifications as their Standard (non-R1) counterparts except as listed below. For more details on the R1 to Standard migration refer to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard Non-R1) Devices.

- The User Flash Memory (UFM) cannot be programmed through the internal WISHBONE interface. It can still be programmed through the JTAG/SPI/I^{2}C ports.
- The on-chip differential input termination resistor value is higher than intended. It is approximately 200Ω as opposed to the intended 100Ω. It is recommended to use external termination resistors for differential inputs. The on-chip termination resistors can be disabled through Lattice design software.
- Soft Error Detection logic may not produce the correct result when it is run for the first time after configuration. To use this feature, discard the result from the first operation. Subsequent operations will produce the correct result.
- Under certain conditions, IIH exceeds data sheet specifications. The following table provides more details:

Condition	Clamp	Pad Rising IIH Max.	Pad Falling IIH Min.	Steady State Pad High IIH	Steady State Pad Low IIL
VPAD > VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD = VCCIO	ON	10 µA	–10 µA	10 µA	10 µA
VPAD = VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD < VCCIO	OFF	10 µA	–10 µA	10 µA	10 µA

- The user SPI interface does not operate correctly in some situations. During master read access and slave write access, the last byte received does not generate the RRDY interrupt.
- In GDDRX2, GDDRX4 and GDDR71 modes, ECLKSYNC may have a glitch in the output under certain conditions, leading to possible loss of synchronization.
- When using the hard I^{2}C IP core, the I^{2}C status registers I2C_1_SR and I2C_2_SR may not update correctly.
- PLL Lock signal will glitch high when coming out of standby. This glitch lasts for about 10 µsec before returning low.
- Dual boot only available on HC devices, requires tying VCC and VCCIO2 to the same 3.3 V or 2.5 V supply.

MachXO2 Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the MachXO2 family are available on the Lattice web site.

- TN1198, Power Estimation and Management for MachXO2 Devices
- TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide
- TN1201, Memory Usage Guide for MachXO2 Devices
- TN1202, MachXO2 sysIO Usage Guide
- TN1203, Implementing High-Speed Interfaces with MachXO2 Devices
- TN1204, MachXO2 Programming and Configuration Usage Guide
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices
- TN1206, MachXO2 SRAM CRC Error Detection Usage Guide
- TN1207, Using TraceID in MachXO2 Devices
- TN1074, PCB Layout Recommendations for BGA Packages
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices
- AN8066, Boundary Scan Testability with Lattice sysIO Capability
- MachXO2 Device Pinout Files
- Thermal Management document
- Lattice design tools

For further information on interface standards, refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, LVDS, DDR, DDR2, LPDDR): www.jedec.org
- PCI: www.pcisig.com

MachXO2 Family Data Sheet Revision History

March 2017 **Data Sheet DS1035**

Date	Version	Section	Change Summary
March 2017	3.3	DC and Switching Characteristics	Updated the Absolute Maximum Ratings section. Added standards.
			Updated the sysIO Recommended Operating Conditions section. Added standards.
			Updated the sysIO Single-Ended DC Electrical Characteristics section. Added standards.
			Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA}. The parameter descriptions were also modified.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA}. The parameter descriptions were also modified.
			Updated the sysCONFIG Port Timing Specifications section. Corrected the t_{INITL} units from ns to µs.
		Pinout Information	Updated the Signal Descriptions section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals.
			Updated the Pinout Information Summary section. Added footnote to MachXO2-1200 32 QFN.
		Ordering Information	Updated the MachXO2 Part Number Description section. Corrected the MG184, BG256, FTG256 package information. Added “(0.8 mm Pitch)” to BG332.
			Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. — Updated LCMXO2-1200ZE-1UWG25ITR50 footnote. — Corrected footnote numbering typo. — Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2-2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s.

Date	Version	Section	Change Summary
May 2016	3.2	All	Moved designation for 84 QFN package information from 'Advanced' to 'Final'.
		Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added ‘Advanced’ 48 QFN package. — Revised footnote 6. — Added footnote 9.
		DC and Switching Characteristics	Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Added footnote 12.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Added footnote 12.
		Pinout Information	Updated the Signal Descriptions section. Added information on GND signal.
			Updated the Pinout Information Summary section. — Added ‘Advanced’ MachXO2-256 48 QFN values. — Added ‘Advanced’ MachXO2-640 48 QFN values. — Added footnote to GND. — Added footnotes 2 and 3.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added ‘Advanced’ SG48 package and revised footnote.
			Updated the Ordering Information section. — Added part numbers for ‘Advanced’ QFN 48 package.
March 2016	3.1	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 32 QFN value for XO2-1200. — Added 84 QFN (7 mm x 7 mm, 0.5 mm) package. — Modified package name to 100-pin TQFP. — Modified package name to 144-pin TQFP. — Added footnote.
		Architecture	Updated the Typical I/O Behavior During Power-up section. Removed reference to TN1202.
		DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications section. Revised $t_{DPPDONE}$ and $t_{DPPINIT}$ Max. values per PCN 03A-16, released March 2016.
		Pinout Information	Updated the Pinout Information Summary section. — Added MachXO2-1200 32 QFN values. — Added ‘Advanced’ MachXO2-4000 84 QFN values.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added ‘Advanced’ QN84 package and footnote.
			Updated the Ordering Information section. — Added part numbers for 1280 LUTs QFN 32 package. — Added part numbers for 4320 LUTs QFN 84 package.
March 2015	3.0	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Changed 64-ball ucBGA dimension.
		Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.

Date	Version	Section	Change Summary
December 2014	2.9	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Removed XO2-4000U data. — Removed 400-ball ftBGA. — Removed 25-ball WLCSP value for XO2-2000U.
		DC and Switching Characteristics	Updated the Recommended Operating Conditions section. Adjusted Max. values for V_{CC} and V_{CCIO}.
			Updated the sysIO Recommended Operating Conditions section. Adjusted Max. values for LVCMOS 3.3, LVTTL, PCI, LVDS33 and LVPECL.
		Pinout Information	Updated the Pinout Information Summary section. Removed MachXO2-4000U.
		Ordering Information	Updated the MachXO2 Part Number Description section. Removed BG400 package.
			Updated the High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
			Updated the High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
November 2014	2.8	Introduction	Updated the Features section. — Revised I/Os under Flexible Logic Architecture. — Revised standby power under Ultra Low Power Devices. — Revise input frequency range under Flexible On-Chip Clocking.
			Updated Table 1-1, MachXO2 Family Selection Guide. — Added XO2-4000U data. — Removed HE and ZE device options for XO2-4000. — Added 400-ball ftBGA.
		Pinout Information	Updated the Pinout Information Summary section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added BG400 package.
			Updated the Ordering Information section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400 part numbers.
October 2014	2.7	Ordering Information	Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Fixed typo in LCMXO2-2000ZE-1UWG49ITR part number package.
		Architecture	Updated the Supported Standards section. Added MIPI information to Table 2-12. Supported Input Standards and Table 2-13. Supported Output Standards.
		DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition.
			Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition.
			Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.
July 2014	2.6	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics[1, 2] section. Updated footnote 4.
			Updated Register-to-Register Performance section. Updated footnote.
		Ordering Information	Updated UW49 package to UWG49 in MachXO2 Part Number Description.
			Updated LCMXO2-2000ZE-1UWG49CTR package in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging.

Date	Version	Section	Change Summary
May 2014	2.5	Architecture	Updated TransFR (Transparent Field Reconfiguration) section. Updated TransFR description for PLL use during background Flash programming.
February 2014	02.4	Introduction	Included the 49 WLCSP package in the MachXO2 Family Selection Guide table.
		Architecture	Added information to Standby Mode and Power Saving Options section.
		Pinout Information	Added the XO2-2000 49 WLCSP in the Pinout Information Summary table.
		Ordering Information	Added UW49 package in MachXO2 Part Number Description.
			Added and LCMXO2-2000ZE-1UWG49CTR in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging section.
			Added and LCMXO2-2000ZE-1UWG49ITR in Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section.
December 2013	02.3	Architecture	Updated information on CLKOS output divider in sysCLOCK Phase Locked Loops (PLLs) section.
		DC and Switching Characteristics	Updated Static Supply Current – ZE Devices table.
			Updated footnote 4 in sysIO Single-Ended DC Electrical Characteristics table; Updated V_{IL} Max. (V) data for LVCMOS 25 and LVCMOS 28.
			Updated V_{OS} test condition in sysIO Differential Electrical Characteristics - LVDS table.
September 2013	02.2	Architecture	Removed I^2C Clock-Stretching feature per PCN #10A-13.
			Removed information on PDPR memory in RAM Mode section.
			Updated Supported Input Standards table.
		DC and Switching Characteristics	Updated Power-On-Reset Voltage Levels table.
June 2013	02.1	Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.
			sysCLOCK Phase Locked Loops (PLLs) section – Added missing cross reference to sysCLOCK PLL Timing table.
		DC and Switching Characteristics	Added slew rate information to footnote 2 of the MachXO2 External Switching Characteristics – HC/HE Devices and the MachXO2 External Switching Characteristics – ZE Devices tables.
			Power-On-Reset Voltage Levels table – Added symbols.

Date	Version	Section	Change Summary
January 2013	02.0	Introduction	Updated the total number IOs to include JTAGENB.
		Architecture	Supported Output Standards table – Added 3.3 V_{CCIO} (Typ.) to LVDS row.
			Changed SRAM CRC Error Detection to Soft Error Detection.
		DC and Switching Characteristics	Power Supply Ramp Rates table – Updated Units column for t_{RAMP} symbol.
			Added new Maximum sysIO Buffer Performance table.
			sysCLOCK PLL Timing table – Updated Min. column values for f_{IN}, f_{OUT}, f_{OUT2} and f_{PFD} parameters. Added t_{SPO} parameter. Updated footnote 6.
			MachXO2 Oscillator Output Frequency table – Updated symbol name for $t_{STABLEOSC.}$
			DC Electrical Characteristics table – Updated conditions for $I_{IL,}$ I_{IH} symbols.
			Corrected parameters tDQVBS and tDQVAS
			Corrected MachXO2 ZE parameters tDVADQ and tDVEDQ
		Pinout Information	Included the MachXO2-4000HE 184 csBGA package.
		Ordering Information	Updated part number.
April 2012	01.9	Architecture	Removed references to TN1200.
		Ordering Information	Updated the Device Status portion of the MachXO2 Part Number Description to include the 50 parts per reel for the WLCSP package.
			Added new part number and footnote 2 for LCMXO2-1200ZE-1UWG25ITR50.
			Updated footnote 1 for LCMXO2-1200ZE-1UWG25ITR.
		Supplemental Information	Removed references to TN1200.
March 2012	01.8	Introduction	Added 32 QFN packaging information to Features bullets and MachXO2 Family Selection Guide table.
		DC and Switching Characteristics	Changed ‘STANDBY’ to ‘USERSTDBY’ in Standby Mode timing diagram.
		Pinout Information	Removed footnote from Pin Information Summary tables.
			Added 32 QFN package to Pin Information Summary table.
		Ordering Information	Updated Part Number Description and Ordering Information tables for 32 QFN package.
			Updated topside mark diagram in the Ordering Information section.

Date	Version	Section	Change Summary
February 2012	01.7	All	Updated document with new corporate logo.
	01.6	—	Data sheet status changed from preliminary to final.
		Introduction	MachXO2 Family Selection Guide table – Removed references to 49-ball WLCSP.
		DC and Switching Characteristics	Updated Flash Download Time table.
			Modified Storage Temperature in the Absolute Maximum Ratings section.
			Updated I_{DK} max in Hot Socket Specifications table.
			Modified Static Supply Current tables for ZE and HC/HE devices.
			Updated Power Supply Ramp Rates table.
			Updated Programming and Erase Supply Current tables.
			Updated data in the External Switching Characteristics table.
			Corrected Absolute Maximum Ratings for Dedicated Input Voltage Applied for LCMXO2 HC.
			DC Electrical Characteristics table – Minor corrections to conditions for I_{IL}, I_{IH}.
		Pinout Information	Removed references to 49-ball WLCSP.
			Signal Descriptions table – Updated description for GND, VCC, and VCCIOx.
			Updated Pin Information Summary table – Number of VCCIOs, GNDs, VCCs, and Total Count of Bonded Pins for MachXO2-256, 640, and 640U and Dual Function I/O for MachXO2-4000 332caBGA.
		Ordering Information	Removed references to 49-ball WLCSP
August 2011	01.5	DC and Switching Characteristics	Updated ESD information.
		Ordering Information	Updated footnote for ordering WLCSP devices.
	01.4	Architecture	Updated information in Clock/Control Distribution Network and sysCLOCK Phase Locked Loops (PLLs).
		DC and Switching Characteristics	Updated I_{IL} and I_{IH} conditions in the DC Electrical Characteristics table.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Updated Pin Information Summary table: Dual Function I/O, DQS Groups Bank 1, Total General Purpose Single-Ended I/O, Differential I/O Per Bank, Total Count of Bonded Pins, Gearboxes. Added column of data for MachXO2-2000 49 WLCSP.
		Ordering Information	Updated R1 Device Specifications text section with information on migration from MachXO2-1200-R1 to Standard (non-R1) devices.
			Corrected Supply Voltage typo for part numbers: LCMX02-2000UHE-4FG484I, LCMX02-2000UHE-5FG484I, LCMX02-2000UHE-6FG484I.
			Added footnote for WLCSP package parts.
		Supplemental Information	Removed reference to Stand-alone Power Calculator for MachXO2 Devices. Added reference to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices.

Date	Version	Section	Change Summary
May 2011	01.3	Multiple	Replaced “SED” with “SRAM CRC Error Detection” throughout the document.
		DC and Switching Characteristics	Added footnote 1 to Program Erase Specifications table.
		Pinout Information	Updated Pin Information Summary tables.
			Signal name SO/SISPISO changed to SO/SPISO in the Signal Descriptions table.
April 2011	01.2	—	Data sheet status changed from Advance to Preliminary.
		Introduction	Updated MachXO2 Family Selection Guide table.
		Architecture	Updated Supported Input Standards table.
			Updated sysMEM Memory Primitives diagram.
			Added differential SSTL and HSTL IO standards.
		DC and Switching Characteristics	Updates following parameters: POR voltage levels, DC electrical characteristics, static supply current for ZE/HE/HC devices, static power consumption contribution of different components – ZE devices, programming and erase Flash supply current.
			Added VREF specifications to sysIO recommended operating conditions.
			Updating timing information based on characterization.
			Added differential SSTL and HSTL IO standards.
		Ordering Information	Added Ordering Part Numbers for R1 devices, and devices in WLCSP packages.
			Added R1 device specifications.
January 2011	01.1	All	Included ultra-high I/O devices.
		DC and Switching Characteristics	Recommended Operating Conditions table – Added footnote 3.
			DC Electrical Characteristics table – Updated data for I_{IL}, I_{IH}. V_{HYST} typical values updated.
			Generic DDRX2 Outputs with Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB}.
			Generic DDRX4 Outputs with Clock and Data Aligned at Pin (GDDRX4_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB}.
			Power-On-Reset Voltage Levels table - clarified note 3.
			Clarified VCCIO related recommended operating conditions specifications.
			Added power supply ramp rate requirements.
			Added Power Supply Ramp Rates table.
			Updated Programming/Erase Specifications table.
			Removed references to V_{CCP}.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Removed references to V_{CCP}.
November 2010	01.0	—	Initial release.

MachXO2™ Family Data Sheet

DS1035 Version 3.3, March 2017

MachXO2 Family Data Sheet Introduction

May 2016 Data Sheet DS1035

Features

- **Flexible Logic Architecture**
  - Six devices with 256 to 6864 LUT4s and 18 to 334 I/Os
- **Ultra Low Power Devices**
  - Advanced 65 nm low power process
  - As low as 22 µW standby power
  - Programmable low swing differential I/Os
  - Stand-by mode and other power saving options
- **Embedded and Distributed Memory**
  - Up to 240 kbits sysMEM™ Embedded Block RAM
  - Up to 54 kbits Distributed RAM
  - Dedicated FIFO control logic
- **On-Chip User Flash Memory**
  - Up to 256 kbits of User Flash Memory
  - 100,000 write cycles
  - Accessible through WISHBONE, SPI, I^2C and JTAG interfaces
  - Can be used as soft processor PROM or as Flash memory
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated gearing logic
  - 7:1 Gearing for Display I/Os
  - Generic DDR, DDRX2, DDRX4
  - Dedicated DDR/DDR2/LPDDR memory with DQS support
- **High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - PCI
    - LVDS, Bus-LVDS, MLVDS, RSDS, LVPECL
    - SSTL 25/18
    - HSTL 18
    - Schmitt trigger inputs, up to 0.5 V hysteresis
  - I/Os support hot socketing
  - On-chip differential termination
  - Programmable pull-up or pull-down mode
- **Flexible On-Chip Clocking**
  - Eight primary clocks
  - Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
  - Up to two analog PLLs per device with fractional-n frequency synthesis
    - Wide input frequency range (7 MHz to 400 MHz)
- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - Single-chip, secure solution
  - Programmable through JTAG, SPI or I^2C
  - Supports background programming of non-volatile memory
  - Optional dual boot with external SPI memory
- **TransFR™ Reconfiguration**
  - In-field logic update while system operates
- **Enhanced System Level Support**
  - On-chip hardened functions: SPI, I^2C, timer/counter
  - On-chip oscillator with 5.5% accuracy
  - Unique TraceID for system tracking
  - One Time Programmable (OTP) mode
  - Single power supply with extended operating range
  - IEEE Standard 1149.1 boundary scan
  - IEEE 1532 compliant in-system programming
- **Broad Range of Package Options**
  - TQFP, WLCSP, ucBGA, csBGA, caBGA, ftBGA, fpBGA, QFN package options
  - Small footprint package options
    - As small as 2.5 mm x 2.5 mm
  - Density migration supported
  - Advanced halogen-free packaging

Table 1-1. MachXO2™ Family Selection Guide

		XO2-256	XO2-640	XO2-640U[1]	XO2-1200	XO2-1200U[1]	XO2-2000	XO2-2000U[1]	XO2-4000	XO2-7000
LUTs		256	640	640	1280	1280	2112	2112	4320	6864
Distributed RAM (kbits)		2	5	5	10	10	16	16	34	54
EBR SRAM (kbits)		0	18	64	64	74	74	92	92	240
Number of EBR SRAM Blocks (9 kbits/block)		0	2	7	7	8	8	10	10	26
UFM (kbits)		0	24	64	64	80	80	96	96	256
Device Options:	HC[2]	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	HE[3]						Yes	Yes	Yes	Yes
	ZE[4]	Yes	Yes		Yes		Yes		Yes	Yes
Number of PLLs		0	0	1	1	1	1	2	2	2
Hardened Functions:	I2C	2	2	2	2	2	2	2	2	2
	SPI	1	1	1	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1	1	1	1
Packages						**IO**				
25-ball WLCSP[5] (2.5 mm x 2.5 mm, 0.4 mm)					18					
32 QFN[6] (5 mm x 5 mm, 0.5 mm)		21			21					
48 QFN[8, 9] (7 mm x 7 mm, 0.5 mm)		40	40							
49-ball WLCSP[5] (3.2 mm x 3.2 mm, 0.4 mm)							38			
64-ball ucBGA (4 mm x 4 mm, 0.4 mm)		44								
84 QFN[7] (7 mm x 7 mm, 0.5 mm)									68	
100-pin TQFP (14 mm x 14 mm)		55	78		79		79			
132-ball csBGA (8 mm x 8 mm, 0.5 mm)		55	79		104		104		104	
144-pin TQFP (20 mm x 20 mm)				107	107		111		114	114
184-ball csBGA[7] (8 mm x 8 mm, 0.5 mm)									150	
256-ball caBGA (14 mm x 14 mm, 0.8 mm)							206		206	206
256-ball ftBGA (17 mm x 17 mm, 1.0 mm)						206	206		206	206
332-ball caBGA (17 mm x 17 mm, 0.8 mm)									274	278
484-ball ftBGA (23 mm x 23 mm, 1.0 mm)								278	278	334

1. Ultra high I/O device.
2. High performance with regulator – VCC = 2.5 V, 3.3 V
3. High performance without regulator – V_{CC} = 1.2 V
4. Low power without regulator – V_{CC} = 1.2 V
5. WLCSP package only available for ZE devices.
6. 32 QFN package only available for HC and ZE devices.
7. 184 csBGA package only available for HE devices.
8. 48-pin QFN information is ‘Advanced’.
9. 48 QFN package only available for HC devices.

Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I^2C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external V_{CC} supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V_{CC} supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I^2C port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

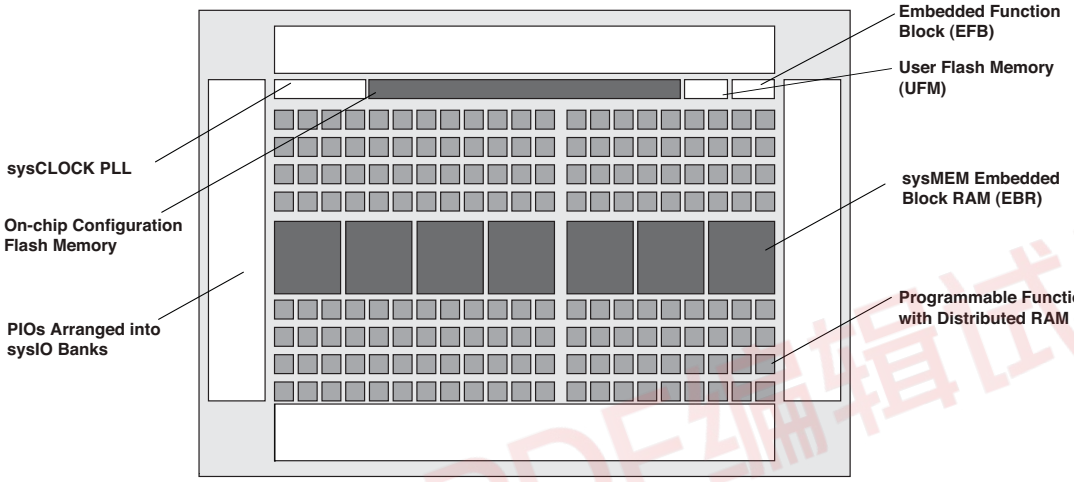
Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

Architecture Overview

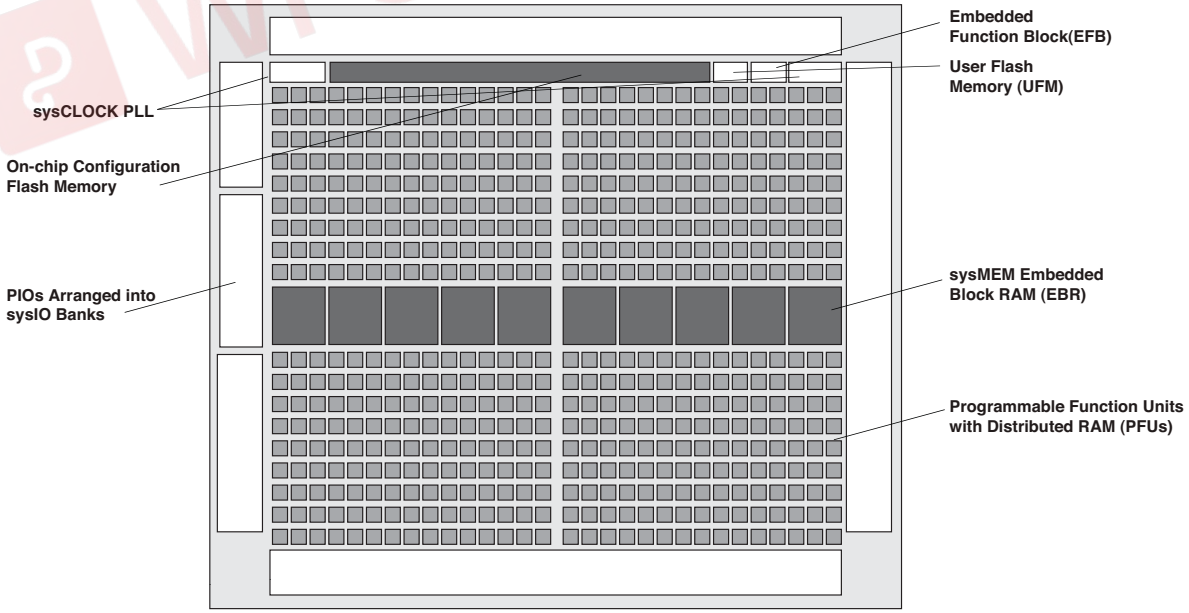
The MachXO2 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.

Figure 2-1. Top View of the MachXO2-1200 Device



Note: MachXO2-256, and MachXO2-640/U are similar to MachXO2-1200. MachXO2-256 has a lower LUT count and no PLL or EBR blocks. MachXO2-640 has no PLL, a lower LUT count and two EBR blocks. MachXO2-640U has a lower LUT count, one PLL and seven EBR blocks.

Figure 2-2. Top View of the MachXO2-4000 Device



Note: MachXO2-1200U, MachXO2-2000/U and MachXO2-7000 are similar to MachXO2-4000. MachXO2-1200U and MachXO2-2000 have a lower LUT count, one PLL, and eight EBR blocks. MachXO2-2000U has a lower LUT count, two PLLs, and 10 EBR blocks. MachXO2-7000 has a higher LUT count, two PLLs, and 26 EBR blocks.

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2-640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

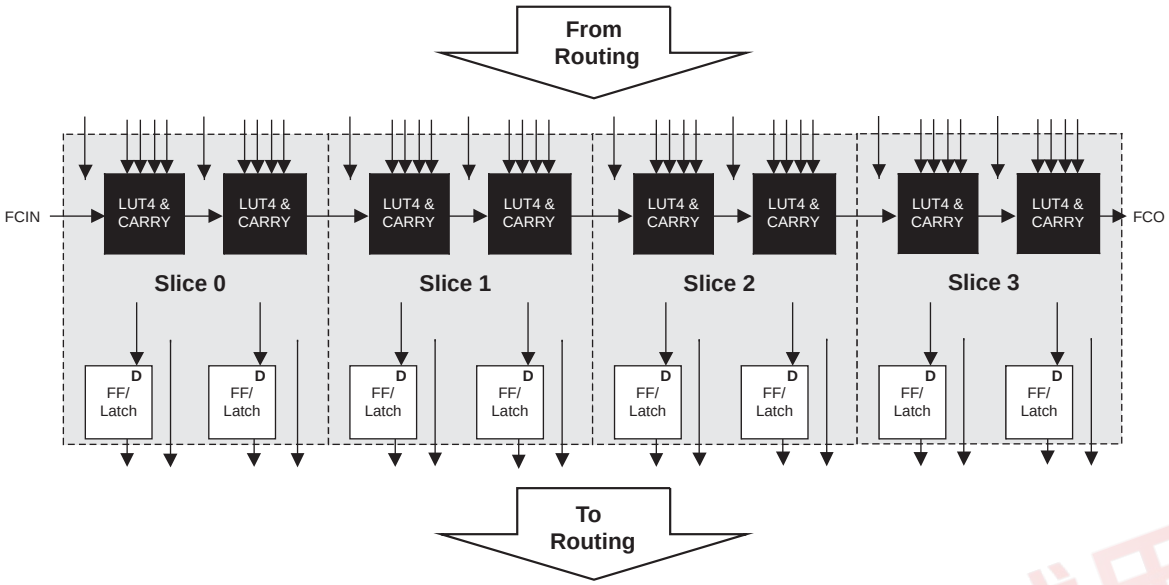
MachXO2 devices provide commonly used hardened functions such as SPI controller, I^2C controller and timer/counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I^2C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

PFU Blocks

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Block Diagram



Slices

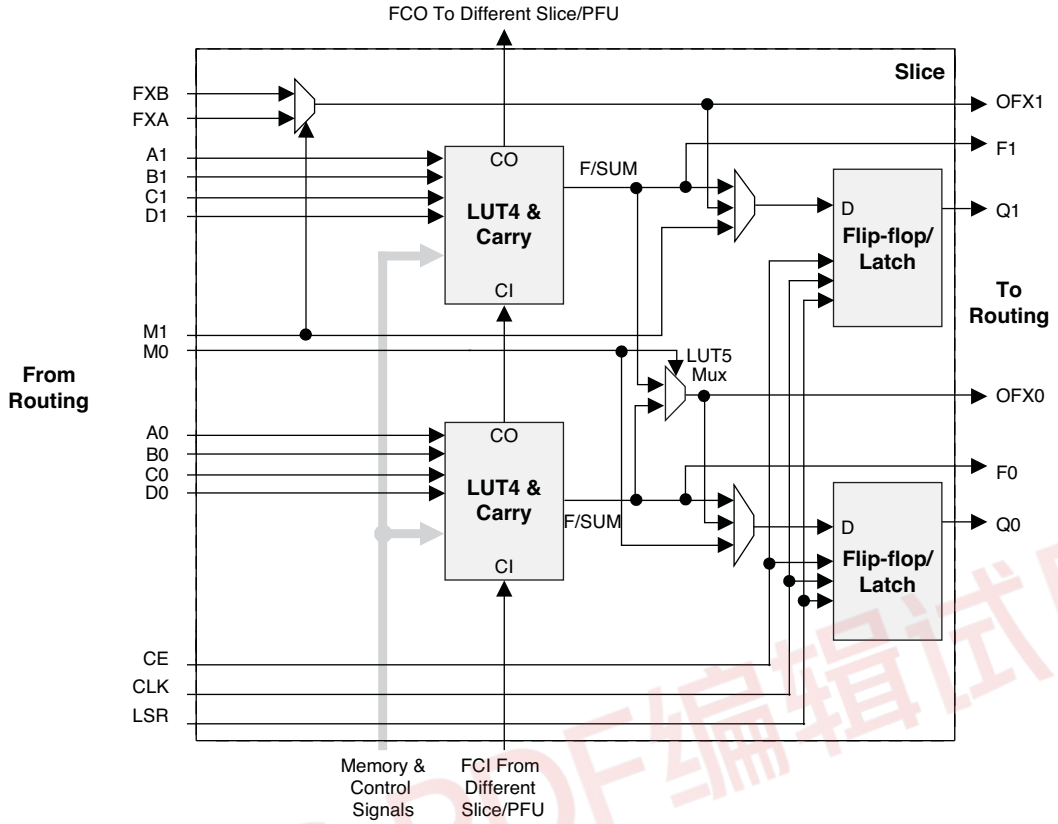
Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU Block	
	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.

Figure 2-4. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multi-purpose input
Input	Control signal	CE	Clock enable
Input	Control signal	LSR	Local set/reset
Input	Control signal	CLK	System clock
Input	Inter-PFU signal	FCIN	Fast carry in[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Fast carry out[1]

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO2 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO2 devices, please see TN1201, Memory Usage Guide for MachXO2 Devices.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

Routing

There are many resources provided in the MachXO2 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Each MachXO2 device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

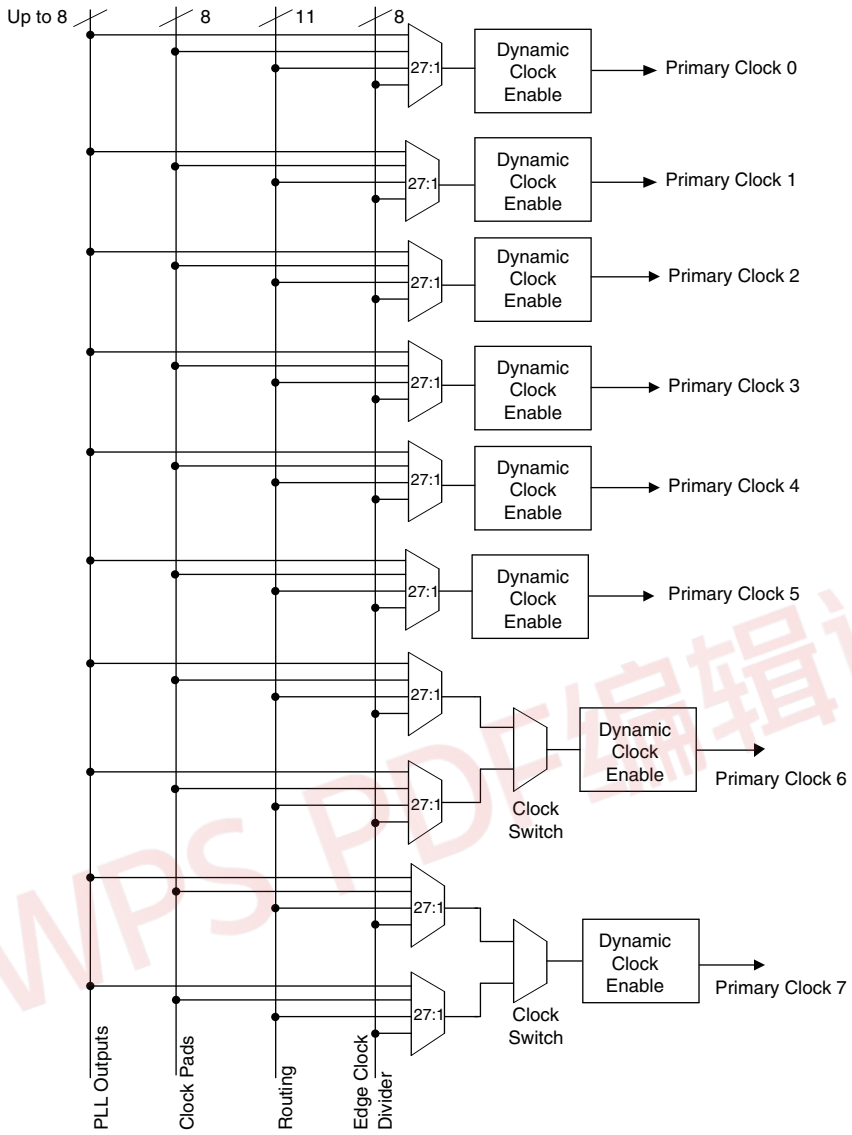
The MachXO2 architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO2-640U, MachXO2-1200/U and higher density devices have two edge clocks each on the top and bottom edges. Lower density devices have no edge clocks. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO2 devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO2 External Switching Characteristics table.

The primary clock signals for the MachXO2-256 and MachXO2-640 are generated from eight 17:1 muxes The available clock sources include eight I/O sources and 9 routing inputs. Primary clock signals for the MachXO2-640U, MachXO2-1200/U and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.

Figure 2-5. Primary Clocks for MachXO2 Devices

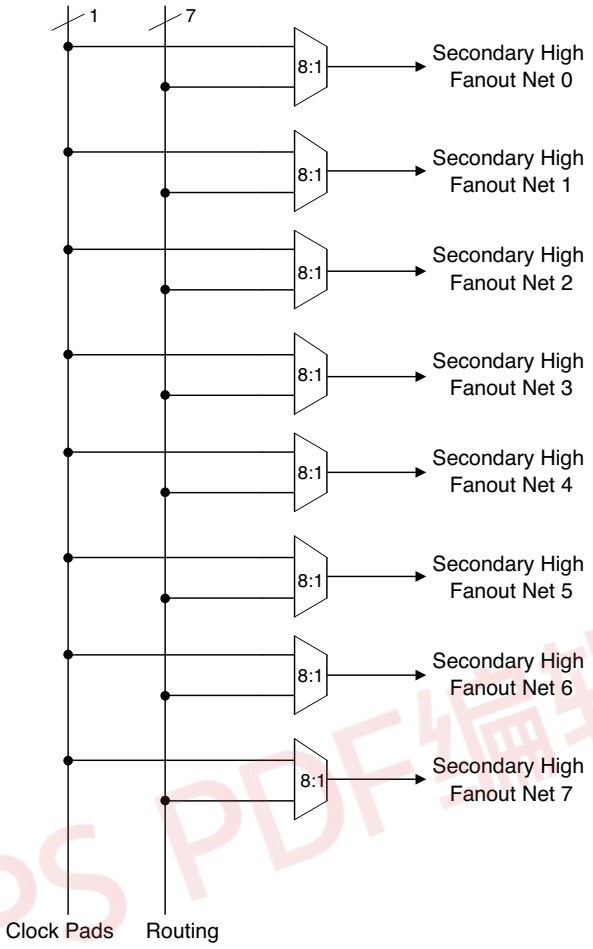


Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO2 External Switching Characteristics table.

Figure 2-6. Secondary High Fanout Nets for MachXO2 Devices



sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The MachXO2-640U, MachXO2-1200/U and larger devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO2 sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO2 clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.

This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the t_{LOCK} parameter has been satisfied.

The MachXO2 also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO2 PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the t_{LOCK} parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

For more details on the PLL and the WISHBONE interface, see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

Figure 2-7. PLL Diagram

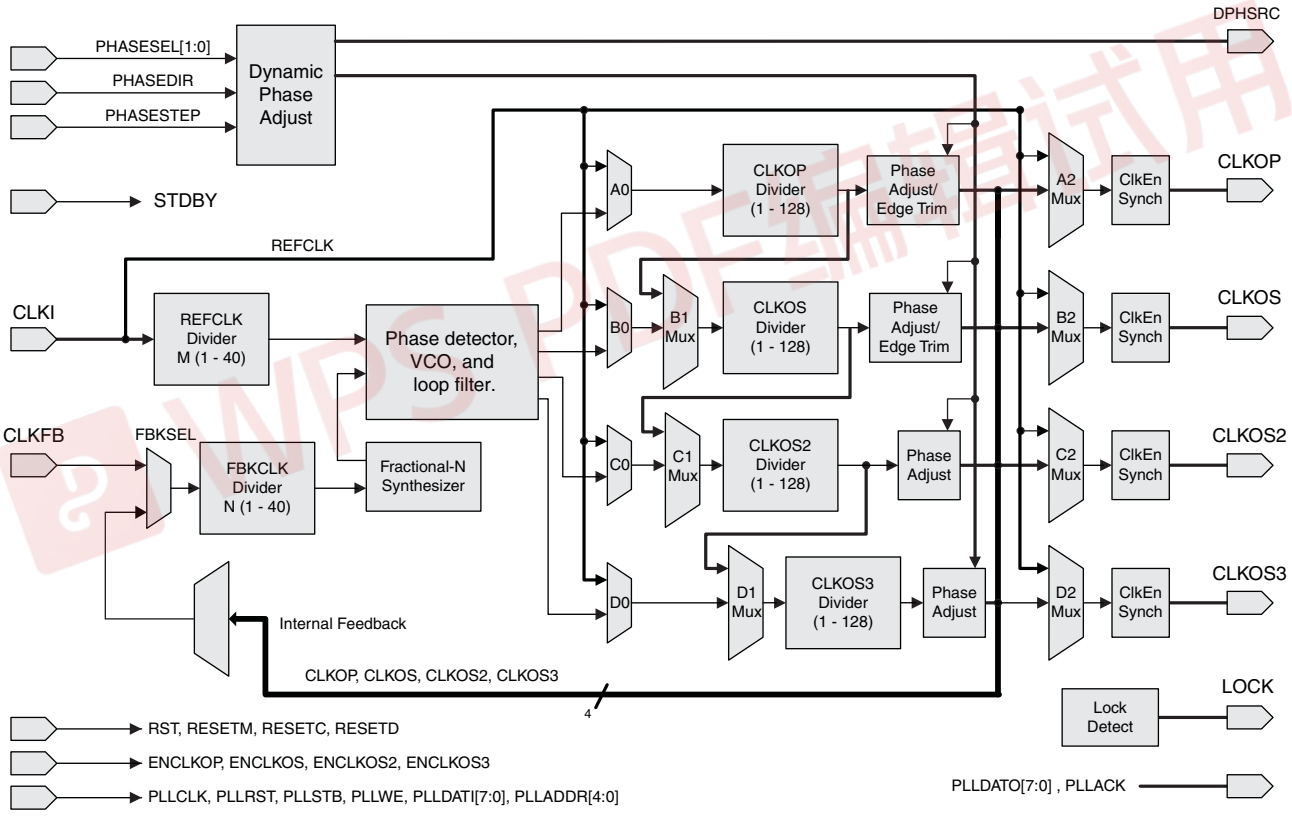


Table 2-4 provides signal descriptions of the PLL block.

Table 2-4. PLL Signal Descriptions

Port Name	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	I	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	I	Dynamic Phase step – toggle shifts VCO phase adjust by one step.

Table 2-4. PLL Signal Descriptions (Continued)

Port Name	I/O	Description
CLKOP	O	Primary PLL output clock (with phase shift adjustment)
CLKOS	O	Secondary PLL output clock (with phase shift adjust)
CLKOS2	O	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	O	Secondary PLL output clock3 (with phase shift adjust)
LOCK	O	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feedback signals.
DPHSRC	O	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset - includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	O	PLL data bus data output
PLLACK	O	PLL data bus acknowledge signal

sysMEM Embedded Block RAM Memory

The MachXO2-640/U and larger devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO2 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

Figure 2-8. sysMEM Memory Primitives

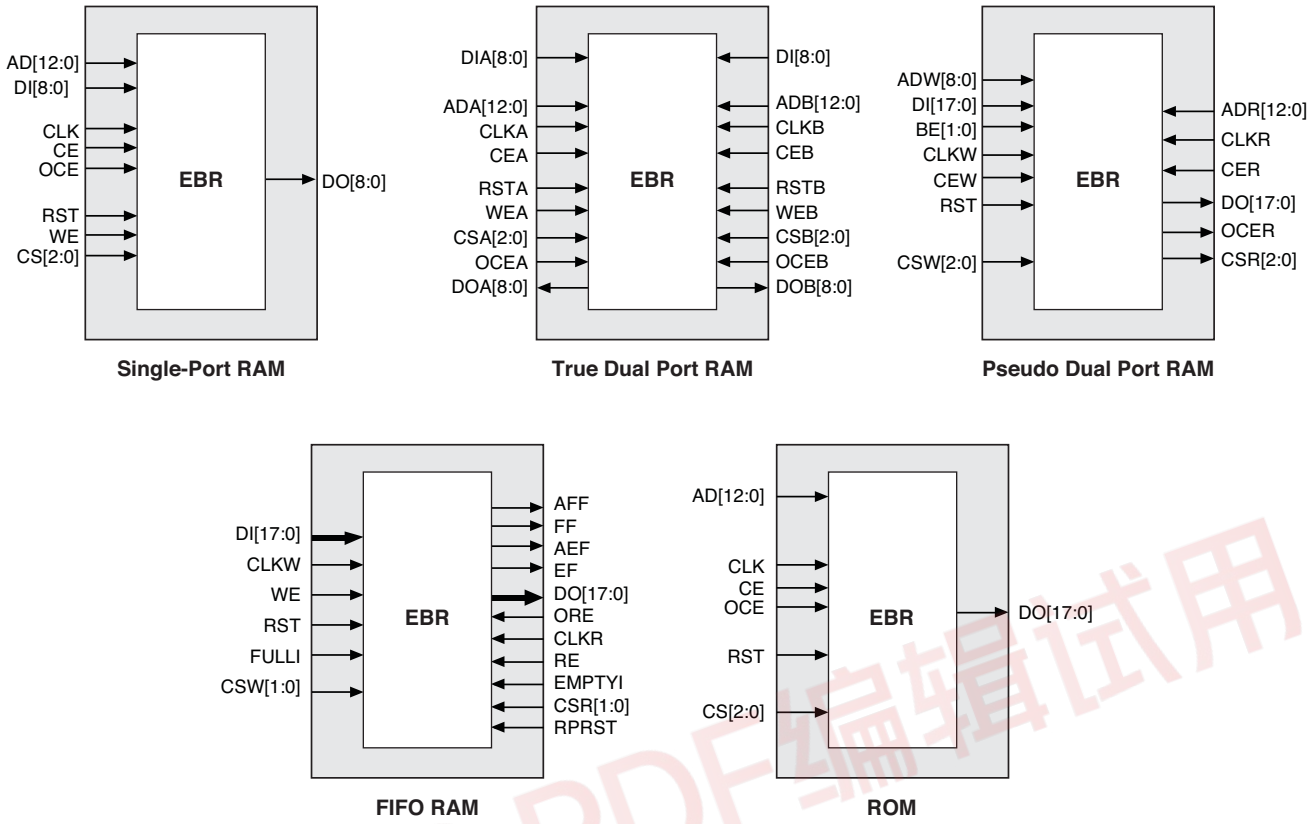


Table 2-6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE[1]	Output Clock Enable	Active High
RST	Reset	Active High
BE[1]	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	—
DI	Data In	—
DO	Data Out	—
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	—
FF	FIFO RAM Full Flag	—
AEF	FIFO RAM Almost Empty Flag	—
EF	FIFO RAM Empty Flag	—
RPRST	FIFO RAM Read Pointer Reset	—

1. Optional signals.
2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.

3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

Table 2-7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

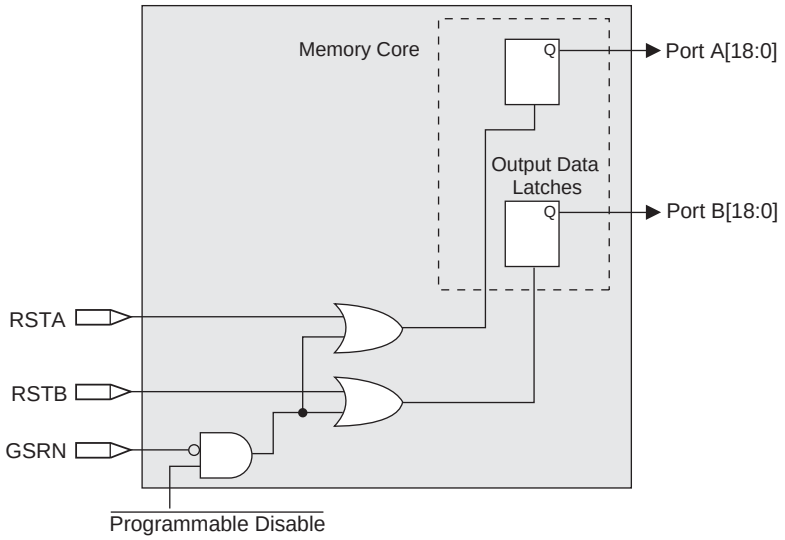
N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

Figure 2-9. Memory Core Reset

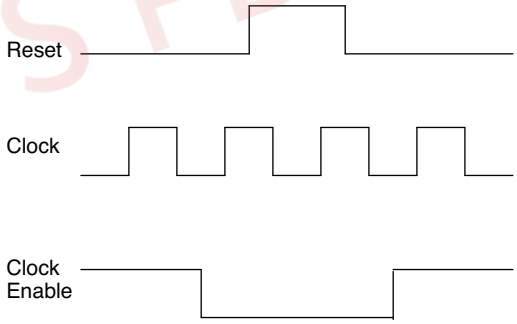


For further information on the sysMEM EBR block, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-10. The reset timing rules apply to the RPReset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For more details refer to TN1201, Memory Usage Guide for MachXO2 Devices.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

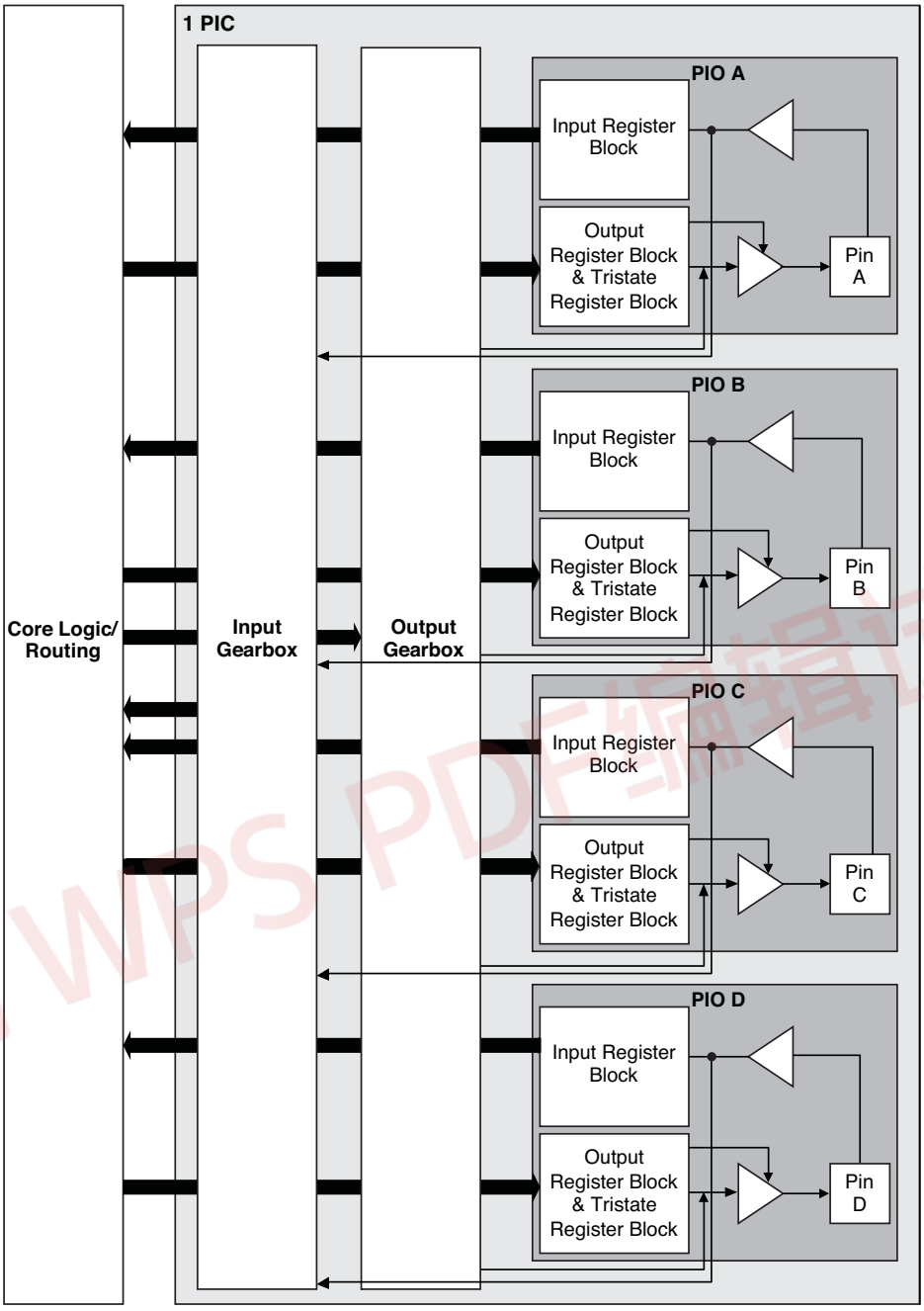
Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO2 devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO2 devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

The MachXO2-640U, MachXO2-1200/U and higher density devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these higher density devices have on-chip differential termination and also provide PCI support.

Figure 2-11. Group of Four Programmable I/O Cells



Notes:
1. Input gearbox is available only in PIC on the bottom edge of MachXO2-640U, MachXO2-1200/U and larger devices.
2. Output gearbox is available only in PIC on the top edge of MachXO2-640U, MachXO2-1200/U and larger devices.

PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Table 2-8. PIO Signal List

Pin Name	I/O Type	Description
CE	Input	Clock Enable
D	Input	Pin input from sysIO buffer.
INDD	Output	Register bypassed input.
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysIO Buffer
TQ	Output	Tri-state output signals to sysIO Buffer
DQSR90[1]	Input	DQS shift 90-degree read clock
DQSW90[1]	Input	DQS shift 90-degree write clock
DDRCLKPOL[1]	Input	DDR input register polarity control signal from DQS
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

1. Available in PIO on right edge only.

Input Register Block

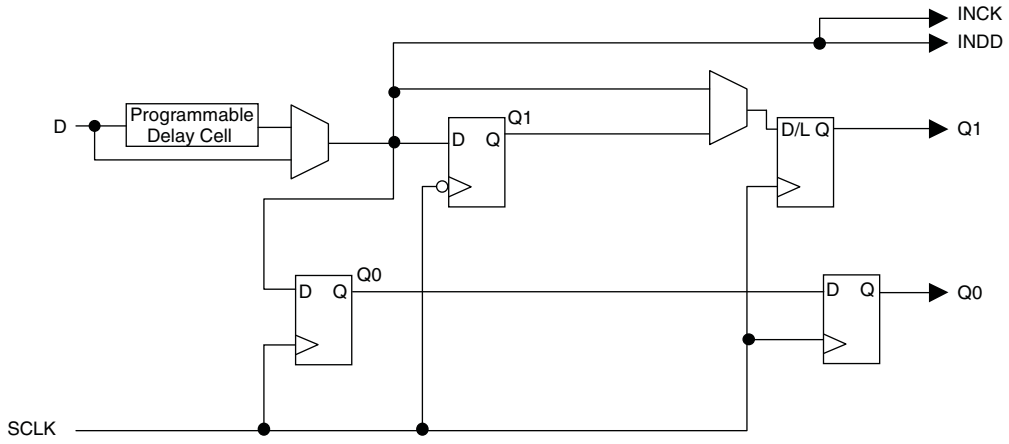
The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition to this functionality, the input register blocks for the PIOs on the right edge include built-in logic to interface to DDR memory.

Figure 2-12 shows the input register block for the PIOs located on the left, top and bottom edges. Figure 2-13 shows the input register block for the PIOs on the right edge.

Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

Figure 2-12. MachXO2 Input Register Block Diagram (PIO on Left, Top and Bottom Edges)



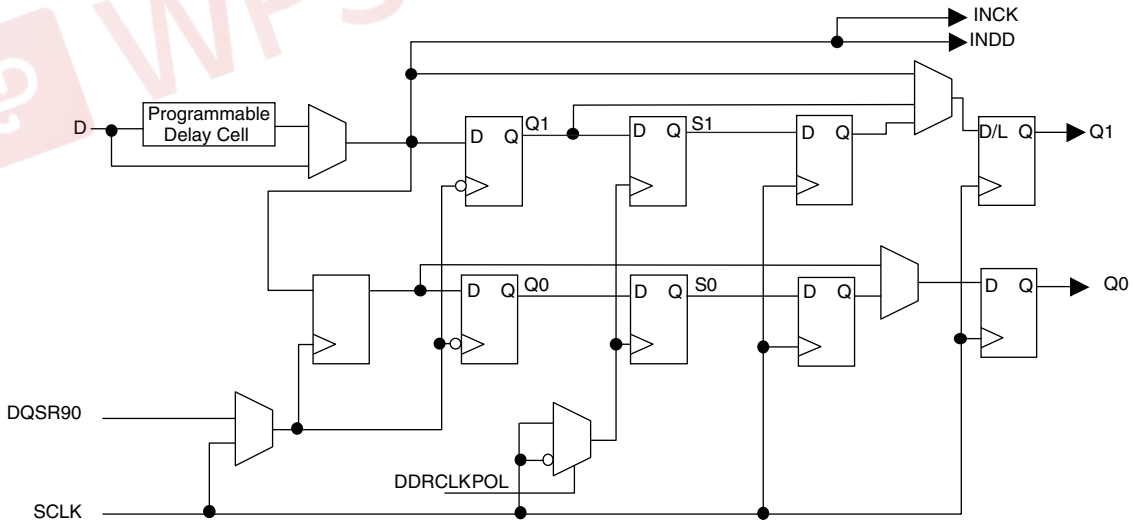
Right Edge

The input register block on the right edge is a superset of the same block on the top, bottom, and left edges. In addition to the modes described above, the input register block on the right edge also supports DDR memory mode.

In DDR memory mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (DQSR90) in the DDR Memory mode creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the DQS domain. The DQSR90 and DDRCLKPOL signals are generated in the DQS read-write block.

Figure 2-13. MachXO2 Input Register Block Diagram (PIO on Right Edge)



Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

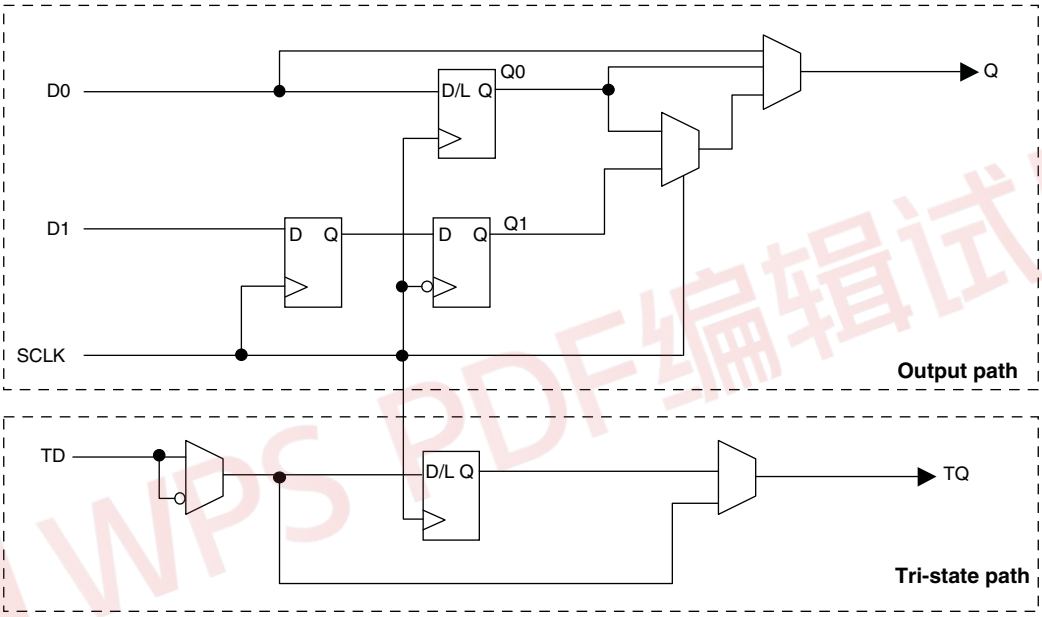
Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-14 shows the output register block on the left, top and bottom edges.

Figure 2-14. MachXO2 Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)



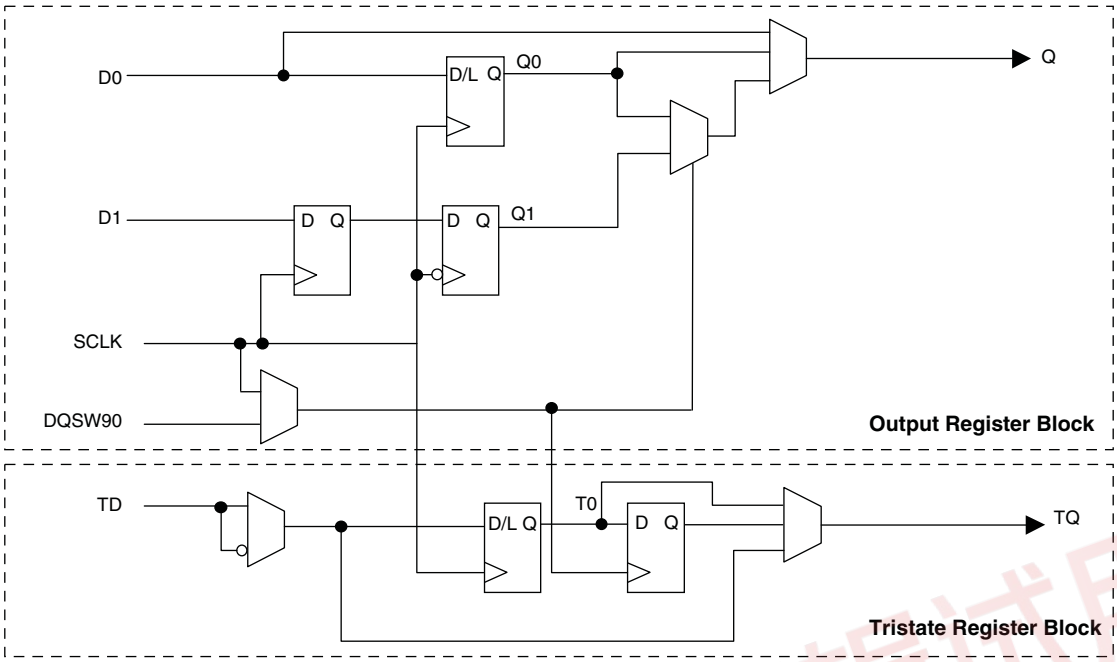
Right Edge

The output register block on the right edge is a superset of the output register on left, top and bottom edges of the device. In addition to supporting SDR and Generic DDR modes, the output register blocks for PIOs on the right edge include additional logic to support DDR-memory interfaces. Operation of this block is similar to that of the output register block on other edges.

In DDR memory mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the DQSW90 signal is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-15 shows the output register block on the right edge.

Figure 2-15. MachXO2 Output Register Block Diagram (PIO on the Right Edges)



Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

The tri-state register blocks on the right edge contain an additional register for DDR memory operation. In DDR memory mode, the register TS input is fed into another register that is clocked using the DQSW90 signal. The output of this register is used as a tri-state control.

Input Gearbox

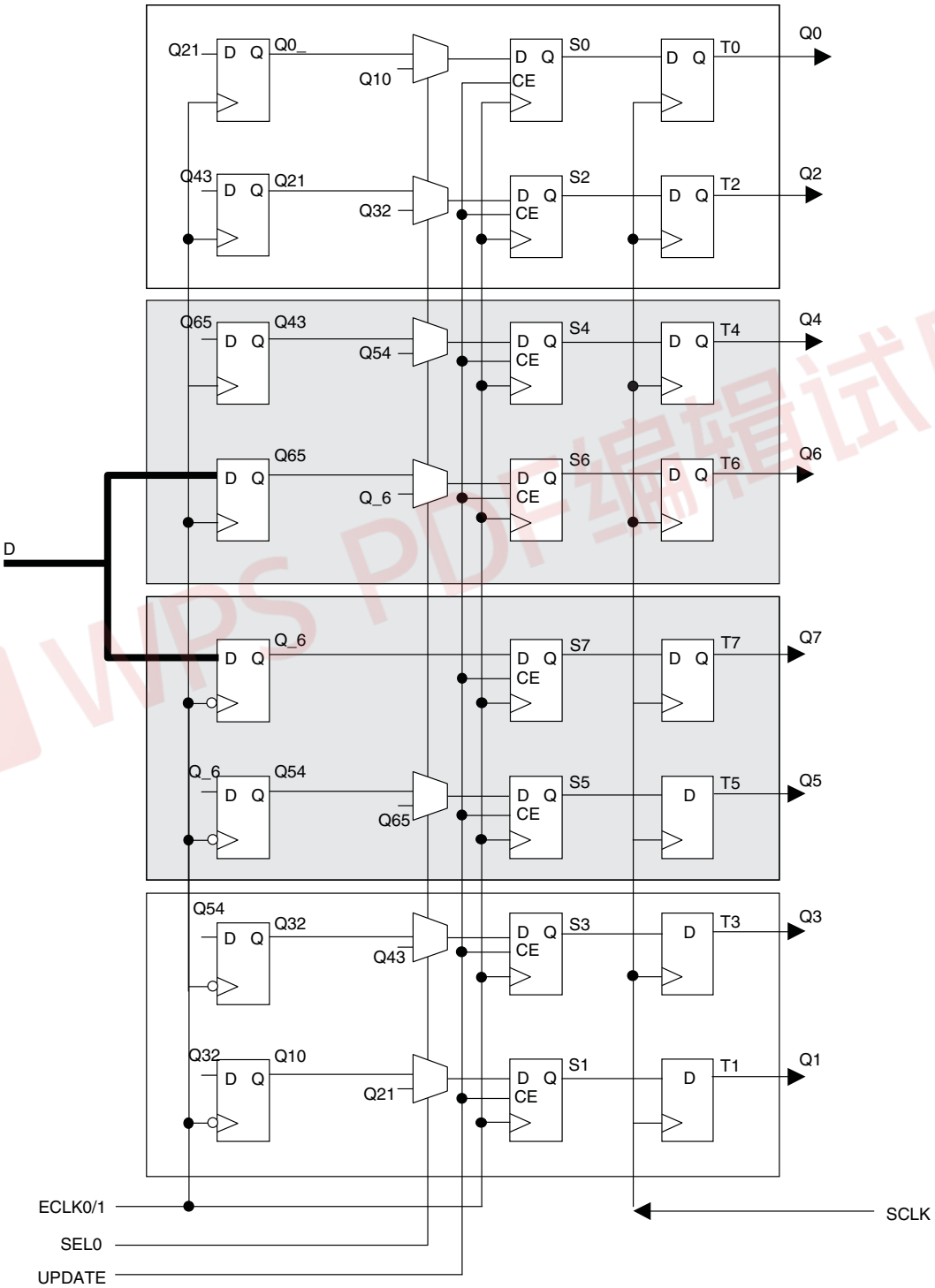
Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

Table 2-9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-16 shows a block diagram of the input gearbox.

Figure 2-16. Input Gearbox



More information on the input gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.

Output Gearbox

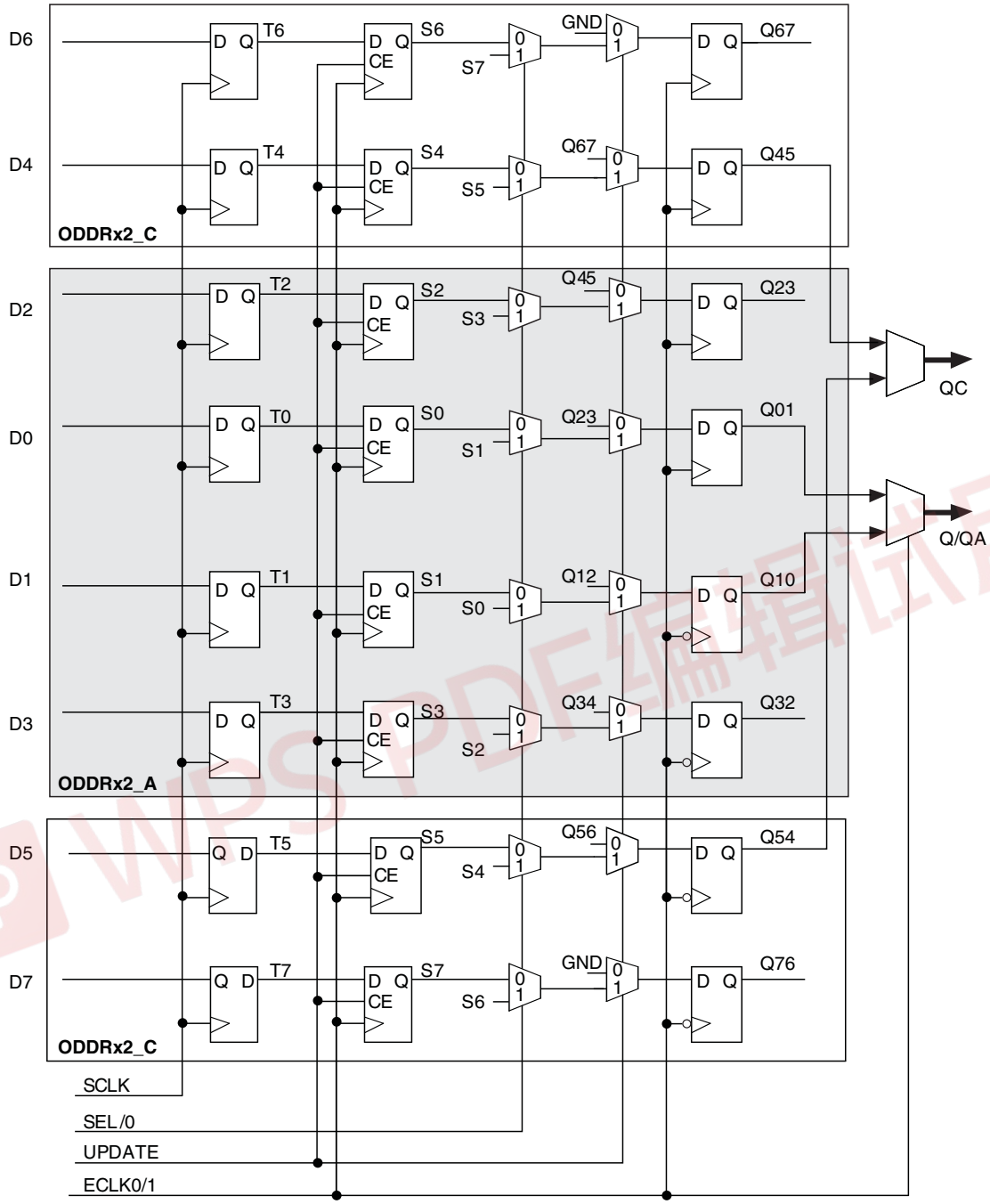
Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

Table 2-10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDRX4(8:1): D[7:0]		
GDDRX2(4:1)(IOL-A): D[3:0]		
GDDRX2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-17 shows the output gearbox block diagram.

Figure 2-17. Output Gearbox



More information on the output gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.

DDR Memory Support

Certain PICs on the right edge of MachXO2-640U, MachXO2-1200/U and larger devices, have additional circuitry to allow the implementation of DDR memory interfaces. There are two groups of 14 or 12 PIOs each on the right edge with additional circuitry to implement DDR memory interfaces. This capability allows the implementation of up to 16-bit wide memory interfaces. One PIO from each group contains a control element, the DQS Read/Write Block, to facilitate the generation of clock and control signals (DQSR90, DQSW90, DDRCLKPOL and DATAVALID). These clock and control signals are distributed to the other PIO in the group through dedicated low skew routing.

DQS Read Write Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Read Write block provides the required clock alignment for DDR memory interfaces. DQSR90 and DQSW90 signals are generated by the DQS Read Write block from the DQS input.

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the read cycle) is unknown. The MachXO2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This circuit changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each read cycle for the correct clock polarity. Prior to the read operation in DDR memories, DQS is in tri-state (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit in the DQS Read Write block detects the first DQS rising edge after the preamble state and generates the DDRCLKPOL signal. This signal is used to control the polarity of the clock to the synchronizing registers.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration signals (6-bit bus) from a DLL on the right edge of the device. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, PCI, SSTL, HSTL, LVDS, BLVDS, MLVDS and LVPECL.

Each bank is capable of supporting multiple I/O standards. In the MachXO2 devices, single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS and PCI), differential (LVDS) and referenced input buffers (SSTL and HSTL) are powered using I/O supply voltage (V_{CCIO}). Each sysIO bank has its own V_{CCIO}. In addition, each bank has a voltage reference, V_{REF}, which allows the use of referenced input buffers independent of the bank V_{CCIO}.

MachXO2-256 and MachXO2-640 devices contain single-ended ratioed input buffers and single-ended output buffers with complementary outputs on all the I/O banks. Note that the single-ended input buffers on these devices do not contain PCI clamps. In addition to the single-ended I/O buffers these two devices also have differential and referenced input buffers on all I/Os. The I/Os are arranged in pairs, the two pads in the pair are described as "T" and "C", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 devices contain three types of sysIO buffer pairs.

1. **Left and Right sysIO Buffer Pairs**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential and referenced input buffers.

2. **Bottom sysIO Buffer Pairs**
   The sysIO buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential and referenced input buffers. Only the I/Os on the bottom banks have programmable PCI clamps and differential input termination. The PCI clamp is enabled after V_{CC} and V_{CCIO} are at valid operating levels and the device has been configured.

3. **Top sysIO Buffer Pairs**
   The sysIO buffer pairs in the top bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential and referenced I/O buffers. Half of the sysIO buffer pairs on the top edge have true differential outputs. The sysIO buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver. The referenced input buffer can also be configured as a differential input buffer.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCIO0} have reached V_{PORUP} level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-down to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to V_{CCIO} as the default functionality). The I/O pins will maintain the blank configuration until V_{CC} and V_{CCIO} (for I/O banks containing configuration I/Os) have reached V_{PORUP} levels at which time the I/Os will take on the user-configured settings only after a proper download/configuration.

Supported Standards

The MachXO2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL, and PCI. The buffer supports the LVTTL, PCI, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO2-640U, MachXO2-1200/U and higher devices support on-chip LVDS output buffers on approximately 50% of the I/Os on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO2 devices. PCI support is provided in the bottom bank of theMachXO2-640U, MachXO2-1200/U and higher density devices. Table 2-11 summarizes the I/O characteristics of the MachXO2 PLDs.

Tables 2-11 and 2-12 show the I/O standards (together with their supply and reference voltages) supported by the MachXO2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1202, MachXO2 sysIO Usage Guide.

Table 2-11. I/O Support Device by Device

	MachXO2-256, MachXO2-640	MachXO2-640U, MachXO2-1200	MachXO2-1200U MachXO2-2000/U, MachXO2-4000, MachXO2-7000
Number of I/O Banks	4	4	6
Type of Input Buffers	Single-ended (all I/O banks) Differential Receivers (all I/O banks)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)
Types of Output Buffers	Single-ended buffers with complementary outputs (all I/O banks)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)
Differential Output Emulation Capability	All I/O banks	All I/O banks	All I/O banks
PCI Clamp Support	No	Clamp on bottom side only	Clamp on bottom side only

Table 2-12. Supported Input Standards

	VCCIO (Typ.)				
Input Standard	**3.3 V**	**2.5 V**	**1.8 V**	**1.5**	**1.2 V**
Single-Ended Interfaces					
LVTTL	✓	✓[2]	✓[2]	✓[2]	
LVCMOS33	✓	✓[2]	✓[2]	✓[2]	
LVCMOS25	✓[2]	✓	✓[2]	✓[2]	
LVCMOS18	✓[2]	✓[2]	✓	✓[2]	
LVCMOS15	✓[2]	✓[2]	✓[2]	✓	✓[2]
LVCMOS12	✓[2]	✓[2]	✓[2]	✓[2]	✓
PCI[1]	✓				
SSTL18 (Class I, Class II)	✓	✓	✓		
SSTL25 (Class I, Class II)	✓	✓			
HSTL18 (Class I, Class II)	✓	✓	✓		
Differential Interfaces					
LVDS	✓	✓			
BLVDS, MVDS, LVPECL, RSDS	✓	✓			
MIPI[3]	✓	✓			
Differential SSTL18 Class I, II	✓	✓	✓		
Differential SSTL25 Class I, II	✓	✓			
Differential HSTL18 Class I, II	✓	✓	✓		

1. Bottom banks of MachXO2-640U, MachXO2-1200/U and higher density devices only.
2. Reduced functionality. Refer to TN1202, MachXO2 sysIO Usage Guide for more detail.
3. These interfaces can be emulated with external resistors in all devices.

Table 2-13. Supported Output Standards

Output Standard	V_{CCIO} (Typ.)
Single-Ended Interfaces	
LVTTL	3.3
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8
LVCMOS15	1.5
LVCMOS12	1.2
LVCMOS33, Open Drain	—
LVCMOS25, Open Drain	—
LVCMOS18, Open Drain	—
LVCMOS15, Open Drain	—
LVCMOS12, Open Drain	—
PCI33	3.3
SSTL25 (Class I)	2.5
SSTL18 (Class I)	1.8
HSTL18(Class I)	1.8
Differential Interfaces	
LVDS[1, 2]	2.5, 3.3
BLVDS, MLVDS, RSDS [2]	2.5
LVPECL[2]	3.3
MIPI[2]	2.5
Differential SSTL18	1.8
Differential SSTL25	2.5
Differential HSTL18	1.8

1. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.

sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO2-1200U, MachXO2-2000/U and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO2-1200 and lower density devices have four banks (one bank per side). Figures 2-18 and 2-19 show the sysIO banks and their associated supplies for all devices.

Figure 2-18. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 Banks

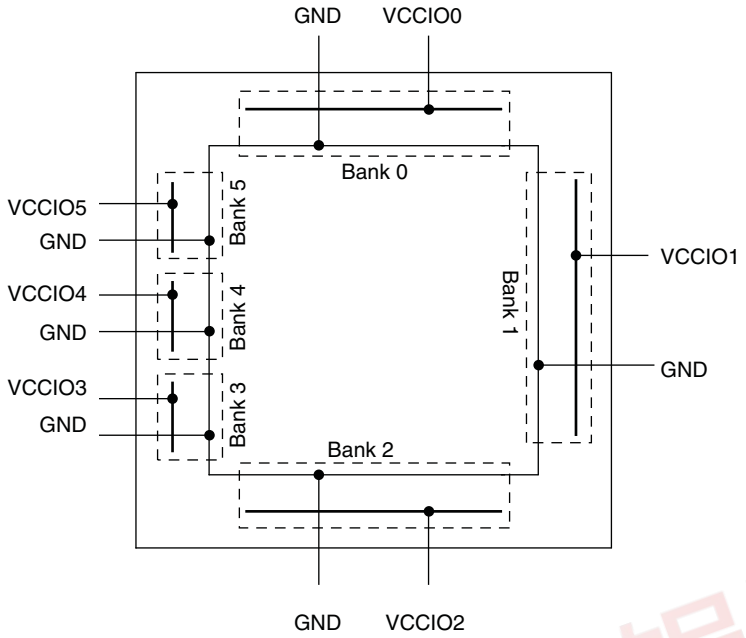
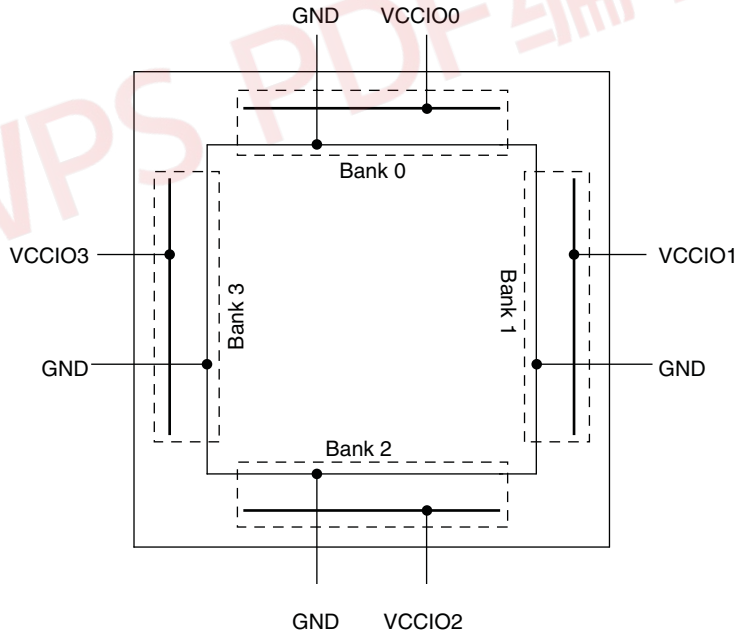


Figure 2-19. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks



Hot Socketing

The MachXO2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO2 ideal for many multiple power supply and hot-swap applications.

On-chip Oscillator

Every MachXO2 device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
2. During configuration, users select a different master clock frequency.
3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-14 lists all the available MCLK frequencies.

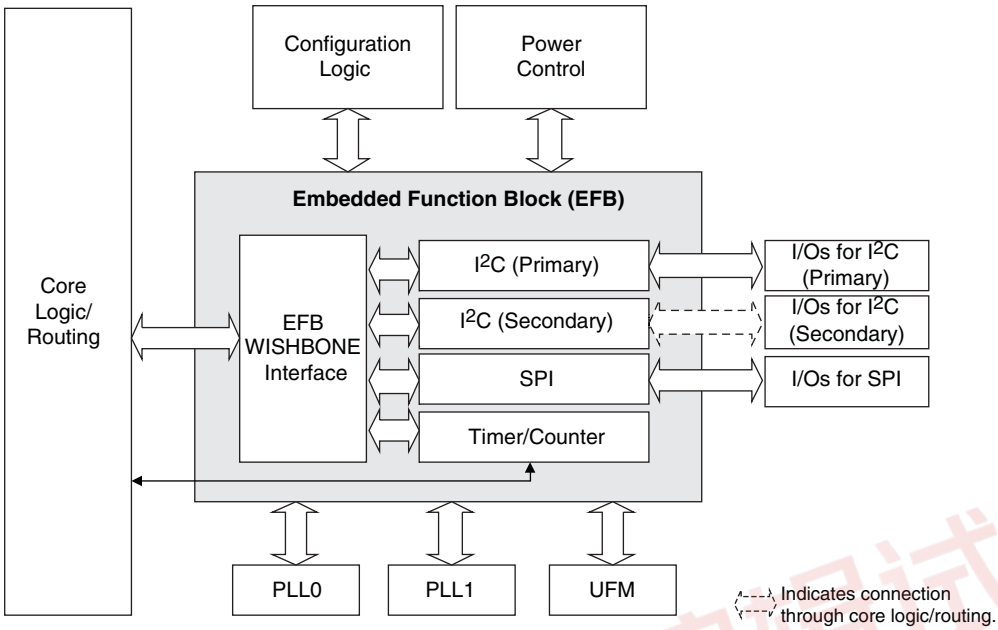
Table 2-14. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

Embedded Hardened IP Functions and User Flash Memory

All MachXO2 devices provide embedded hardened functions such as SPI, I^2C and Timer/Counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2-20.

Figure 2-20. Embedded Function Block Interface



Hardened I²C IP Core

Every MachXO2 device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I²C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface

Figure 2-21. I²C Core Block Diagram

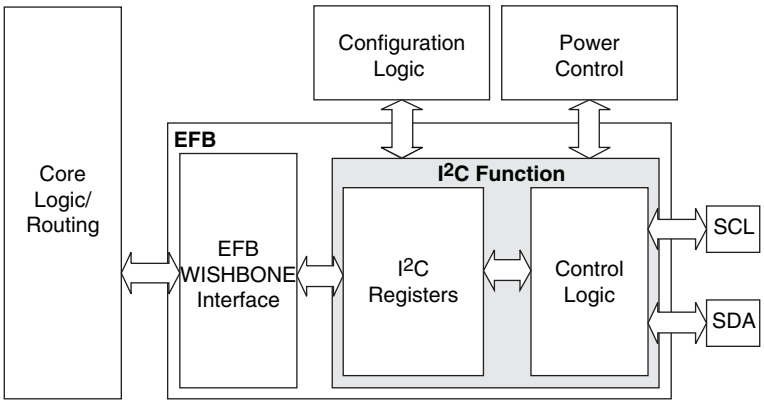


Table 2-15 describes the signals interfacing with the I²C cores.

Table 2-15. I²C Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I²C core. The signal is an output if the I²C core is in master mode. The signal is an input if the I²C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device.
i2c_sda	Bi-directional	Bi-directional data line of the I²C core. The signal is an output when data is transmitted from the I²C core. The signal is an input when data is received into the I²C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device.
i2c_irqo	Output	Interrupt request output signal of the I²C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I²C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.

Hardened SPI IP Core

Every MachXO2 device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO2 devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface

There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology (Appendix B)
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices

Figure 2-22. SPI Core Block Diagram

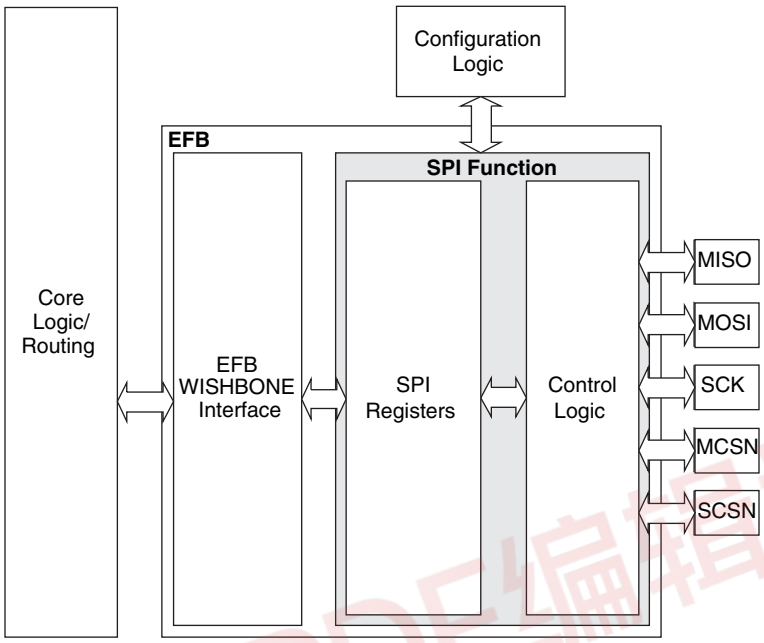


Table 2-16 describes the signals interfacing with the SPI cores.

Table 2-16. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	O	Master	SPI master chip-select output
spi_csn[1..7]	O	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	O	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
ufm_sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the User Flash Memory (UFM).
cfg_stdby	O	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.
cfg_wake	O	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.

Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  - — Watchdog timer
  - — Clear timer on compare match
  - — Fast PWM
  - — Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

Figure 2-23. Timer/Counter Block Diagram

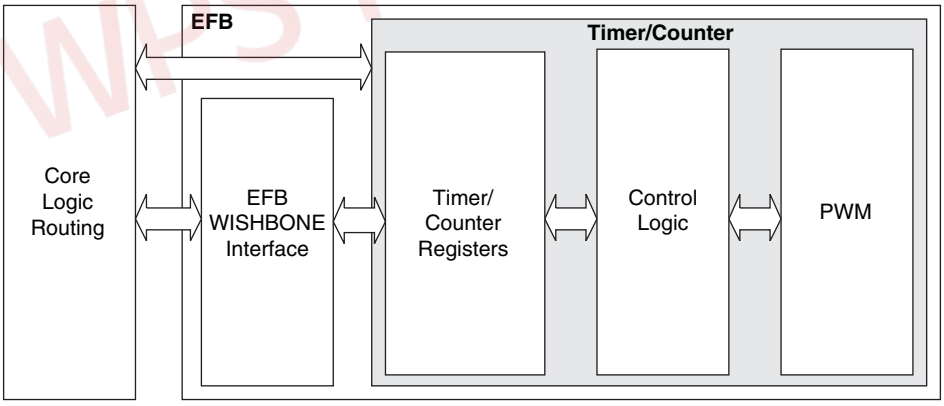


Table 2-17. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	O	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	O	Timer counter output signal

For more details on these embedded functions, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

User Flash Memory (UFM)

MachXO2-640/U and higher density devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I^2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

Standby Mode and Power Saving Options

MachXO2 devices are available in three options for maximum flexibility: ZE, HC and HE devices. The ZE devices have ultra low static and dynamic power consumption. These devices use a 1.2 V core voltage that further reduces power consumption. The HC and HE devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the HE devices operate at 1.2 V V_{CC}.

MachXO2 devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO2 devices support an ultra low power Stand-by mode. While most of these features are available in all three device types, these features are mainly intended for use with MachXO2 ZE devices to manage power consumption.

In the stand-by mode the MachXO2 devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I^2C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO2 devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

Table 2-18. MachXO2 Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe V_{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1198, Power Estimation and Management for MachXO2 Devices.

Power On Reset

MachXO2 devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the V_{PORUP} level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices), V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators (HC devices), V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time ($t_{REFRESH}$) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tristate. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min) they should not shut down the bandgap or POR circuit.

Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I^2C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

1. Internal Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I^2C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, MachXO2 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

TransFR (Transparent Field Reconfiguration)
TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

When implementing background programming of the on-chip Flash, care must be taken for the operation of the PLL. For devices that have two PLLs (XO2-2000U, -4000 and -7000), the system must put the RPLL (Right-side PLL) in reset state during the background Flash programming. More detailed description can be found in TN1204, MachXO2 Programming and Configuration Usage Guide.

Security and One-Time Programmable Mode (OTP)
For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO2 devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile Flash memory spaces. The device can be in one of two modes:

1. Unlocked – Readback of the SRAM configuration and non-volatile Flash memory spaces is allowed.

2. Permanently Locked – The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Dual Boot
MachXO2 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the on-chip Flash. The golden image MUST reside in an external SPI Flash. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Soft Error Detection
The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1206, MachXO2 Soft Error Detection Usage Guide.

TraceID

Each MachXO2 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I^2C, or JTAG interfaces.

Density Shifting

The MachXO2 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO2 migration files.

MachXO2 Family Data Sheet DC and Switching Characteristics

March 2017 Data Sheet DS1035

Absolute Maximum Ratings[1, 2, 3]

	MachXO2 ZE/HE (1.2 V)	MachXO2 HC (2.5 V / 3.3 V)
Supply Voltage V_{CC}	–0.5 V to 1.32 V	–0.5 V to 3.75 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied[4, 5]	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied[4]	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T_J)	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to (V_{IHMAX} + 2) volts is permitted for a duration of <20 ns.
5. The dual function I^2C pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.

Recommended Operating Conditions[1]

Symbol	Parameter	Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V / 3.3 V Devices	2.375	3.6	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	1.14	3.6	V
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature Industrial Operation	–40	100	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

Power Supply Ramp Rates[1]

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.01	—	100	V/ms

1. Assumes monotonic ramp rates.

Power-On-Reset Voltage Levels[1, 2, 3, 4, 5]

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and V_{CCIO0})	0.9	—	1.06	V
$V_{PORUPEXT}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	—	2.1	V
$V_{PORDNBG}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CCINT})	0.75	—	0.93	V
$V_{PORDNBGEXT}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	—	1.33	V
$V_{PORDNSRAM}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CCINT})	—	0.6	—	V
$V_{PORDNSRAMEXT}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	—	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.
3. Note that V_{PORUP} (min.) and $V_{PORDNBG}$ (max.) are in different process corners. For any given process corner $V_{PORDNBG}$ (max.) is always 12.0 mV below V_{PORUP} (min.).
4. $V_{PORUPEXT}$ is for HC devices only. In these devices a separate POR circuit monitors the external V_{CC} power supply.
5. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

Programming/Erase Specifications

Symbol	Parameter	Min.	Max.[1]	Units
$N_{PROGCYC}$	Flash Programming cycles per $t_{RETENTION}$	—	10,000	Cycles
	Flash functional programming cycles	—	100,000	
$t_{RETENTION}$	Data retention at 100 °C junction temperature	10	—	Years
	Data retention at 85 °C junction temperature	20	—	

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Max.	Units
I_{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/–1000	µA

1. Insensitive to sequence of V_{CC} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO}.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

ESD Performance

Please refer to the MachXO2 Product Family Qualification Summary for complete qualification data, including ESD performance.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4]	Input or I/O Leakage	Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX)	—	—	+175	µA
		Clamp OFF and $V_{IN} = V_{CCIO}$	–10	—	10	µA
		Clamp OFF and V_{CCIO} –0.97 V < V_{IN} < V_{CCIO}	–175	—	—	µA
		Clamp OFF and 0 V < V_{IN} < V_{CCIO} –0.97 V	—	—	10	µA
		Clamp OFF and V_{IN} = GND	—	—	10	µA
		Clamp ON and 0 V < V_{IN} < V_{CCIO}	—	—	10	µA
I_{PU}	I/O Active Pull-up Current	0 < V_{IN} < 0.7 V_{CCIO}	–30	—	-309	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) < V_{IN} < V_{CCIO}	30	—	305	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	–30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	305	µA
I_{BHHO}	Bus Hold High Overdrive current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	–309	µA
V_{BHT}[3]	Bus Hold Trip Points		V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	3	5	9	pF
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	3	5.5	7	pF
V_{HYST}	Hysteresis for Schmitt Trigger Inputs[5]	V_{CCIO} = 3.3 V, Hysteresis = Large	—	450	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Large	—	250	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Large	—	125	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Large	—	100	—	mV
		V_{CCIO} = 3.3 V, Hysteresis = Small	—	250	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Small	—	150	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Small	—	60	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Small	—	40	—	mV

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. When V_{IH} is higher than V_{CCIO}, a transient current typically of 30 ns in duration or less with a peak current of 6 mA can occur on the high-to-low transition. For true LVDS output pins in MachXO2-640U, MachXO2-1200/U and larger devices, V_{IH} must be less than or equal to V_{CCIO}.
5. With bus keeper circuit turned on. For more details, refer to TN1202, MachXO2 sysIO Usage Guide.

Static Supply Current – ZE Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO2-256ZE	18	µA
		LCMXO2-640ZE	28	µA
		LCMXO2-1200ZE	56	µA
		LCMXO2-2000ZE	80	µA
		LCMXO2-4000ZE	124	µA
		LCMXO2-7000ZE	189	µA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	1	µA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off. To estimate the impact of turning each of these items on, please refer to the following table or for more detail with your specific design use the Power Calculator tool.
3. Frequency = 0 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Static Power Consumption Contribution of Different Components – ZE Devices

The table below can be used for approximating static power consumption. For a more accurate power analysis for your design please use the Power Calculator tool.

Symbol	Parameter	Typ.	Units
I_{DCBG}	Bandgap DC power contribution	101	µA
I_{DCPOR}	POR DC power contribution	38	µA
$I_{DCIOBANKCONTROLLER}$	DC power contribution per I/O bank controller	143	µA

Static Supply Current – HC/HE Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO2-256HC	1.15	mA
		LCMXO2-640HC	1.84	mA
		LCMXO2-640UHC	3.48	mA
		LCMXO2-1200HC	3.49	mA
		LCMXO2-1200UHC	4.80	mA
		LCMXO2-2000HC	4.80	mA
		LCMXO2-2000UHC	8.44	mA
		LCMXO2-4000HC	8.45	mA
		LCMXO2-7000HC	12.87	mA
		LCMXO2-2000HE	1.39	mA
		LCMXO2-4000HE	2.55	mA
		LCMXO2-7000HE	4.06	mA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
3. Frequency = 0 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Programming and Erase Flash Supply Current – HC/HE Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO2-256HC	14.6	mA
		LCMXO2-640HC	16.1	mA
		LCMXO2-640UHC	18.8	mA
		LCMXO2-1200HC	18.8	mA
		LCMXO2-1200UHC	22.1	mA
		LCMXO2-2000HC	22.1	mA
		LCMXO2-2000UHC	26.8	mA
		LCMXO2-4000HC	26.8	mA
		LCMXO2-7000HC	33.2	mA
		LCMXO2-2000HE	18.3	mA
		LCMXO2-2000UHE	20.4	mA
		LCMXO2-4000HE	20.4	mA
		LCMXO2-7000HE	23.9	mA
I_{CCIO}	Bank Power Supply[6]	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. T_J = 25 °C, power supplies at nominal voltage.
6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

Programming and Erase Flash Supply Current – ZE Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO2-256ZE	13	mA
		LCMXO2-640ZE	14	mA
		LCMXO2-1200ZE	15	mA
		LCMXO2-2000ZE	17	mA
		LCMXO2-4000ZE	18	mA
		LCMXO2-7000ZE	20	mA
I_{CCIO}	Bank Power Supply[6]	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. TJ = 25 °C, power supplies at nominal voltage.
6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.6	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.6	—	—	—
PCI[3]	3.135	3.3	3.6	—	—	—
SSTL25	2.375	2.5	2.625	1.15	1.25	1.35
SSTL18	1.71	1.8	1.89	0.833	0.9	0.969
HSTL18	1.71	1.8	1.89	0.816	0.9	1.08
LVCMOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVCMOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVCMOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVCMOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVCMOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVCMOS12R33[4]	3.135	3.3	3.6	0.45	0.6	0.75
LVCMOS12R25[4]	2.375	2.5	2.625	0.45	0.6	0.75
LVCMOS10R33[4]	3.135	3.3	3.6	0.35	0.5	0.65
LVCMOS10R25[4]	2.375	2.5	2.625	0.35	0.5	0.65
LVDS25[1, 2]	2.375	2.5	2.625	—	—	—
LVDS33[1, 2]	3.135	3.3	3.6	—	—	—
LVPECL[1]	3.135	3.3	3.6	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—
RSDS[1]	2.375	2.5	2.625	—	—	—
SSTL18D	1.71	1.8	1.89	—	—	—
SSTL25D	2.375	2.5	2.625	—	—	—
HSTL18D	1.71	1.8	1.89	—	—	—

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
3. Input on the bottom bank of the MachXO2-640U, MachXO2-1200/U and larger devices only.
4. Supported only for inputs and BIDIs for all ZE devices, and –6 speed grade for HE and HC devices.

sysIO Single-Ended DC Electrical Characteristics[1, 2]

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max.[4] (mA)	I_{OH} Max.[4] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3 LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
							16	–16
							24	–24
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
							16	–16
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.5	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.2	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} – 0.4	4	–2
							8	–6
					0.2	V_{CCIO} – 0.2	0.1	–0.1
PCI	–0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	–0.5
SSTL25 Class I	–0.3	V_{REF} – 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	8	8
SSTL25 Class II	–0.3	V_{REF} – 0.18	V_{REF} + 0.18	3.6	NA	NA	NA	NA
SSTL18 Class I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	3.6	0.40	V_{CCIO} - 0.40	8	8
SSTL18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	3.6	NA	NA	NA	NA
HSTL18 Class I	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	V_{CCIO} - 0.40	8	8
HSTL18 Class II	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS25R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS12R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max.[4] (mA)	I_{OH} Max.[4] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS10R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain

1. MachXO2 devices allow LVCMOS inputs to be placed in I/O banks where V_{CCIO} is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO2 devices do not meet the relevant JEDEC specification are documented in the table below.
2. MachXO2 devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1202, MachXO2 sysIO Usage Guide.
3. The dual function I^2C pins SCL and SDA are limited to a V_{IL} min of –0.25 V or to –0.3 V with a duration of <10 ns.
4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive VCCIO or GND pad connections, or between the last VCCIO or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n * 8 mA. “n” is the number of I/O pads between the two consecutive bank VCCIO or GND connections or between the last VCCIO and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

Input Standard	V_{CCIO} (V)	V_{IL} Max. (V)
LVCMOS 33	1.5	0.685
LVCMOS 25	1.5	0.687
LVCMOS 18	1.5	0.655

sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of MachXO2-640U, MachXO2-1200/U and higher density devices in the MachXO2 PLD family.

LVDS

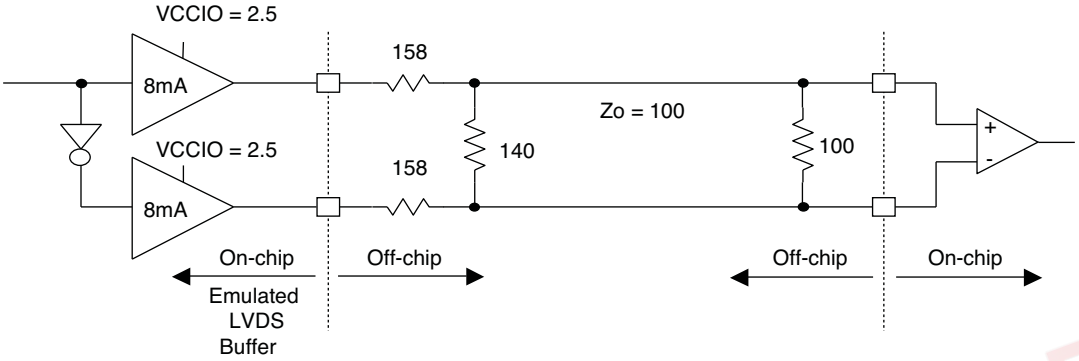
Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO} = 3.3 V	0	—	2.605	V
		V_{CCIO} = 2.5 V	0	—	2.05	V
V_{THD}	Differential Input Threshold		±100	—		mV
V_{CM}	Input Common Mode Voltage	V_{CCIO} = 3.3 V	0.05	—	2.6	V
		V_{CCIO} = 2.5 V	0.05	—	2.0	V
I_{IN}	Input current	Power on	—	—	±10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.375	—	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.90	1.025	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.395	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0 V driver outputs shorted	—	—	24	mA

LVDS Emulation

MachXO2 devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

Figure 3-1. LVDS Using External Resistors (LVDS25E)



Note: All resistors are ±1%.

Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	158	Ohms
R_P	Driver parallel resistor	140	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	6.03	mA

BLVDS

The MachXO2 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

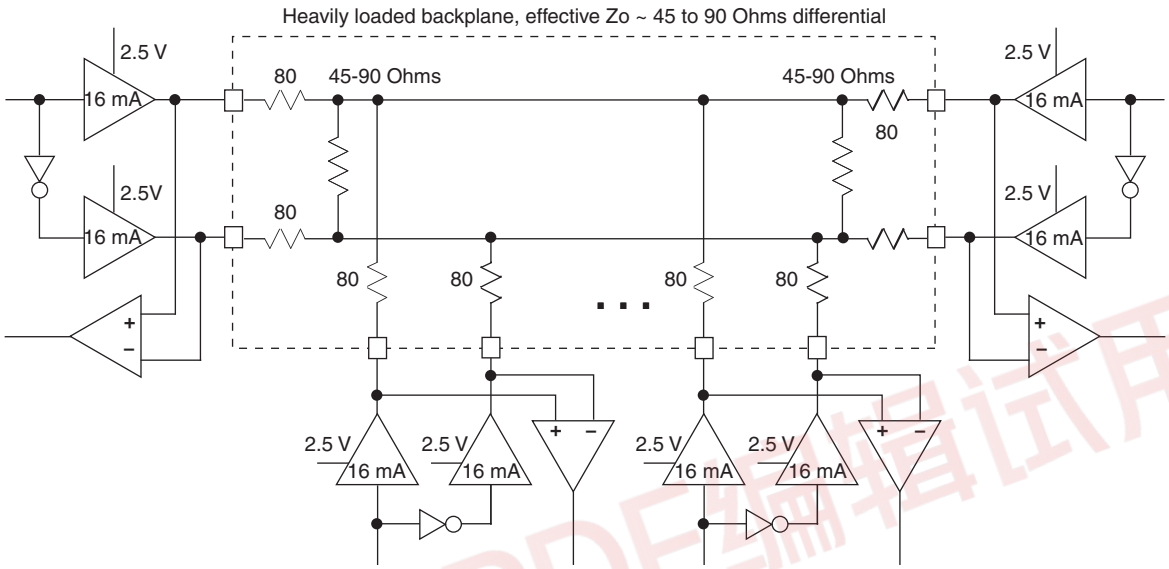


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	20	20	Ohms
R_S	Driver series resistance	80	80	Ohms
R_{TLEFT}	Left end termination	45	90	Ohms
R_{TRIGHT}	Right end termination	45	90	Ohms
V_{OH}	Output high voltage	1.376	1.480	V
V_{OL}	Output low voltage	1.124	1.020	V
V_{OD}	Output differential voltage	0.253	0.459	V
V_{CM}	Output common mode voltage	1.250	1.250	V
I_{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.

LVPECL

The MachXO2 family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

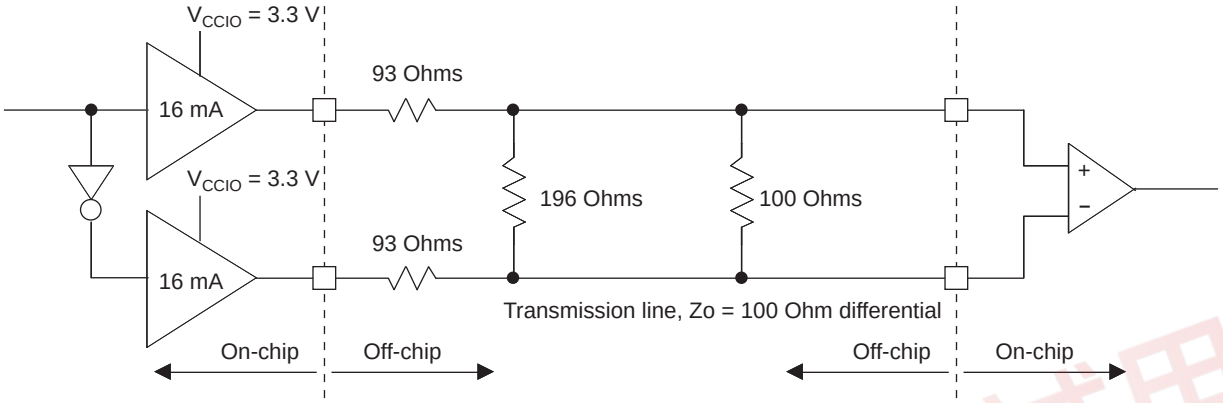


Table 3-3. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	93	Ohms
R_P	Driver parallel resistor	196	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	2.05	V
V_{OL}	Output low voltage	1.25	V
V_{OD}	Output differential voltage	0.80	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	12.11	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

RSDS

The MachXO2 family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

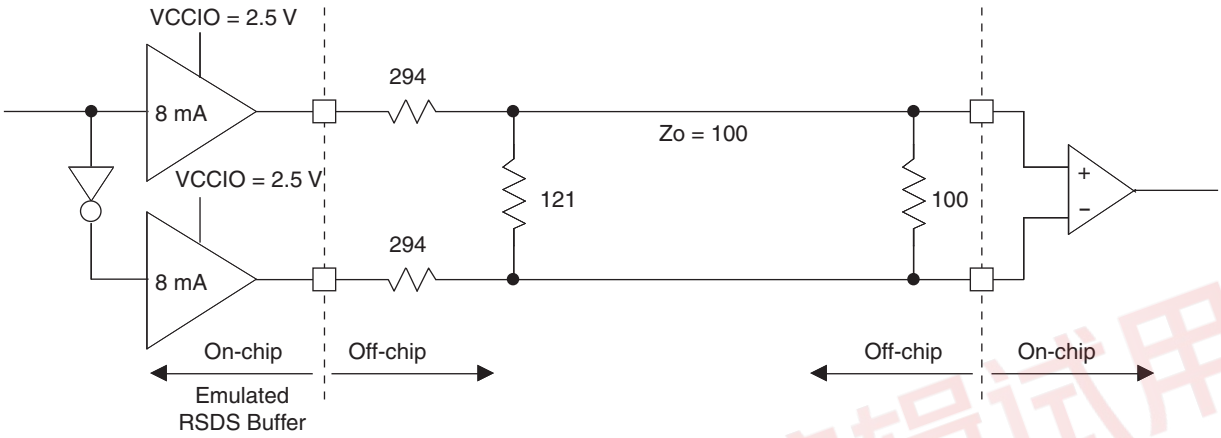


Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	294	Ohms
R_P	Driver parallel resistor	121	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	Ohms
I_{DC}	DC output current	3.66	mA

Typical Building Block Function Performance – HC/HE Devices[1]

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	-6 Timing	Units
Basic Functions		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

Register-to-Register Performance

Function	-6 Timing	Units
Basic Functions		
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

Typical Building Block Function Performance – ZE Devices[1]

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–3 Timing	Units
Basic Functions		
16-bit decoder	13.9	ns
4:1 MUX	10.9	ns
16:1 MUX	12.0	ns

Register-to-Register Performance

Function	–3 Timing	Units
Basic Functions		
16:1 MUX	191	MHz
16-bit adder	134	MHz
16-bit counter	148	MHz
64-bit counter	77	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	90	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	214	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
LVDS25	400	MHz
LVDS25E	150	MHz
RSDS25	150	MHz
RSDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
SSTL25_I	150	MHz
SSTL25_II	150	MHz
SSTL25D_I	150	MHz
SSTL25D_II	150	MHz
SSTL18_I	150	MHz
SSTL18_II	150	MHz
SSTL18D_I	150	MHz
SSTL18D_II	150	MHz
HSTL18_I	150	MHz
HSTL18_II	150	MHz
HSTL18D_I	150	MHz
HSTL18D_II	150	MHz
PCI33	134	MHz
LVTTL33	150	MHz
LVTTL33D	150	MHz
LVCMOS33	150	MHz
LVCMOS33D	150	MHz
LVCMOS25	150	MHz
LVCMOS25D	150	MHz
LVCMOS25R33	150	MHz
LVCMOS18	150	MHz
LVCMOS18D	150	MHz
LVCMOS18R33	150	MHz
LVCMOS18R25	150	MHz
LVCMOS15	150	MHz
LVCMOS15D	150	MHz
LVCMOS15R33	150	MHz
LVCMOS15R25	150	MHz
LVCMOS12	91	MHz
LVCMOS12D	91	MHz

MachXO2 External Switching Characteristics – HC/HE Devices[1, 2, 3, 4, 5, 6, 7]

Over Recommended Operating Conditions

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f_{MAX_PRI}[8]	Frequency for Primary Clock Tree	All MachXO2 devices	—	388	—	323	—	269	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	0.5	—	0.6	—	0.7	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO2-256HC-HE	—	912	—	939	—	975	ps
		MachXO2-640HC-HE	—	844	—	871	—	908	ps
		MachXO2-1200HC-HE	—	868	—	902	—	951	ps
		MachXO2-2000HC-HE	—	867	—	897	—	941	ps
		MachXO2-4000HC-HE	—	865	—	892	—	931	ps
		MachXO2-7000HC-HE	—	902	—	942	—	989	ps
Edge Clock									
f_{MAX_EDGE}[8]	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	400	—	333	—	278	MHz
Pin-LUT-Pin Propagation Delay									
t_{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	—	6.72	—	6.96	—	7.24	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t_{CO}	Clock to Output – PIO Output Register	MachXO2-256HC-HE	—	7.13	—	7.30	—	7.57	ns
		MachXO2-640HC-HE	—	7.15	—	7.30	—	7.57	ns
		MachXO2-1200HC-HE	—	7.44	—	7.64	—	7.94	ns
		MachXO2-2000HC-HE	—	7.46	—	7.66	—	7.96	ns
		MachXO2-4000HC-HE	—	7.51	—	7.71	—	8.01	ns
		MachXO2-7000HC-HE	—	7.54	—	7.75	—	8.06	ns
t_{SU}	Clock to Data Setup – PIO Input Register	MachXO2-256HC-HE	–0.06	—	–0.06	—	–0.06	—	ns
		MachXO2-640HC-HE	–0.06	—	–0.06	—	–0.06	—	ns
		MachXO2-1200HC-HE	–0.17	—	–0.17	—	–0.17	—	ns
		MachXO2-2000HC-HE	–0.20	—	–0.20	—	–0.20	—	ns
		MachXO2-4000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-7000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	MachXO2-256HC-HE	1.75	—	1.95	—	2.16	—	ns
		MachXO2-640HC-HE	1.75	—	1.95	—	2.16	—	ns
		MachXO2-1200HC-HE	1.88	—	2.12	—	2.36	—	ns
		MachXO2-2000HC-HE	1.89	—	2.13	—	2.37	—	ns
		MachXO2-4000HC-HE	1.94	—	2.18	—	2.43	—	ns
		MachXO2-7000HC-HE	1.98	—	2.23	—	2.49	—	ns

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-256HC-HE	1.42	—	1.59	—	1.96	—	ns
		MachXO2-640HC-HE	1.41	—	1.58	—	1.96	—	ns
		MachXO2-1200HC-HE	1.63	—	1.79	—	2.17	—	ns
		MachXO2-2000HC-HE	1.61	—	1.76	—	2.13	—	ns
		MachXO2-4000HC-HE	1.66	—	1.81	—	2.19	—	ns
		MachXO2-7000HC-HE	1.53	—	1.67	—	2.03	—	ns
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-256HC-HE	–0.24	—	–0.24	—	–0.24	—	ns
		MachXO2-640HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-1200HC-HE	–0.24	—	–0.24	—	–0.24	—	ns
		MachXO2-2000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000HC-HE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-7000HC-HE	–0.21	—	–0.21	—	–0.21	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices	—	388	—	323	—	269	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
t_{COE}	Clock to Output – PIO Output Register	MachXO2-1200HC-HE	—	7.53	—	7.76	—	8.10	ns
		MachXO2-2000HC-HE	—	7.53	—	7.76	—	8.10	ns
		MachXO2-4000HC-HE	—	7.45	—	7.68	—	8.00	ns
		MachXO2-7000HC-HE	—	7.53	—	7.76	—	8.10	ns
t_{SUE}	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
		MachXO2-2000HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
		MachXO2-4000HC-HE	–0.16	—	–0.16	—	–0.16	—	ns
		MachXO2-7000HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
t_{HE}	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	1.97	—	2.24	—	2.52	—	ns
		MachXO2-2000HC-HE	1.97	—	2.24	—	2.52	—	ns
		MachXO2-4000HC-HE	1.89	—	2.16	—	2.43	—	ns
		MachXO2-7000HC-HE	1.97	—	2.24	—	2.52	—	ns
t_{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	1.56	—	1.69	—	2.05	—	ns
		MachXO2-2000HC-HE	1.56	—	1.69	—	2.05	—	ns
		MachXO2-4000HC-HE	1.74	—	1.88	—	2.25	—	ns
		MachXO2-7000HC-HE	1.66	—	1.81	—	2.17	—	ns
t_{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-2000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000HC-HE	–0.34	—	–0.34	—	–0.34	—	ns
		MachXO2-7000HC-HE	–0.29	—	–0.29	—	–0.29	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t_{COPLL}	Clock to Output – PIO Output Register	MachXO2-1200HC-HE	—	5.97	—	6.00	—	6.13	ns
		MachXO2-2000HC-HE	—	5.98	—	6.01	—	6.14	ns
		MachXO2-4000HC-HE	—	5.99	—	6.02	—	6.16	ns
		MachXO2-7000HC-HE	—	6.02	—	6.06	—	6.20	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	0.36	—	0.36	—	0.65	—	ns
		MachXO2-2000HC-HE	0.36	—	0.36	—	0.63	—	ns
		MachXO2-4000HC-HE	0.35	—	0.35	—	0.62	—	ns
		MachXO2-7000HC-HE	0.34	—	0.34	—	0.59	—	ns

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HPLL}	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	0.41	—	0.48	—	0.55	—	ns
		MachXO2-2000HC-HE	0.42	—	0.49	—	0.56	—	ns
		MachXO2-4000HC-HE	0.43	—	0.50	—	0.58	—	ns
		MachXO2-7000HC-HE	0.46	—	0.54	—	0.62	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	2.88	—	3.19	—	3.72	—	ns
		MachXO2-2000HC-HE	2.87	—	3.18	—	3.70	—	ns
		MachXO2-4000HC-HE	2.96	—	3.28	—	3.81	—	ns
		MachXO2-7000HC-HE	3.05	—	3.35	—	3.87	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-2000HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-4000HC-HE	–0.87	—	–0.87	—	–0.87	—	ns
		MachXO2-7000HC-HE	–0.91	—	–0.91	—	–0.91	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.317	—	0.344	—	0.368	UI
t_{DVE}	Input Data Hold After CLK		0.742	—	0.702	—	0.668	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	All MachXO2 devices, all sides	0.566	—	0.560	—	0.538	—	ns
t_{HO}	Input Data Hold After CLK		0.778	—	0.879	—	1.090	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.316	—	0.342	—	0.364	UI
t_{DVE}	Input Data Hold After CLK		0.710	—	0.675	—	0.679	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.233	—	0.219	—	0.198	—	ns
t_{HO}	Input Data Hold After CLK		0.287	—	0.287	—	0.344	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only.[11]	—	0.290	—	0.320	—	0.345	UI
t_{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	0.703	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only.[11]	0.233	—	0.219	—	0.198	—	ns
t_{HO}	Input Data Hold After ECLK		0.287	—	0.287	—	0.344	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1)[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only.[11]	—	0.290	—	0.320	—	0.345	UI
t_{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	0.703	—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	All MachXO2 devices, all sides.	—	0.520	—	0.550	—	0.580	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.520	—	0.550	—	0.580	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK frequency		—	150	—	125	—	104	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	All MachXO2 devices, all sides.	1.210	—	1.510	—	1.870	—	ns
t_{DVA}	Output Data Valid After CLK Output		1.210	—	1.510	—	1.870	—	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		—	150	—	125	—	104	MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.535	—	0.670	—	0.830	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	0.830	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.455	—	0.570	—	0.710	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.455	—	0.570	—	0.710	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[9, 12]									
t_{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.160	—	0.180	—	0.200	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.160	—	0.180	—	0.200	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.369	—	0.395	—	0.421	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.529	—	0.530	—	0.527	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM LPDDR Serial Data Speed		—	280	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	140	—	125	—	104	MHz
f_{LPDDR}	LPDDR Data Transfer Rate		0	280	0	250	0	208	Mbps
DDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.350	—	0.387	—	0.414	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.545	—	0.538	—	0.532	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	150	—	125	—	104	MHz
f_{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps
DDR2[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.360	—	0.378	—	0.406	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.555	—	0.549	—	0.542	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	150	—	125	—	104	MHz
f_{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
7. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps (–6), 113 ps (–5), 120 ps (–4).
8. This number for general purpose usage. Duty cycle tolerance is +/– 10%.
9. Duty cycle is +/–5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32 QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

MachXO2 External Switching Characteristics – ZE Devices[1, 2, 3, 4, 5, 6, 7]

Over Recommended Operating Conditions

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f_{MAX_PRI}[8]	Frequency for Primary Clock Tree	All MachXO2 devices	—	150	—	125	—	104	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	1.00	—	1.20	—	1.40	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO2-256ZE	—	1250	—	1272	—	1296	ps
		MachXO2-640ZE	—	1161	—	1183	—	1206	ps
		MachXO2-1200ZE	—	1213	—	1267	—	1322	ps
		MachXO2-2000ZE	—	1204	—	1250	—	1296	ps
		MachXO2-4000ZE	—	1195	—	1233	—	1269	ps
		MachXO2-7000ZE	—	1243	—	1268	—	1296	ps
Edge Clock									
f_{MAX_EDGE}[8]	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	210	—	175	—	146	MHz
Pin-LUT-Pin Propagation Delay									
t_{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	—	9.35	—	9.78	—	10.21	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t_{CO}	Clock to Output – PIO Output Register	MachXO2-256ZE	—	10.46	—	10.86	—	11.25	ns
		MachXO2-640ZE	—	10.52	—	10.92	—	11.32	ns
		MachXO2-1200ZE	—	11.24	—	11.68	—	12.12	ns
		MachXO2-2000ZE	—	11.27	—	11.71	—	12.16	ns
		MachXO2-4000ZE	—	11.28	—	11.78	—	12.28	ns
		MachXO2-7000ZE	—	11.22	—	11.76	—	12.30	ns
t_{SU}	Clock to Data Setup – PIO Input Register	MachXO2-256ZE	–0.21	—	–0.21	—	–0.21	—	ns
		MachXO2-640ZE	–0.22	—	–0.22	—	–0.22	—	ns
		MachXO2-1200ZE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-2000ZE	–0.27	—	–0.27	—	–0.27	—	ns
		MachXO2-4000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-7000ZE	–0.33	—	–0.33	—	–0.33	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	MachXO2-256ZE	3.96	—	4.25	—	4.65	—	ns
		MachXO2-640ZE	4.01	—	4.31	—	4.71	—	ns
		MachXO2-1200ZE	3.95	—	4.29	—	4.73	—	ns
		MachXO2-2000ZE	3.94	—	4.29	—	4.74	—	ns
		MachXO2-4000ZE	3.96	—	4.36	—	4.87	—	ns
		MachXO2-7000ZE	3.93	—	4.37	—	4.91	—	ns

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-256ZE	2.62	—	2.91	—	3.14	—	ns
		MachXO2-640ZE	2.56	—	2.85	—	3.08	—	ns
		MachXO2-1200ZE	2.30	—	2.57	—	2.79	—	ns
		MachXO2-2000ZE	2.25	—	2.50	—	2.70	—	ns
		MachXO2-4000ZE	2.39	—	2.60	—	2.76	—	ns
		MachXO2-7000ZE	2.17	—	2.33	—	2.43	—	ns
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-256ZE	–0.44	—	–0.44	—	–0.44	—	ns
		MachXO2-640ZE	–0.43	—	–0.43	—	–0.43	—	ns
		MachXO2-1200ZE	–0.28	—	–0.28	—	–0.28	—	ns
		MachXO2-2000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-4000ZE	–0.34	—	–0.34	—	–0.34	—	ns
		MachXO2-7000ZE	–0.21	—	–0.21	—	–0.21	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices	—	150	—	125	—	104	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
t_{COE}	Clock to Output – PIO Output Register	MachXO2-1200ZE	—	11.10	—	11.51	—	11.91	ns
		MachXO2-2000ZE	—	11.10	—	11.51	—	11.91	ns
		MachXO2-4000ZE	—	10.89	—	11.28	—	11.67	ns
		MachXO2-7000ZE	—	11.10	—	11.51	—	11.91	ns
t_{SUE}	Clock to Data Setup – PIO Input Register	MachXO2-1200ZE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-2000ZE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000ZE	–0.15	—	–0.15	—	–0.15	—	ns
		MachXO2-7000ZE	–0.23	—	–0.23	—	–0.23	—	ns
t_{HE}	Clock to Data Hold – PIO Input Register	MachXO2-1200ZE	3.81	—	4.11	—	4.52	—	ns
		MachXO2-2000ZE	3.81	—	4.11	—	4.52	—	ns
		MachXO2-4000ZE	3.60	—	3.89	—	4.28	—	ns
		MachXO2-7000ZE	3.81	—	4.11	—	4.52	—	ns
t_{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200ZE	2.78	—	3.11	—	3.40	—	ns
		MachXO2-2000ZE	2.78	—	3.11	—	3.40	—	ns
		MachXO2-4000ZE	3.11	—	3.48	—	3.79	—	ns
		MachXO2-7000ZE	2.94	—	3.30	—	3.60	—	ns
t_{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200ZE	–0.29	—	-0.29	—	–0.29	—	ns
		MachXO2-2000ZE	–0.29	—	-0.29	—	–0.29	—	ns
		MachXO2-4000ZE	–0.46	—	-0.46	—	–0.46	—	ns
		MachXO2-7000ZE	–0.37	—	-0.37	—	–0.37	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t_{COPLL}	Clock to Output – PIO Output Register	MachXO2-1200ZE	—	7.95	—	8.07	—	8.19	ns
		MachXO2-2000ZE	—	7.97	—	8.10	—	8.22	ns
		MachXO2-4000ZE	—	7.98	—	8.10	—	8.23	ns
		MachXO2-7000ZE	—	8.02	—	8.14	—	8.26	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO2-1200ZE	0.85	—	0.85	—	0.89	—	ns
		MachXO2-2000ZE	0.84	—	0.84	—	0.86	—	ns
		MachXO2-4000ZE	0.84	—	0.84	—	0.85	—	ns
		MachXO2-7000ZE	0.83	—	0.83	—	0.81	—	ns

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HPLL}	Clock to Data Hold – PIO Input Register	MachXO2-1200ZE	0.66	—	0.68	—	0.80	—	ns
		MachXO2-2000ZE	0.68	—	0.70	—	0.83	—	ns
		MachXO2-4000ZE	0.68	—	0.71	—	0.84	—	ns
		MachXO2-7000ZE	0.73	—	0.74	—	0.87	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200ZE	5.14	—	5.69	—	6.20	—	ns
		MachXO2-2000ZE	5.11	—	5.67	—	6.17	—	ns
		MachXO2-4000ZE	5.27	—	5.84	—	6.35	—	ns
		MachXO2-7000ZE	5.15	—	5.71	—	6.23	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200ZE	–1.36	—	–1.36	—	–1.36	—	ns
		MachXO2-2000ZE	–1.35	—	–1.35	—	–1.35	—	ns
		MachXO2-4000ZE	–1.43	—	–1.43	—	–1.43	—	ns
		MachXO2-7000ZE	–1.41	—	–1.41	—	–1.41	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.382	—	0.401	—	0.417	UI
t_{DVE}	Input Data Hold After CLK		0.670	—	0.684	—	0.693	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	All MachXO2 devices, all sides	1.319	—	1.412	—	1.462	—	ns
t_{HO}	Input Data Hold After CLK		0.717	—	1.010	—	1.340	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.361	—	0.346	—	0.334	UI
t_{DVE}	Input Data Hold After CLK		0.602	—	0.625	—	0.648	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.472	—	0.672	—	0.865	—	ns
t_{HO}	Input Data Hold After CLK		0.363	—	0.501	—	0.743	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input - GDDRX4_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.307	—	0.316	—	0.326	UI
t_{DVE}	Input Data Hold After ECLK		0.662	—	0.650	—	0.649	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.434	—	0.535	—	0.630	—	ns
t_{HO}	Input Data Hold After ECLK		0.385	—	0.395	—	0.463	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz
7:1 LVDS Inputs – GDDR71_RX.ECLK.7.1[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.307	—	0.316	—	0.326	UI
t_{DVE}	Input Data Hold After ECLK		0.662	—	0.650	—	0.649	—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	210	—	176	—	146	MHz
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	60	—	50	—	42	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	All MachXO2 devices, all sides	—	0.850	—	0.910	—	0.970	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.850	—	0.910	—	0.970	ns
f_{DATA}	DDRX1 Output Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK frequency		—	70	—	58	—	49	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	All MachXO2 devices, all sides	2.720	—	3.380	—	4.140	—	ns
t_{DVA}	Output Data Valid After CLK Output		2.720	—	3.380	—	4.140	—	ns
f_{DATA}	DDRX1 Output Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		—	70	—	58	—	49	MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	—	0.270	—	0.300	—	0.330	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.270	—	0.300	—	0.330	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	1.445	—	1.760	—	2.140	—	ns
t_{DVA}	Output Data Valid After CLK Output		1.445	—	1.760	—	2.140	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	—	0.270	—	0.300	—	0.330	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.270	—	0.300	—	0.330	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	0.873	—	1.067	—	1.319	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.873	—	1.067	—	1.319	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[9, 12]									
t_{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.240	—	0.270	—	0.300	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.240	—	0.270	—	0.300	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	420	—	352	—	292	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	210	—	176	—	146	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	60	—	50	—	42	MHz

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.349	—	0.381	—	0.396	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.630	—	0.613	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM LPDDR Serial Data Speed		—	120	—	110	—	96	Mbps
f_{SCLK}	SCLK Frequency		—	60	—	55	—	48	MHz
f_{LPDDR}	LPDDR Data Transfer Rate		0	120	0	110	0	96	Mbps
DDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.347	—	0.374	—	0.393	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.637	—	0.616	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f_{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f_{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps
DDR2[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.372	—	0.394	—	0.410	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.690	—	0.658	—	0.618	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f_{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f_{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
7. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 167 ps (–3), 182 ps (–2), 195 ps (–1).
8. This number for general purpose usage. Duty cycle tolerance is +/–10%.
9. Duty cycle is +/– 5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

Figure 3-5. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms

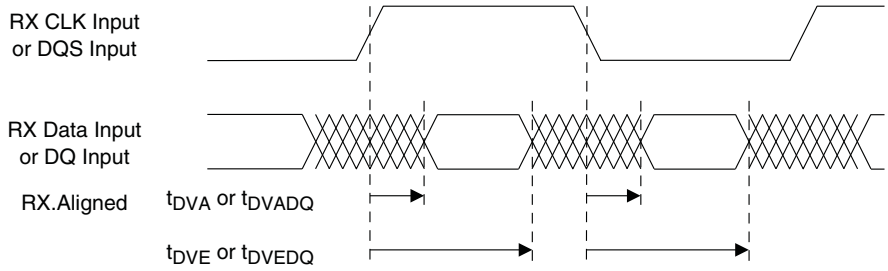


Figure 3-6. Receiver RX.CLK.Centered Waveforms

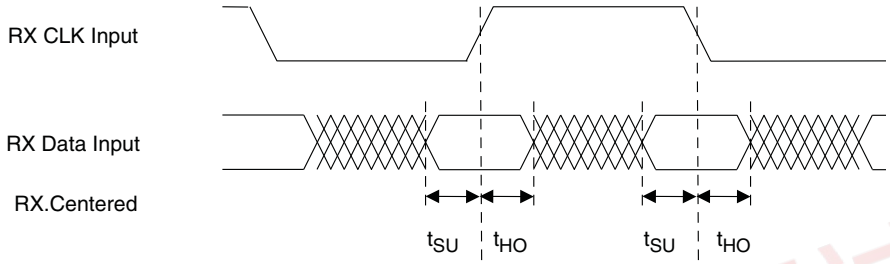


Figure 3-7. Transmitter TX.CLK.Aligned Waveforms

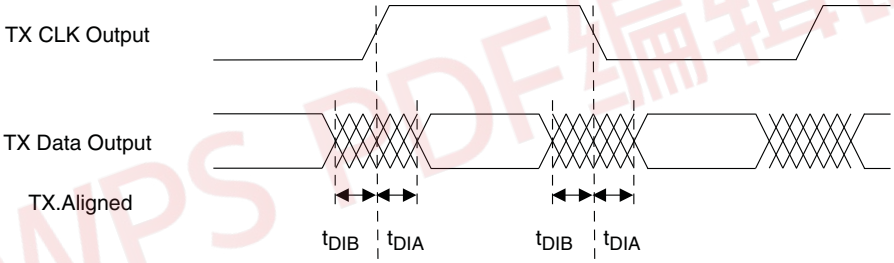


Figure 3-8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms

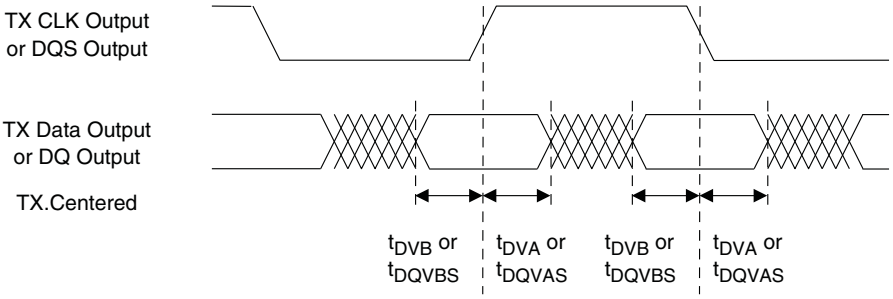


Figure 3-9. GDDR71 Video Timing Waveforms

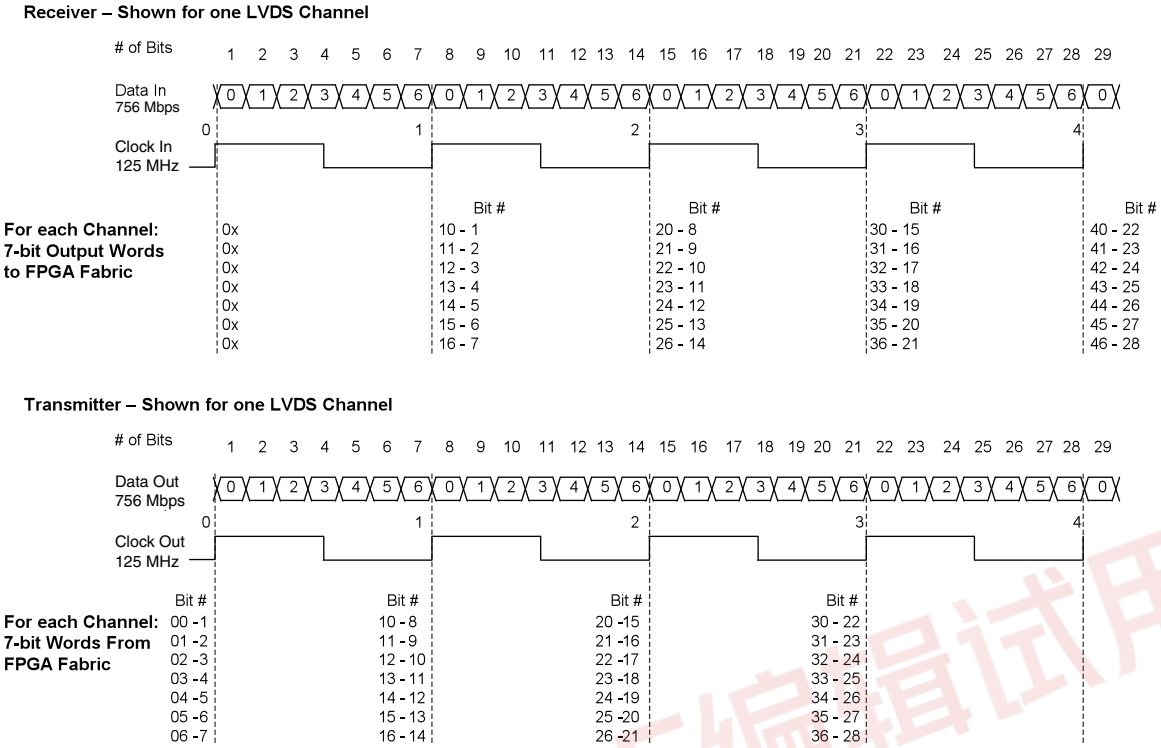


Figure 3-10. Receiver GDDR71_RX. Waveforms

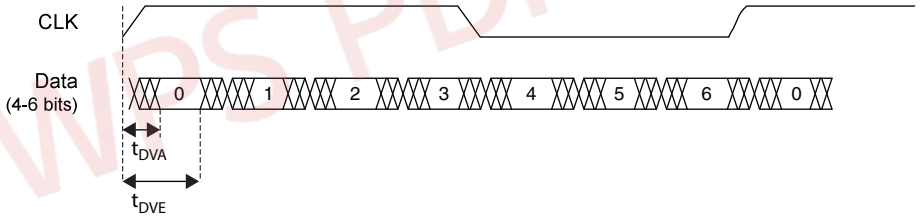
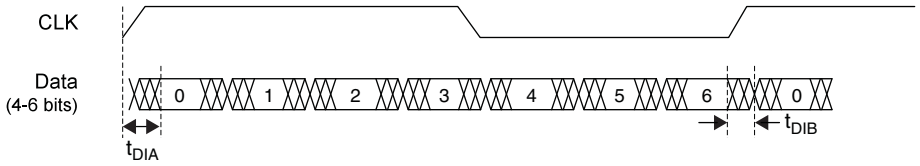


Figure 3-11. Transmitter GDDR71_TX. Waveforms



sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)		1.5625	400	MHz
f_{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f_{VCO}	PLL VCO Frequency		200	800	MHz
f_{PFD}	Phase Detector Input Frequency		7	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Without duty trim selected[3]	45	55	%
t_{DT_TRIM}[7]	Edge Duty Trim Accuracy		–75	75	%
t_{PH}[4]	Output Phase Accuracy		–6	6	%
t_{OPJIT}[1, 8]	Output Clock Period Jitter	f_{OUT} > 100 MHz	—	150	ps p-p
		f_{OUT} < 100 MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} > 100 MHz	—	180	ps p-p
		f_{OUT} < 100 MHz	—	0.009	UIPP
	Output Clock Phase Jitter	f_{PFD} > 100 MHz	—	160	ps p-p
		f_{PFD} < 100 MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	230	ps p-p
		f_{OUT} < 100 MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	230	ps p-p
		f_{OUT} < 100 MHz	—	0.12	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	–120	120	ps
t_W	Output Clock Pulse Width	At 90% or 10%[3]	0.9	—	ns
t_{LOCK}[2, 5]	PLL Lock-in Time		—	15	ms
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[6]	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{STABLE}[5]	STANDBY High to PLL Stable		—	15	ms
t_{RST}	RST/RESETM Pulse Width		1	—	ns
t_{RSTREC}	RST Recovery Time		1	—	ns
t_{RST_DIV}	RESETC/D Pulse Width		10	—	ns
t_{RSTREC_DIV}	RESETC/D Recovery Time		1	—	ns
$t_{ROTATE-SETUP}$	PHASESTEP Setup Time		10	—	ns

sysCLOCK PLL Timing (Continued)

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
t_{ROTATE_WD}	PHASESTEP Pulse Width		4	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide for more details.
5. At minimum $f_{PFD.}$ As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

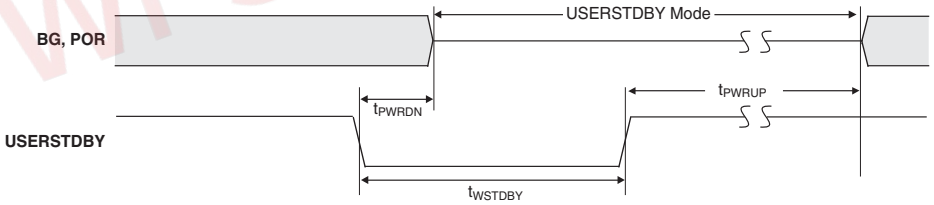
MachXO2 Oscillator Output Frequency

Symbol	Parameter	Min.	Typ.	Max	Units
f_{MAX}	Oscillator Output Frequency (Commercial Grade Devices, 0 to 85°C)	125.685	133	140.315	MHz
	Oscillator Output Frequency (Industrial Grade Devices, –40 °C to 100 °C)	124.355	133	141.645	MHz
t_{DT}	Output Clock Duty Cycle	43	50	57	%
t_{OPJIT}[1]	Output Clock Period Jitter	0.01	0.012	0.02	UIPP
$t_{STABLEOSC}$	STDBY Low to Oscillator Stable	0.01	0.05	0.1	µs

1. Output Clock Period Jitter specified at 133 MHz. The values for lower frequencies will be smaller UIPP. The typical value for 133 MHz is 95 ps and for 2.08 MHz the typical value is 1.54 ns.

MachXO2 Standby Mode Timing – HC/HE Devices

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	USERSTDBY High to Stop	All	—	—	9	ns
t_{PWRUP}	USERSTDBY Low to Power Up	LCMXO2-256		—		µs
		LCMXO2-640		—		µs
		LCMXO2-640U		—		µs
		LCMXO2-1200	20	—	50	µs
		LCMXO2-1200U		—		µs
		LCMXO2-2000		—		µs
		LCMXO2-2000U		—		µs
		LCMXO2-4000		—		µs
		LCMXO2-7000		—		µs
t_{WSTDBY}	USERSTDBY Pulse Width	All	18	—	—	ns



MachXO2 Standby Mode Timing – ZE Devices

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	USERSTDBY High to Stop	All	—	—	13	ns
t_{PWRUP}	USERSTDBY Low to Power Up	LCMXO2-256		—		µs
		LCMXO2-640		—		µs
		LCMXO2-1200	20	—	50	µs
		LCMXO2-2000		—		µs
		LCMXO2-4000		—		µs
		LCMXO2-7000		—		µs
t_{WSTDBY}	USERSTDBY Pulse Width	All	19	—	—	ns
$t_{BNDGAPSTBL}$	USERSTDBY High to Bandgap Stable	All	—	—	15	ns

Flash Download Time[1, 2]

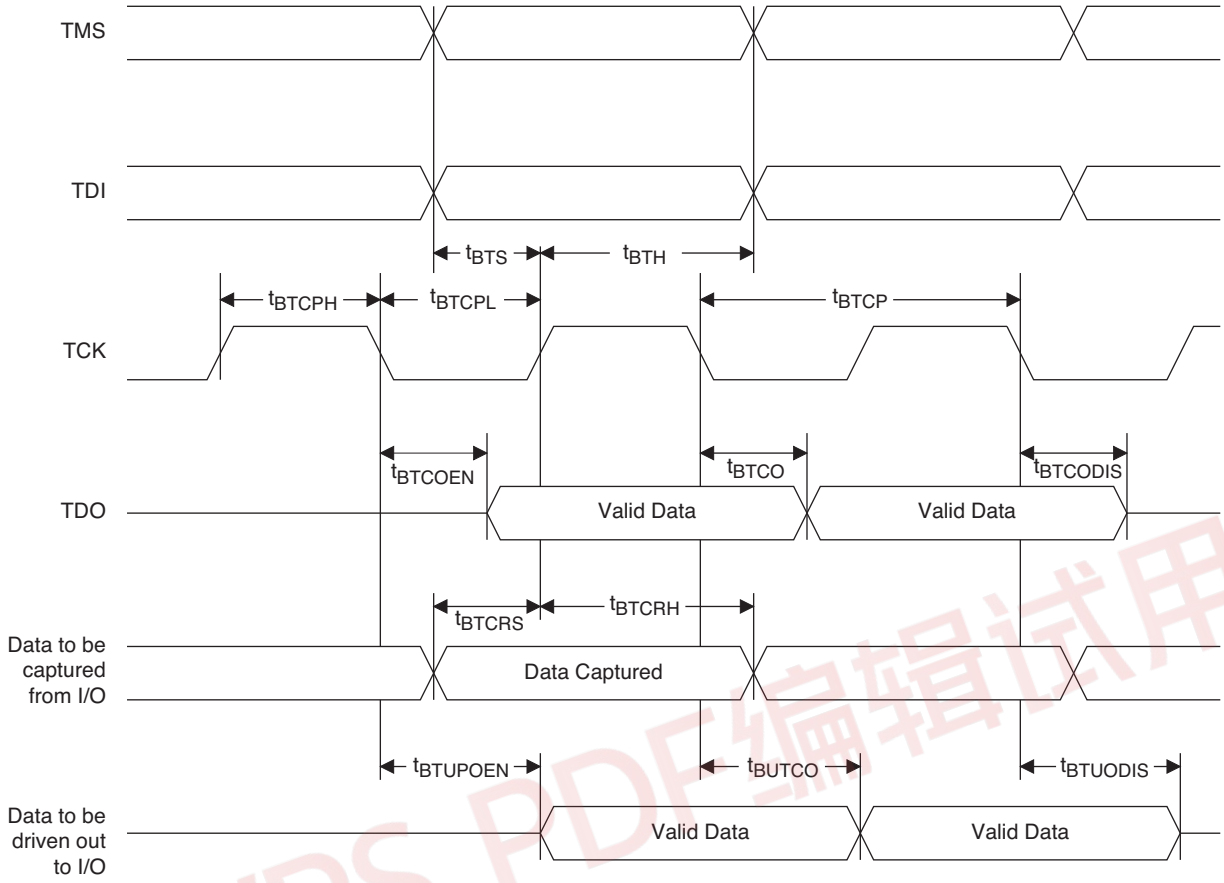
Symbol	Parameter	Device	Typ.	Units
$t_{REFRESH}$	POR to Device I/O Active	LCMXO2-256	0.6	ms
		LCMXO2-640	1.0	ms
		LCMXO2-640U	1.9	ms
		LCMXO2-1200	1.9	ms
		LCMXO2-1200U	1.4	ms
		LCMXO2-2000	1.4	ms
		LCMXO2-2000U	2.4	ms
		LCMXO2-4000	2.4	ms
		LCMXO2-7000	3.8	ms

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.
2. The Flash download time is measured starting from the maximum voltage of POR trip point.

JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	20	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-12. JTAG Port Timing Waveforms



sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Modes					
t_{PRGM}	PROGRAMN low pulse accept		55	—	ns
t_{PRGMJ}	PROGRAMN low pulse rejection		—	25	ns
t_{INITL}	INITN low time	LCMXO2-256	—	30	µs
		LCMXO2-640	—	35	µs
		LCMXO2-640U/ LCMXO2-1200	—	55	µs
		LCMXO2-1200U/ LCMXO2-2000	—	70	µs
		LCMXO2-2000U/ LCMXO2-4000	—	105	µs
		LCMXO2-7000	—	130	µs
$t_{DPPINIT}$	PROGRAMN low to INITN low		—	150	ns
$t_{DPPDONE}$	PROGRAMN low to DONE low		—	150	ns
t_{IODISS}	PROGRAMN low to I/O disable		—	120	ns
Slave SPI					
f_{MAX}	CCLK clock frequency		—	66	MHz
t_{CCLKH}	CCLK clock pulse width high		7.5	—	ns
t_{CCLKL}	CCLK clock pulse width low		7.5	—	ns
t_{STSU}	CCLK setup time		2	—	ns
t_{STH}	CCLK hold time		0	—	ns
t_{STCO}	CCLK falling edge to valid output		—	10	ns
t_{STOZ}	CCLK falling edge to valid disable		—	10	ns
t_{STOV}	CCLK falling edge to valid enable		—	10	ns
t_{SCS}	Chip select high time		25	—	ns
t_{SCSS}	Chip select setup time		3	—	ns
t_{SCSH}	Chip select hold time		3	—	ns
Master SPI					
f_{MAX}	MCLK clock frequency		—	133	MHz
t_{MCLKH}	MCLK clock pulse width high		3.75	—	ns
t_{MCLKL}	MCLK clock pulse width low		3.75	—	ns
t_{STSU}	MCLK setup time		5	—	ns
t_{STH}	MCLK hold time		1	—	ns
t_{CSSPI}	INITN high to chip select low		100	200	ns
t_{MCLK}	INITN high to first MCLK edge		0.75	1	µs

I²C Port Timing Specifications[1, 2]

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCL clock frequency	—	400	kHz

1. MachXO2 supports the following modes:
   • Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
   • Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
2. Refer to the I²C specification for timing requirements.

SPI Port Timing Specifications[1]

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCK clock frequency	—	45	MHz

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

Switching Test Conditions

Figure 3-13 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-5.

Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards

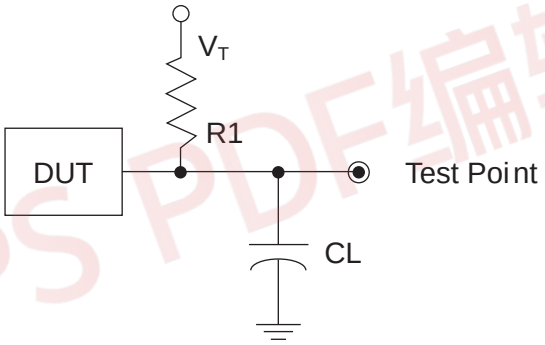


Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R1	CL	Timing Ref.	VT
LVTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5 V	V_{OL}
LVTTL and LVCMOS 3.3 (Z -> L)			1.5 V	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVTTL + LVCMOS (H -> Z)			V_{OH} – 0.15 V	V_{OL}
LVTTL + LVCMOS (L -> Z)			V_{OL} – 0.15 V	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the group to which the pad is connected. Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic. During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.
NC	—	No connect.
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together. For QFN 48 package, the exposed die pad is the device ground.
VCC	—	V_{CC} – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIOx	—	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.
PLL and Clock Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)		
[LOC]_GPLL[T, C]_IN	—	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.
Test and Programming (Dual function pins used for test access port and during sysCONFIG™)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
JTAGENB	I	Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then: If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O. If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.
Configuration (Dual function pins used during sysCONFIG)		
PROGRAMN	I	Initiates configuration sequence when asserted low. During configuration, or when reserved as PROGRAMN in user mode, this pin always has an active pull-up.

Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, or when reserved as INITn in user mode, this pin has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress. During configuration, or when reserved as DONE in user mode, this pin has an active pull-up.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.
SCL	I/O	Slave I^2C clock input and master I^2C clock output.
SDA	I/O	Slave I^2C data input and master I^2C data output.

Pinout Information Summary

	MachXO2-256					MachXO2-640			MachXO2-640U
	32 QFN[1]	48 QFN[3]	64 ucBGA	100 TQFP	132 csBGA	48 QFN[3]	100 TQFP	132 csBGA	144 TQFP
General Purpose I/O per Bank									
Bank 0	8	10	9	13	13	10	18	19	27
Bank 1	2	10	12	14	14	10	20	20	26
Bank 2	9	10	11	14	14	10	20	20	28
Bank 3	2	10	12	14	14	10	20	20	26
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Single Ended I/O	21	40	44	55	55	40	78	79	107
Differential I/O per Bank									
Bank 0	4	5	5	7	7	5	9	10	14
Bank 1	1	5	6	7	7	5	10	10	13
Bank 2	4	5	5	7	7	5	10	10	14
Bank 3	1	5	6	7	7	5	10	10	13
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Differential I/O	10	20	22	28	28	20	39	40	54
Dual Function I/O	22	25	27	29	29	25	29	29	33
High-speed Differential I/O									
Bank 0	0	0	0	0	0	0	0	0	7
Gearboxes									
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	0	0	0	0	0	0	0	0	7
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	0	0	0	0	0	0	0	0	7
DQS Groups									
Bank 1	0	0	0	0	0	0	0	0	2
VCCIO Pins									
Bank 0	2	2	2	2	2	2	2	2	3
Bank 1	1	1	2	2	2	1	2	2	3
Bank 2	2	2	2	2	2	2	2	2	3
Bank 3	1	1	2	2	2	1	2	2	3
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
VCC	2	2	2	2	2	2	2	2	4
GND[2]	2	1	8	8	8	1	8	10	12
NC	0	0	1	26	58	0	3	32	8
Reserved for Configuration	1	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	32	49	64	100	132	49	100	132	144

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.
2. For 48 QFN package, exposed die pad is the device ground.
3. 48-pin QFN information is 'Advanced'.

	MachXO2-1200					MachXO2-1200U
	100 TQFP	132 csBGA	144 TQFP	25 WLCSP	32 QFN[1]	256 ftBGA
General Purpose I/O per Bank						
Bank 0	18	25	27	11	9	50
Bank 1	21	26	26	0	2	52
Bank 2	20	28	28	7	9	52
Bank 3	20	25	26	0	2	16
Bank 4	0	0	0	0	0	16
Bank 5	0	0	0	0	0	20
Total General Purpose Single Ended I/O	79	104	107	18	22	206
Differential I/O per Bank						
Bank 0	9	13	14	5	4	25
Bank 1	10	13	13	0	1	26
Bank 2	10	14	14	2	4	26
Bank 3	10	12	13	0	1	8
Bank 4	0	0	0	0	0	8
Bank 5	0	0	0	0	0	10
Total General Purpose Differential I/O	39	52	54	7	10	103
Dual Function I/O	31	33	33	18	22	33
High-speed Differential I/O						
Bank 0	4	7	7	0	0	14
Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	4	7	7	0	0	14
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	5	7	7	0	2	14
DQS Groups						
Bank 1	1	2	2	0	0	2
VCCIO Pins						
Bank 0	2	3	3	1	2	4
Bank 1	2	3	3	0	1	4
Bank 2	2	3	3	1	2	4
Bank 3	3	3	3	0	1	1
Bank 4	0	0	0	0	0	2
Bank 5	0	0	0	0	0	1
VCC	2	4	4	2	2	8
GND	8	10	12	2	2	24
NC	1	1	8	0	0	1
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	100	132	144	25	32	256

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.

	MachXO2-2000						MachXO2-2000U
	49 WLCSP	100 TQFP	132 csBGA	144 TQFP	256 caBGA	256 ftBGA	484 ftBGA
General Purpose I/O per Bank							
Bank 0	19	18	25	27	50	50	70
Bank 1	0	21	26	28	52	52	68
Bank 2	13	20	28	28	52	52	72
Bank 3	0	6	7	8	16	16	24
Bank 4	0	6	8	10	16	16	16
Bank 5	6	8	10	10	20	20	28
Total General Purpose Single-Ended I/O	38	79	104	111	206	206	278
Differential I/O per Bank							
Bank 0	7	9	13	14	25	25	35
Bank 1	0	10	13	14	26	26	34
Bank 2	6	10	14	14	26	26	36
Bank 3	0	3	3	4	8	8	12
Bank 4	0	3	4	5	8	8	8
Bank 5	3	4	5	5	10	10	14
Total General Purpose Differential I/O	16	39	52	56	103	103	139
Dual Function I/O	24	31	33	33	33	33	37
High-speed Differential I/O							
Bank 0	5	4	8	9	14	14	18
Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	4	8	9	14	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	10	14	14	14	14	18
DQS Groups							
Bank 1	0	1	2	2	2	2	2
VCCIO Pins							
Bank 0	2	2	3	3	4	4	10
Bank 1	0	2	3	3	4	4	10
Bank 2	1	2	3	3	4	4	10
Bank 3	0	1	1	1	1	1	3
Bank 4	0	1	1	1	2	2	4
Bank 5	1	1	1	1	1	1	3
VCC	2	2	4	4	8	8	12
GND	4	8	10	12	24	24	48
NC	0	1	1	4	1	1	105
Reserved for Configuration	1	1	1	1	v	1	1
Total Count of Bonded Pins	39	100	132	144	256	256	484

	MachXO2-4000							
	84 QFN	132 csBGA	144 TQFP	184 csBGA	256 caBGA	256 ftBGA	332 caBGA	484 fpBGA
General Purpose I/O per Bank								
Bank 0	27	25	27	37	50	50	68	70
Bank 1	10	26	29	37	52	52	68	68
Bank 2	22	28	29	39	52	52	70	72
Bank 3	0	7	9	10	16	16	24	24
Bank 4	9	8	10	12	16	16	16	16
Bank 5	0	10	10	15	20	20	28	28
Total General Purpose Single Ended I/O	68	104	114	150	206	206	274	278
Differential I/O per Bank								
Bank 0	13	13	14	18	25	25	34	35
Bank 1	4	13	14	18	26	26	34	34
Bank 2	11	14	14	19	26	26	35	36
Bank 3	0	3	4	4	8	8	12	12
Bank 4	4	4	5	6	8	8	8	8
Bank 5	0	5	5	7	10	10	14	14
Total General Purpose Differential I/O	32	52	56	72	103	103	137	139
Dual Function I/O	28	37	37	37	37	37	37	37
High-speed Differential I/O								
Bank 0	8	8	9	8	18	18	18	18
Gearboxes								
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	8	8	9	9	18	18	18	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	11	14	14	12	18	18	18	18
DQS Groups								
Bank 1	1	2	2	2	2	2	2	2
VCCIO Pins								
Bank 0	3	3	3	3	4	4	4	10
Bank 1	1	3	3	3	4	4	4	10
Bank 2	2	3	3	3	4	4	4	10
Bank 3	1	1	1	1	1	1	2	3
Bank 4	1	1	1	1	2	2	1	4
Bank 5	1	1	1	1	1	1	2	3
VCC	4	4	4	4	8	8	8	12
GND	4	10	12	16	24	24	27	48
NC	1	1	1	1	1	1	5	105
Reserved for configuration	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	84	132	144	184	256	256	332	484

	MachXO2-7000					
	144 TQFP	**256 caBGA**	**256 ftBGA**	**332 caBGA**	**400 caBGA**	**484 fpBGA**
General Purpose I/O per Bank						
Bank 0	27	50	50	68	83	82
Bank 1	29	52	52	70	84	84
Bank 2	29	52	52	70	84	84
Bank 3	9	16	16	24	28	28
Bank 4	10	16	16	16	24	24
Bank 5	10	20	20	30	32	32
Total General Purpose Single Ended I/O	114	206	206	278	335	334
Differential I/O per Bank						
Bank 0	14	25	25	34	42	41
Bank 1	14	26	26	35	42	42
Bank 2	14	26	26	35	42	42
Bank 3	4	8	8	12	14	14
Bank 4	5	8	8	8	12	12
Bank 5	5	10	10	15	16	16
Total General Purpose Differential I/O	56	103	103	139	168	167
Dual Function I/O	37	37	37	37	37	37
High-speed Differential I/O						
Bank 0	9	20	20	21	21	21
Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	9	20	20	21	21	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	14	20	20	21	21	21
DQS Groups						
Bank 1	2	2	2	2	2	2
VCCIO Pins						
Bank 0	3	4	4	4	5	10
Bank 1	3	4	4	4	5	10
Bank 2	3	4	4	4	5	10
Bank 3	1	1	1	2	2	3
Bank 4	1	2	2	1	2	4
Bank 5	1	1	1	2	2	3
VCC	4	8	8	8	10	12
GND	12	24	24	27	33	48
NC	1	1	1	1	0	49
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	144	256	256	332	400	484

For Further Information

For further information regarding logic signal connections for various packages please refer to the MachXO2 Device Pinout Files.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Users must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1198, Power Estimation and Management for MachXO2 Devices
- The Power Calculator tool is included with the Lattice design tools, or as a standalone download from www.latticesemi.com/software

MachXO2 Family Data Sheet Ordering Information

March 2017 Data Sheet DS1035

MachXO2 Part Number Description

LCMXO2 – XXXX X X X – X XXXXXX X XX XX

Device Family
MachXO2 PLD

Logic Capacity
256 = 256 LUTs
640 = 640 LUTs
1200 = 1280 LUTs
2000 = 2112 LUTs
4000 = 4320 LUTs
7000 = 6864 LUTs

I/O Count
Blank = Standard Device
U = Ultra High I/O Device

Power/Performance
Z = Low Power
H = High Performance

Supply Voltage
C = 2.5 V / 3.3 V
E = 1.2 V

Speed
1 = Slowest
2
3 = Fastest
} Low Power

4 = Slowest
5
6 = Fastest
} High Performance

Device Status
Blank = Production Device
ES = Engineering Sample
R1 = Production Release 1 Device
1K = WLCSP Package, 1,000 parts per reel

Shipping Method
Blank = Trays
TR = Tape and Reel

Grade
C = Commercial
I = Industrial

Package
UWG25 = 25-Ball Halogen-Free WLCSP (0.4 mm Pitch)
SG32 = 32-Pin Halogen-Free QFN (0.5 mm Pitch)
SG48 = 48-Pin Halogen-Free QFN (0.5 mm Pitch)
UWG49 = 49-ball Halogen-Free WLCSP (0.4 mm Pitch)
UMG64 = 64-Ball Halogen-Free ucBGA (0.4 mm Pitch)
QN84 = 84-Pin Halogen-Free QFN (0.5 mm Pitch)
TG100 = 100-Pin Halogen-Free TQFP
TG144 = 144-Pin Halogen-Free TQFP
MG132 = 132-Ball Halogen-Free csBGA (0.5 mm Pitch)
MG184 = 184-Ball Halogen-Free csBGA (0.5 mm Pitch)
BG256 = 256-Ball Halogen-Free caBGA (0.8 mm Pitch)
FTG256 = 256-Ball Halogen-Free ftBGA (1.0 mm Pitch)
BG332 = 332-Ball Halogen-Free caBGA (0.8 mm Pitch)
FG484 = 484-Ball Halogen-Free fpBGA (1.0 mm Pitch)

* 48-pin QFN information is 'Advanced'.

Ordering Information

MachXO2 devices have top-side markings, for commercial and industrial grades, as shown below:

Notes:

1. Markings are abbreviated for small packages.

2. See PCN 05A-12 for information regarding a change to the top-side mark logo.

Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32C	256	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-256ZE-2SG32C	256	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-256ZE-3SG32C	256	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-256ZE-1UMG64C	256	1.2 V	–1	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-2UMG64C	256	1.2 V	–2	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-3UMG64C	256	1.2 V	–3	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-1TG100C	256	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-2TG100C	256	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-3TG100C	256	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-1MG132C	256	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-2MG132C	256	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-3MG132C	256	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100C	640	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-2TG100C	640	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-3TG100C	640	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-1MG132C	640	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-2MG132C	640	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-3MG132C	640	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1SG32C	1280	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-2SG32C	1280	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-3SG32C	1280	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-1TG100C	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100C	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100C	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132C	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132C	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132C	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144C	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144C	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144C	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1TG100C	2112	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-2TG100C	2112	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-3TG100C	2112	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-1MG132C	2112	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-2MG132C	2112	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-3MG132C	2112	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-1TG144C	2112	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-2TG144C	2112	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-3TG144C	2112	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-1BG256C	2112	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-2BG256C	2112	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-3BG256C	2112	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-1FTG256C	2112	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-2000ZE-2FTG256C	2112	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-2000ZE-3FTG256C	2112	1.2 V	–3	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000ZE-1QN84C	4320	1.2 V	–1	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-2QN84C	4320	1.2 V	–2	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-3QN84C	4320	1.2 V	–3	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-1MG132C	4320	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-2MG132C	4320	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-3MG132C	4320	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-1TG144C	4320	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-2TG144C	4320	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-3TG144C	4320	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-1BG256C	4320	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-2BG256C	4320	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-3BG256C	4320	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-1FTG256C	4320	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-2FTG256C	4320	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-3FTG256C	4320	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-1BG332C	4320	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-2BG332C	4320	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-3BG332C	4320	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-1FG484C	4320	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-4000ZE-2FG484C	4320	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-4000ZE-3FG484C	4320	1.2 V	–3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144C	6864	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-2TG144C	6864	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-3TG144C	6864	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-1BG256C	6864	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-2BG256C	6864	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-3BG256C	6864	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-1FTG256C	6864	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-2FTG256C	6864	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-3FTG256C	6864	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-1BG332C	6864	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-2BG332C	6864	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-3BG332C	6864	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-1FG484C	6864	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-2FG484C	6864	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-3FG484C	6864	1.2 V	–3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100CR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100CR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100CR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132CR1[1]	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132CR1[1]	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132CR1[1]	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144CR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144CR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144CR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200ZE-speed package CR1” are the same as the “LCMXO2-1200ZE-speed package C” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32C	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	COM
LCMXO2-256HC-5SG32C	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	COM
LCMXO2-256HC-6SG32C	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	COM
LCMXO2-256HC-4SG48C	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	COM
LCMXO2-256HC-5SG48C	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	COM
LCMXO2-256HC-6SG48C	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	COM
LCMXO2-256HC-4UMG64C	256	2.5 V / 3.3 V	–4	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-5UMG64C	256	2.5 V / 3.3 V	–5	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-6UMG64C	256	2.5 V / 3.3 V	–6	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-4TG100C	256	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-256HC-5TG100C	256	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-256HC-6TG100C	256	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-256HC-4MG132C	256	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-256HC-5MG132C	256	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-256HC-6MG132C	256	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48C	640	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	COM
LCMXO2-640HC-5SG48C	640	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	COM
LCMXO2-640HC-6SG48C	640	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	COM
LCMXO2-640HC-4TG100C	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-640HC-5TG100C	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-640HC-6TG100C	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-640HC-4MG132C	640	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-640HC-5MG132C	640	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-640HC-6MG132C	640	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144C	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-5TG144C	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-6TG144C	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32C	1280	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	COM
LCMXO2-1200HC-5SG32C	1280	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	COM
LCMXO2-1200HC-6SG32C	1280	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	COM
LCMXO2-1200HC-4TG100C	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100C	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100C	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132C	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132C	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132C	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144C	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144C	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144C	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256C	1280	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-1200UHC-5FTG256C	1280	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-1200UHC-6FTG256C	1280	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100C	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-5TG100C	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-6TG100C	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-4MG132C	2112	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-5MG132C	2112	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-6MG132C	2112	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-4TG144C	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-5TG144C	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-6TG144C	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-4BG256C	2112	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-5BG256C	2112	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-6BG256C	2112	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-4FTG256C	2112	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HC-5FTG256C	2112	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HC-6FTG256C	2112	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484C	2112	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-5FG484C	2112	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-6FG484C	2112	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84C	4320	2.5 V / 3.3 V	–4	Halogen-Free QFN	84	COM
LCMXO2-4000HC-5QN84C	4320	2.5 V / 3.3 V	–5	Halogen-Free QFN	84	COM
LCMXO2-4000HC-6QN84C	4320	2.5 V / 3.3 V	–6	Halogen-Free QFN	84	COM
LCMXO2-4000HC-4MG132C	4320	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-5MG132C	4320	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-6MG132C	4320	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-4TG144C	4320	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-5TG144C	4320	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-6TG144C	4320	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-4BG256C	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-5BG256C	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-6BG256C	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-4FTG256C	4320	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-5FTG256C	4320	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-6FTG256C	4320	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-4BG332C	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-5BG332C	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-6BG332C	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-4FG484C	4320	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-5FG484C	4320	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-6FG484C	4320	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144C	6864	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-5TG144C	6864	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-6TG144C	6864	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-4BG256C	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-5BG256C	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-6BG256C	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-4FTG256C	6864	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-5FTG256C	6864	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-6FTG256C	6864	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-4BG332C	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-5BG332C	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-6BG332C	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-4FG400C	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-5FG400C	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-6FG400C	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-4FG484C	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-5FG484C	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-6FG484C	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100CR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100CR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100CR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132CR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132CR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132CR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144CR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144CR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144CR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200HC-speed package CR1” are the same as the “LCMXO2-1200HC-speed package C” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100C	2112	1.2 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-5TG100C	2112	1.2 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-6TG100C	2112	1.2 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-4TG144C	2112	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-5TG144C	2112	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-6TG144C	2112	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-4MG132C	2112	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-5MG132C	2112	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-6MG132C	2112	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-4BG256C	2112	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-5BG256C	2112	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-6BG256C	2112	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-4FTG256C	2112	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-5FTG256C	2112	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-6FTG256C	2112	1.2 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484C	2112	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-5FG484C	2112	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-6FG484C	2112	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4TG144C	4320	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-5TG144C	4320	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-6TG144C	4320	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-4MG132C	4320	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-5MG132C	4320	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-6MG132C	4320	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-4BG256C	4320	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4MG184C	4320	1.2 V	–4	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5MG184C	4320	1.2 V	–5	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-6MG184C	4320	1.2 V	–6	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5BG256C	4320	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-6BG256C	4320	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4FTG256C	4320	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-5FTG256C	4320	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-6FTG256C	4320	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-4BG332C	4320	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-5BG332C	4320	1.2 V	–5	Halogen-Free caBGA	332	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-6BG332C	4320	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-4FG484C	4320	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-5FG484C	4320	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-6FG484C	4320	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144C	6864	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-5TG144C	6864	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-6TG144C	6864	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-4BG256C	6864	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-5BG256C	6864	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-6BG256C	6864	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-4FTG256C	6864	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-5FTG256C	6864	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-6FTG256C	6864	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-4BG332C	6864	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-5BG332C	6864	1.2 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-6BG332C	6864	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-4FG484C	6864	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-5FG484C	6864	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-6FG484C	6864	1.2 V	–6	Halogen-Free fpBGA	484	COM

Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32I	256	1.2 V	–1	Halogen-Free QFN	32	IND
LCMXO2-256ZE-2SG32I	256	1.2 V	–2	Halogen-Free QFN	32	IND
LCMXO2-256ZE-3SG32I	256	1.2 V	–3	Halogen-Free QFN	32	IND
LCMXO2-256ZE-1UMG64I	256	1.2 V	–1	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-2UMG64I	256	1.2 V	–2	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-3UMG64I	256	1.2 V	–3	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-1TG100I	256	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-2TG100I	256	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-3TG100I	256	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-1MG132I	256	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-2MG132I	256	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-3MG132I	256	1.2 V	–3	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100I	640	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-2TG100I	640	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-3TG100I	640	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-1MG132I	640	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-2MG132I	640	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-3MG132I	640	1.2 V	–3	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1UWG25ITR[1]	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR50[3]	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR1K[2]	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1SG32I	1280	1.2 V	–1	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-2SG32I	1280	1.2 V	–2	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-3SG32I	1280	1.2 V	–3	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-1TG100I	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100I	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100I	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132I	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132I	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132I	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144I	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144I	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144I	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1UWG49ITR[1]	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR50[3]	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR1K[2]	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1TG100I	2112	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-2TG100I	2112	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-3TG100I	2112	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-1MG132I	2112	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-2MG132I	2112	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-3MG132I	2112	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-1TG144I	2112	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-2TG144I	2112	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-3TG144I	2112	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-1BG256I	2112	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-2BG256I	2112	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-3BG256I	2112	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-1FTG256I	2112	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-2FTG256I	2112	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-3FTG256I	2112	1.2 V	–3	Halogen-Free ftBGA	256	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000ZE-1QN84I	4320	1.2 V	–1	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-2QN84I	4320	1.2 V	–2	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-3QN84I	4320	1.2 V	–3	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-1MG132I	4320	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-2MG132I	4320	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-3MG132I	4320	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-1TG144I	4320	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-2TG144I	4320	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-3TG144I	4320	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-1BG256I	4320	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-2BG256I	4320	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-3BG256I	4320	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-1FTG256I	4320	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-2FTG256I	4320	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-3FTG256I	4320	1.2 V	–3	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-1BG332I	4320	1.2 V	–1	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-2BG332I	4320	1.2 V	–2	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-3BG332I	4320	1.2 V	–3	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-1FG484I	4320	1.2 V	–1	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-2FG484I	4320	1.2 V	–2	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-3FG484I	4320	1.2 V	–3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144I	6864	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-2TG144I	6864	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-3TG144I	6864	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-1BG256I	6864	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-2BG256I	6864	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-3BG256I	6864	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-1FTG256I	6864	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-2FTG256I	6864	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-3FTG256I	6864	1.2 V	–3	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-1BG332I	6864	1.2 V	–1	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-2BG332I	6864	1.2 V	–2	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-3BG332I	6864	1.2 V	–3	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-1FG484I	6864	1.2 V	–1	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-2FG484I	6864	1.2 V	–2	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-3FG484I	6864	1.2 V	–3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100IR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100IR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100IR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132IR1[1]	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132IR1[1]	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132IR1[1]	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144IR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144IR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144IR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200ZE-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32I	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	IND
LCMXO2-256HC-5SG32I	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	IND
LCMXO2-256HC-6SG32I	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	IND
LCMXO2-256HC-4SG48I	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	IND
LCMXO2-256HC-5SG48I	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	IND
LCMXO2-256HC-6SG48I	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	IND
LCMXO2-256HC-4UMG64I	256	2.5 V / 3.3 V	–4	Halogen-Free ucBGA	64	IND
LCMXO2-256HC-5UMG64I	256	2.5 V / 3.3 V	–5	Halogen-Free ucBGA	64	IND
LCMXO2-256HC-6UMG64I	256	2.5 V / 3.3 V	–6	Halogen-Free ucBGA	64	IND
LCMXO2-256HC-4TG100I	256	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-256HC-5TG100I	256	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-256HC-6TG100I	256	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-256HC-4MG132I	256	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-256HC-5MG132I	256	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-256HC-6MG132I	256	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48I	640	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	IND
LCMXO2-640HC-5SG48I	640	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	IND
LCMXO2-640HC-6SG48I	640	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	IND
LCMXO2-640HC-4TG100I	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-640HC-5TG100I	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-640HC-6TG100I	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-640HC-4MG132I	640	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-640HC-5MG132I	640	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-640HC-6MG132I	640	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144I	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-640UHC-5TG144I	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-640UHC-6TG144I	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32I	1280	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	IND
LCMXO2-1200HC-5SG32I	1280	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	IND
LCMXO2-1200HC-6SG32I	1280	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	IND
LCMXO2-1200HC-4TG100I	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100I	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100I	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132I	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132I	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132I	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144I	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144I	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144I	1280	2.5 V/ 3.3 V	–6	Halogen-Free TQFP	144	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256I	1280	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-5FTG256I	1280	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-6FTG256I	1280	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100I	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-5TG100I	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-6TG100I	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-4MG132I	2112	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-5MG132I	2112	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-6MG132I	2112	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-4TG144I	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-5TG144I	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-6TG144I	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-4BG256I	2112	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-5BG256I	2112	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-6BG256I	2112	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-4FTG256I	2112	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-5FTG256I	2112	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-6FTG256I	2112	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484I	2112	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-5FG484I	2112	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-6FG484I	2112	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84I	4320	2.5 V / 3.3 V	–4	Halogen-Free QFN	84	IND
LCMXO2-4000HC-5QN84I	4320	2.5 V / 3.3 V	–5	Halogen-Free QFN	84	IND
LCMXO2-4000HC-6QN84I	4320	2.5 V / 3.3 V	–6	Halogen-Free QFN	84	IND
LCMXO2-4000HC-4TG144I	4320	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-5TG144I	4320	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-6TG144I	4320	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-4MG132I	4320	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-5MG132I	4320	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-6MG132I	4320	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-4BG256I	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-5BG256I	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-6BG256I	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-4FTG256I	4320	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-5FTG256I	4320	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-6FTG256I	4320	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-4BG332I	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-5BG332I	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-6BG332I	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-4FG484I	4320	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-5FG484I	4320	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-6FG484I	4320	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144I	6864	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-5TG144I	6864	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-6TG144I	6864	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-4BG256I	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-5BG256I	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-6BG256I	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-4FTG256I	6864	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-5FTG256I	6864	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-6FTG256I	6864	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-4BG332I	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-5BG332I	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-6BG332I	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-4FG400I	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-5FG400I	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-6FG400I	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-4FG484I	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-5FG484I	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-6FG484I	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100IR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100IR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100IR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132IR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132IR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132IR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144IR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144IR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144IR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200HC-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High Performance Industrial Grade Devices Without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100I	2112	1.2 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-5TG100I	2112	1.2 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-6TG100I	2112	1.2 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-4MG132I	2112	1.2 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-5MG132I	2112	1.2 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-6MG132I	2112	1.2 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-4TG144I	2112	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-5TG144I	2112	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-6TG144I	2112	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-4BG256I	2112	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-5BG256I	2112	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-6BG256I	2112	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-4FTG256I	2112	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-5FTG256I	2112	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-6FTG256I	2112	1.2 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484I	2112	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-5FG484I	2112	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-6FG484I	2112	1.2 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4MG132I	4320	1.2 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-5MG132I	4320	1.2 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-6MG132I	4320	1.2 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-4TG144I	4320	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-5TG144I	4320	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-6TG144I	4320	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-4MG184I	4320	1.2 V	–4	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-5MG184I	4320	1.2 V	–5	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-6MG184I	4320	1.2 V	–6	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-4BG256I	4320	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-5BG256I	4320	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-6BG256I	4320	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-4FTG256I	4320	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-5FTG256I	4320	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-6FTG256I	4320	1.2 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-4BG332I	4320	1.2 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-5BG332I	4320	1.2 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-6BG332I	4320	1.2 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-4FG484I	4320	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-5FG484I	4320	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-6FG484I	4320	1.2 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144I	6864	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-5TG144I	6864	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-6TG144I	6864	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-4BG256I	6864	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-5BG256I	6864	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-6BG256I	6864	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-4FTG256I	6864	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-5FTG256I	6864	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-6FTG256I	6864	1.2 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-4BG332I	6864	1.2 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-5BG332I	6864	1.2 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-6BG332I	6864	1.2 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-4FG484I	6864	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-5FG484I	6864	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-6FG484I	6864	1.2 V	–6	Halogen-Free fpBGA	484	IND

R1 Device Specifications

The LCMXO2-1200ZE/HC "R1" devices have the same specifications as their Standard (non-R1) counterparts except as listed below. For more details on the R1 to Standard migration refer to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard Non-R1) Devices.

- The User Flash Memory (UFM) cannot be programmed through the internal WISHBONE interface. It can still be programmed through the JTAG/SPI/I^{2}C ports.
- The on-chip differential input termination resistor value is higher than intended. It is approximately 200Ω as opposed to the intended 100Ω. It is recommended to use external termination resistors for differential inputs. The on-chip termination resistors can be disabled through Lattice design software.
- Soft Error Detection logic may not produce the correct result when it is run for the first time after configuration. To use this feature, discard the result from the first operation. Subsequent operations will produce the correct result.
- Under certain conditions, IIH exceeds data sheet specifications. The following table provides more details:

Condition	Clamp	Pad Rising IIH Max.	Pad Falling IIH Min.	Steady State Pad High IIH	Steady State Pad Low IIL
VPAD > VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD = VCCIO	ON	10 µA	–10 µA	10 µA	10 µA
VPAD = VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD < VCCIO	OFF	10 µA	–10 µA	10 µA	10 µA

- The user SPI interface does not operate correctly in some situations. During master read access and slave write access, the last byte received does not generate the RRDY interrupt.
- In GDDRX2, GDDRX4 and GDDR71 modes, ECLKSYNC may have a glitch in the output under certain conditions, leading to possible loss of synchronization.
- When using the hard I^{2}C IP core, the I^{2}C status registers I2C_1_SR and I2C_2_SR may not update correctly.
- PLL Lock signal will glitch high when coming out of standby. This glitch lasts for about 10 µsec before returning low.
- Dual boot only available on HC devices, requires tying VCC and VCCIO2 to the same 3.3 V or 2.5 V supply.

MachXO2 Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the MachXO2 family are available on the Lattice web site.

- TN1198, Power Estimation and Management for MachXO2 Devices
- TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide
- TN1201, Memory Usage Guide for MachXO2 Devices
- TN1202, MachXO2 sysIO Usage Guide
- TN1203, Implementing High-Speed Interfaces with MachXO2 Devices
- TN1204, MachXO2 Programming and Configuration Usage Guide
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices
- TN1206, MachXO2 SRAM CRC Error Detection Usage Guide
- TN1207, Using TraceID in MachXO2 Devices
- TN1074, PCB Layout Recommendations for BGA Packages
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices
- AN8066, Boundary Scan Testability with Lattice sysIO Capability
- MachXO2 Device Pinout Files
- Thermal Management document
- Lattice design tools

For further information on interface standards, refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, LVDS, DDR, DDR2, LPDDR): www.jedec.org
- PCI: www.pcisig.com

MachXO2 Family Data Sheet Revision History

March 2017 **Data Sheet DS1035**

Date	Version	Section	Change Summary
March 2017	3.3	DC and Switching Characteristics	Updated the Absolute Maximum Ratings section. Added standards.
			Updated the sysIO Recommended Operating Conditions section. Added standards.
			Updated the sysIO Single-Ended DC Electrical Characteristics section. Added standards.
			Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA}. The parameter descriptions were also modified.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA}. The parameter descriptions were also modified.
			Updated the sysCONFIG Port Timing Specifications section. Corrected the t_{INITL} units from ns to µs.
		Pinout Information	Updated the Signal Descriptions section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals.
			Updated the Pinout Information Summary section. Added footnote to MachXO2-1200 32 QFN.
		Ordering Information	Updated the MachXO2 Part Number Description section. Corrected the MG184, BG256, FTG256 package information. Added “(0.8 mm Pitch)” to BG332.
			Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. — Updated LCMXO2-1200ZE-1UWG25ITR50 footnote. — Corrected footnote numbering typo. — Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2-2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s.

Date	Version	Section	Change Summary
May 2016	3.2	All	Moved designation for 84 QFN package information from 'Advanced' to 'Final'.
		Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added ‘Advanced’ 48 QFN package. — Revised footnote 6. — Added footnote 9.
		DC and Switching Characteristics	Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Added footnote 12.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Added footnote 12.
		Pinout Information	Updated the Signal Descriptions section. Added information on GND signal.
			Updated the Pinout Information Summary section. — Added ‘Advanced’ MachXO2-256 48 QFN values. — Added ‘Advanced’ MachXO2-640 48 QFN values. — Added footnote to GND. — Added footnotes 2 and 3.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added ‘Advanced’ SG48 package and revised footnote.
			Updated the Ordering Information section. — Added part numbers for ‘Advanced’ QFN 48 package.
March 2016	3.1	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 32 QFN value for XO2-1200. — Added 84 QFN (7 mm x 7 mm, 0.5 mm) package. — Modified package name to 100-pin TQFP. — Modified package name to 144-pin TQFP. — Added footnote.
		Architecture	Updated the Typical I/O Behavior During Power-up section. Removed reference to TN1202.
		DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications section. Revised $t_{DPPDONE}$ and $t_{DPPINIT}$ Max. values per PCN 03A-16, released March 2016.
		Pinout Information	Updated the Pinout Information Summary section. — Added MachXO2-1200 32 QFN values. — Added ‘Advanced’ MachXO2-4000 84 QFN values.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added ‘Advanced’ QN84 package and footnote.
			Updated the Ordering Information section. — Added part numbers for 1280 LUTs QFN 32 package. — Added part numbers for 4320 LUTs QFN 84 package.
March 2015	3.0	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Changed 64-ball ucBGA dimension.
		Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.

Date	Version	Section	Change Summary
December 2014	2.9	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Removed XO2-4000U data. — Removed 400-ball ftBGA. — Removed 25-ball WLCSP value for XO2-2000U.
		DC and Switching Characteristics	Updated the Recommended Operating Conditions section. Adjusted Max. values for V_{CC} and V_{CCIO}.
			Updated the sysIO Recommended Operating Conditions section. Adjusted Max. values for LVCMOS 3.3, LVTTL, PCI, LVDS33 and LVPECL.
		Pinout Information	Updated the Pinout Information Summary section. Removed MachXO2-4000U.
		Ordering Information	Updated the MachXO2 Part Number Description section. Removed BG400 package.
			Updated the High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
			Updated the High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
November 2014	2.8	Introduction	Updated the Features section. — Revised I/Os under Flexible Logic Architecture. — Revised standby power under Ultra Low Power Devices. — Revise input frequency range under Flexible On-Chip Clocking.
			Updated Table 1-1, MachXO2 Family Selection Guide. — Added XO2-4000U data. — Removed HE and ZE device options for XO2-4000. — Added 400-ball ftBGA.
		Pinout Information	Updated the Pinout Information Summary section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added BG400 package.
			Updated the Ordering Information section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400 part numbers.
October 2014	2.7	Ordering Information	Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Fixed typo in LCMXO2-2000ZE-1UWG49ITR part number package.
		Architecture	Updated the Supported Standards section. Added MIPI information to Table 2-12. Supported Input Standards and Table 2-13. Supported Output Standards.
		DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition.
			Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition.
			Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.
July 2014	2.6	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics[1, 2] section. Updated footnote 4.
			Updated Register-to-Register Performance section. Updated footnote.
		Ordering Information	Updated UW49 package to UWG49 in MachXO2 Part Number Description.
			Updated LCMXO2-2000ZE-1UWG49CTR package in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging.

Date	Version	Section	Change Summary
May 2014	2.5	Architecture	Updated TransFR (Transparent Field Reconfiguration) section. Updated TransFR description for PLL use during background Flash programming.
February 2014	02.4	Introduction	Included the 49 WLCSP package in the MachXO2 Family Selection Guide table.
		Architecture	Added information to Standby Mode and Power Saving Options section.
		Pinout Information	Added the XO2-2000 49 WLCSP in the Pinout Information Summary table.
		Ordering Information	Added UW49 package in MachXO2 Part Number Description.
			Added and LCMXO2-2000ZE-1UWG49CTR in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging section.
			Added and LCMXO2-2000ZE-1UWG49ITR in Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section.
December 2013	02.3	Architecture	Updated information on CLKOS output divider in sysCLOCK Phase Locked Loops (PLLs) section.
		DC and Switching Characteristics	Updated Static Supply Current – ZE Devices table.
			Updated footnote 4 in sysIO Single-Ended DC Electrical Characteristics table; Updated V_{IL} Max. (V) data for LVCMOS 25 and LVCMOS 28.
			Updated V_{OS} test condition in sysIO Differential Electrical Characteristics - LVDS table.
September 2013	02.2	Architecture	Removed I^2C Clock-Stretching feature per PCN #10A-13.
			Removed information on PDPR memory in RAM Mode section.
			Updated Supported Input Standards table.
		DC and Switching Characteristics	Updated Power-On-Reset Voltage Levels table.
June 2013	02.1	Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.
			sysCLOCK Phase Locked Loops (PLLs) section – Added missing cross reference to sysCLOCK PLL Timing table.
		DC and Switching Characteristics	Added slew rate information to footnote 2 of the MachXO2 External Switching Characteristics – HC/HE Devices and the MachXO2 External Switching Characteristics – ZE Devices tables.
			Power-On-Reset Voltage Levels table – Added symbols.

Date	Version	Section	Change Summary
January 2013	02.0	Introduction	Updated the total number IOs to include JTAGENB.
		Architecture	Supported Output Standards table – Added 3.3 V_{CCIO} (Typ.) to LVDS row.
			Changed SRAM CRC Error Detection to Soft Error Detection.
		DC and Switching Characteristics	Power Supply Ramp Rates table – Updated Units column for t_{RAMP} symbol.
			Added new Maximum sysIO Buffer Performance table.
			sysCLOCK PLL Timing table – Updated Min. column values for f_{IN}, f_{OUT}, f_{OUT2} and f_{PFD} parameters. Added t_{SPO} parameter. Updated footnote 6.
			MachXO2 Oscillator Output Frequency table – Updated symbol name for $t_{STABLEOSC.}$
			DC Electrical Characteristics table – Updated conditions for $I_{IL,}$ I_{IH} symbols.
			Corrected parameters tDQVBS and tDQVAS
			Corrected MachXO2 ZE parameters tDVADQ and tDVEDQ
		Pinout Information	Included the MachXO2-4000HE 184 csBGA package.
		Ordering Information	Updated part number.
April 2012	01.9	Architecture	Removed references to TN1200.
		Ordering Information	Updated the Device Status portion of the MachXO2 Part Number Description to include the 50 parts per reel for the WLCSP package.
			Added new part number and footnote 2 for LCMXO2-1200ZE-1UWG25ITR50.
			Updated footnote 1 for LCMXO2-1200ZE-1UWG25ITR.
		Supplemental Information	Removed references to TN1200.
March 2012	01.8	Introduction	Added 32 QFN packaging information to Features bullets and MachXO2 Family Selection Guide table.
		DC and Switching Characteristics	Changed ‘STANDBY’ to ‘USERSTDBY’ in Standby Mode timing diagram.
		Pinout Information	Removed footnote from Pin Information Summary tables.
			Added 32 QFN package to Pin Information Summary table.
		Ordering Information	Updated Part Number Description and Ordering Information tables for 32 QFN package.
			Updated topside mark diagram in the Ordering Information section.

Date	Version	Section	Change Summary
February 2012	01.7	All	Updated document with new corporate logo.
	01.6	—	Data sheet status changed from preliminary to final.
		Introduction	MachXO2 Family Selection Guide table – Removed references to 49-ball WLCSP.
		DC and Switching Characteristics	Updated Flash Download Time table.
			Modified Storage Temperature in the Absolute Maximum Ratings section.
			Updated I_{DK} max in Hot Socket Specifications table.
			Modified Static Supply Current tables for ZE and HC/HE devices.
			Updated Power Supply Ramp Rates table.
			Updated Programming and Erase Supply Current tables.
			Updated data in the External Switching Characteristics table.
			Corrected Absolute Maximum Ratings for Dedicated Input Voltage Applied for LCMXO2 HC.
			DC Electrical Characteristics table – Minor corrections to conditions for I_{IL}, I_{IH}.
		Pinout Information	Removed references to 49-ball WLCSP.
			Signal Descriptions table – Updated description for GND, VCC, and VCCIOx.
			Updated Pin Information Summary table – Number of VCCIOs, GNDs, VCCs, and Total Count of Bonded Pins for MachXO2-256, 640, and 640U and Dual Function I/O for MachXO2-4000 332caBGA.
		Ordering Information	Removed references to 49-ball WLCSP
August 2011	01.5	DC and Switching Characteristics	Updated ESD information.
		Ordering Information	Updated footnote for ordering WLCSP devices.
	01.4	Architecture	Updated information in Clock/Control Distribution Network and sysCLOCK Phase Locked Loops (PLLs).
		DC and Switching Characteristics	Updated I_{IL} and I_{IH} conditions in the DC Electrical Characteristics table.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Updated Pin Information Summary table: Dual Function I/O, DQS Groups Bank 1, Total General Purpose Single-Ended I/O, Differential I/O Per Bank, Total Count of Bonded Pins, Gearboxes. Added column of data for MachXO2-2000 49 WLCSP.
		Ordering Information	Updated R1 Device Specifications text section with information on migration from MachXO2-1200-R1 to Standard (non-R1) devices.
			Corrected Supply Voltage typo for part numbers: LCMX02-2000UHE-4FG484I, LCMX02-2000UHE-5FG484I, LCMX02-2000UHE-6FG484I.
			Added footnote for WLCSP package parts.
		Supplemental Information	Removed reference to Stand-alone Power Calculator for MachXO2 Devices. Added reference to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices.

Date	Version	Section	Change Summary
May 2011	01.3	Multiple	Replaced “SED” with “SRAM CRC Error Detection” throughout the document.
		DC and Switching Characteristics	Added footnote 1 to Program Erase Specifications table.
		Pinout Information	Updated Pin Information Summary tables.
			Signal name SO/SISPISO changed to SO/SPISO in the Signal Descriptions table.
April 2011	01.2	—	Data sheet status changed from Advance to Preliminary.
		Introduction	Updated MachXO2 Family Selection Guide table.
		Architecture	Updated Supported Input Standards table.
			Updated sysMEM Memory Primitives diagram.
			Added differential SSTL and HSTL IO standards.
		DC and Switching Characteristics	Updates following parameters: POR voltage levels, DC electrical characteristics, static supply current for ZE/HE/HC devices, static power consumption contribution of different components – ZE devices, programming and erase Flash supply current.
			Added VREF specifications to sysIO recommended operating conditions.
			Updating timing information based on characterization.
			Added differential SSTL and HSTL IO standards.
		Ordering Information	Added Ordering Part Numbers for R1 devices, and devices in WLCSP packages.
			Added R1 device specifications.
January 2011	01.1	All	Included ultra-high I/O devices.
		DC and Switching Characteristics	Recommended Operating Conditions table – Added footnote 3.
			DC Electrical Characteristics table – Updated data for I_{IL}, I_{IH}. V_{HYST} typical values updated.
			Generic DDRX2 Outputs with Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB}.
			Generic DDRX4 Outputs with Clock and Data Aligned at Pin (GDDRX4_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB}.
			Power-On-Reset Voltage Levels table - clarified note 3.
			Clarified VCCIO related recommended operating conditions specifications.
			Added power supply ramp rate requirements.
			Added Power Supply Ramp Rates table.
			Updated Programming/Erase Specifications table.
			Removed references to V_{CCP}.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Removed references to V_{CCP}.
November 2010	01.0	—	Initial release.

MachXO2™ Family Data Sheet

DS1035 Version 3.3, March 2017

MachXO2 Family Data Sheet Introduction

May 2016 Data Sheet DS1035

Features

- **Flexible Logic Architecture**
  - Six devices with 256 to 6864 LUT4s and 18 to 334 I/Os
- **Ultra Low Power Devices**
  - Advanced 65 nm low power process
  - As low as 22 µW standby power
  - Programmable low swing differential I/Os
  - Stand-by mode and other power saving options
- **Embedded and Distributed Memory**
  - Up to 240 kbits sysMEM™ Embedded Block RAM
  - Up to 54 kbits Distributed RAM
  - Dedicated FIFO control logic
- **On-Chip User Flash Memory**
  - Up to 256 kbits of User Flash Memory
  - 100,000 write cycles
  - Accessible through WISHBONE, SPI, I^2C and JTAG interfaces
  - Can be used as soft processor PROM or as Flash memory
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated gearing logic
  - 7:1 Gearing for Display I/Os
  - Generic DDR, DDRX2, DDRX4
  - Dedicated DDR/DDR2/LPDDR memory with DQS support
- **High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - PCI
    - LVDS, Bus-LVDS, MLVDS, RSDS, LVPECL
    - SSTL 25/18
    - HSTL 18
    - Schmitt trigger inputs, up to 0.5 V hysteresis
  - I/Os support hot socketing
  - On-chip differential termination
  - Programmable pull-up or pull-down mode
- **Flexible On-Chip Clocking**
  - Eight primary clocks
  - Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
  - Up to two analog PLLs per device with fractional-n frequency synthesis
    - Wide input frequency range (7 MHz to 400 MHz)
- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - Single-chip, secure solution
  - Programmable through JTAG, SPI or I^2C
  - Supports background programming of non-volatile memory
  - Optional dual boot with external SPI memory
- **TransFR™ Reconfiguration**
  - In-field logic update while system operates
- **Enhanced System Level Support**
  - On-chip hardened functions: SPI, I^2C, timer/counter
  - On-chip oscillator with 5.5% accuracy
  - Unique TraceID for system tracking
  - One Time Programmable (OTP) mode
  - Single power supply with extended operating range
  - IEEE Standard 1149.1 boundary scan
  - IEEE 1532 compliant in-system programming
- **Broad Range of Package Options**
  - TQFP, WLCSP, ucBGA, csBGA, caBGA, ftBGA, fpBGA, QFN package options
  - Small footprint package options
    - As small as 2.5 mm x 2.5 mm
  - Density migration supported
  - Advanced halogen-free packaging

Table 1-1. MachXO2™ Family Selection Guide

		XO2-256	XO2-640	XO2-640U[1]	XO2-1200	XO2-1200U[1]	XO2-2000	XO2-2000U[1]	XO2-4000	XO2-7000
LUTs		256	640	640	1280	1280	2112	2112	4320	6864
Distributed RAM (kbits)		2	5	5	10	10	16	16	34	54
EBR SRAM (kbits)		0	18	64	64	74	74	92	92	240
Number of EBR SRAM Blocks (9 kbits/block)		0	2	7	7	8	8	10	10	26
UFM (kbits)		0	24	64	64	80	80	96	96	256
Device Options:	HC[2]	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	HE[3]						Yes	Yes	Yes	Yes
	ZE[4]	Yes	Yes		Yes		Yes		Yes	Yes
Number of PLLs		0	0	1	1	1	1	2	2	2
Hardened Functions:	I2C	2	2	2	2	2	2	2	2	2
	SPI	1	1	1	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1	1	1	1
Packages						**IO**				
25-ball WLCSP[5] (2.5 mm x 2.5 mm, 0.4 mm)					18					
32 QFN[6] (5 mm x 5 mm, 0.5 mm)		21			21					
48 QFN[8, 9] (7 mm x 7 mm, 0.5 mm)		40	40							
49-ball WLCSP[5] (3.2 mm x 3.2 mm, 0.4 mm)							38			
64-ball ucBGA (4 mm x 4 mm, 0.4 mm)		44								
84 QFN[7] (7 mm x 7 mm, 0.5 mm)									68	
100-pin TQFP (14 mm x 14 mm)		55	78		79		79			
132-ball csBGA (8 mm x 8 mm, 0.5 mm)		55	79		104		104		104	
144-pin TQFP (20 mm x 20 mm)				107	107		111		114	114
184-ball csBGA[7] (8 mm x 8 mm, 0.5 mm)									150	
256-ball caBGA (14 mm x 14 mm, 0.8 mm)							206		206	206
256-ball ftBGA (17 mm x 17 mm, 1.0 mm)						206	206		206	206
332-ball caBGA (17 mm x 17 mm, 0.8 mm)									274	278
484-ball ftBGA (23 mm x 23 mm, 1.0 mm)								278	278	334

1. Ultra high I/O device.
2. High performance with regulator – VCC = 2.5 V, 3.3 V
3. High performance without regulator – V_{CC} = 1.2 V
4. Low power without regulator – V_{CC} = 1.2 V
5. WLCSP package only available for ZE devices.
6. 32 QFN package only available for HC and ZE devices.
7. 184 csBGA package only available for HE devices.
8. 48-pin QFN information is ‘Advanced’.
9. 48 QFN package only available for HC devices.

Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I^2C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external V_{CC} supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V_{CC} supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I^2C port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

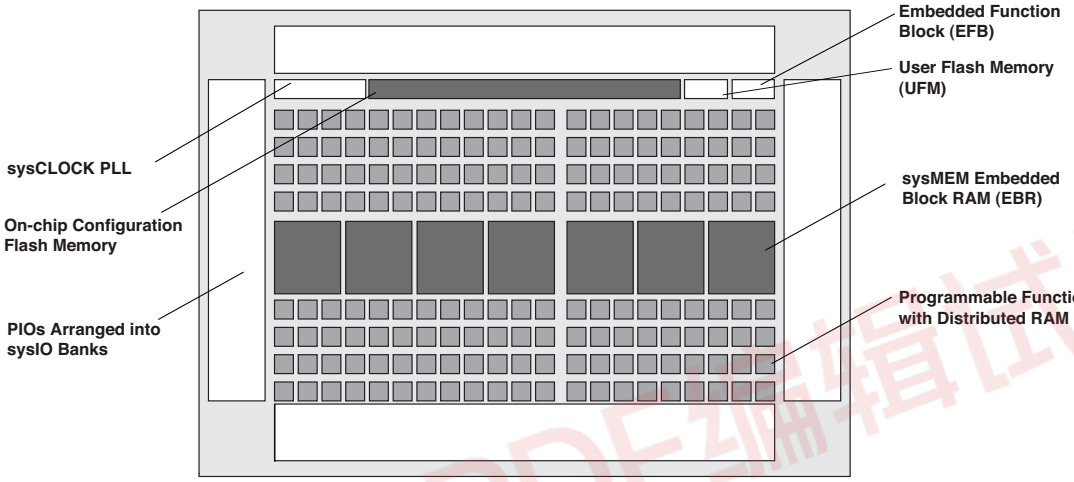
Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

Architecture Overview

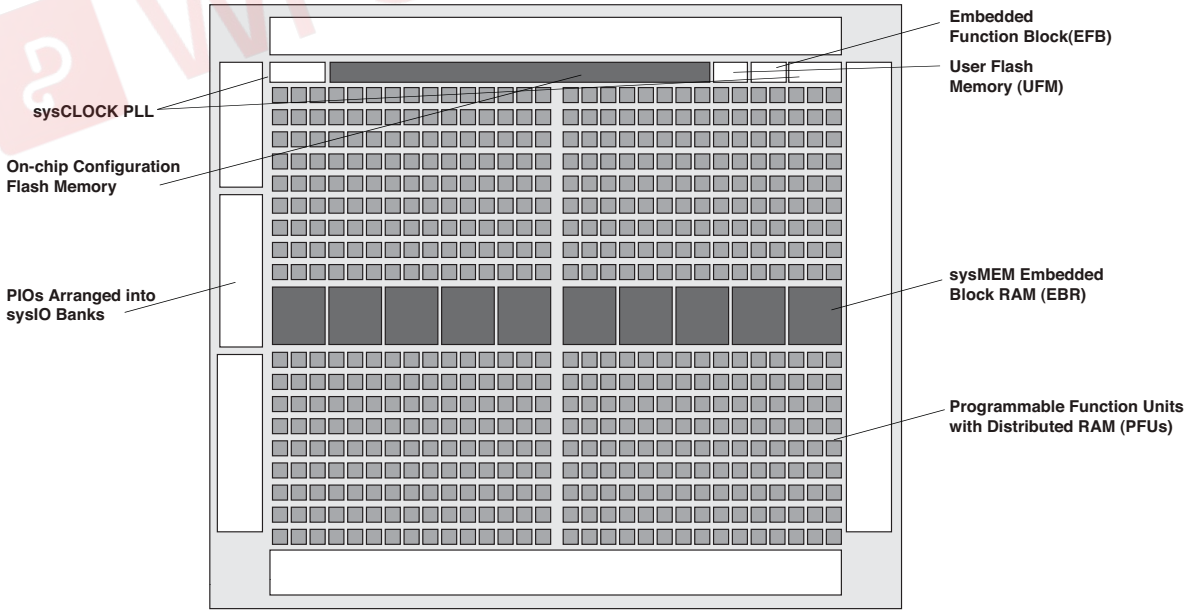
The MachXO2 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.

Figure 2-1. Top View of the MachXO2-1200 Device



Note: MachXO2-256, and MachXO2-640/U are similar to MachXO2-1200. MachXO2-256 has a lower LUT count and no PLL or EBR blocks. MachXO2-640 has no PLL, a lower LUT count and two EBR blocks. MachXO2-640U has a lower LUT count, one PLL and seven EBR blocks.

Figure 2-2. Top View of the MachXO2-4000 Device



Note: MachXO2-1200U, MachXO2-2000/U and MachXO2-7000 are similar to MachXO2-4000. MachXO2-1200U and MachXO2-2000 have a lower LUT count, one PLL, and eight EBR blocks. MachXO2-2000U has a lower LUT count, two PLLs, and 10 EBR blocks. MachXO2-7000 has a higher LUT count, two PLLs, and 26 EBR blocks.

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2-640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

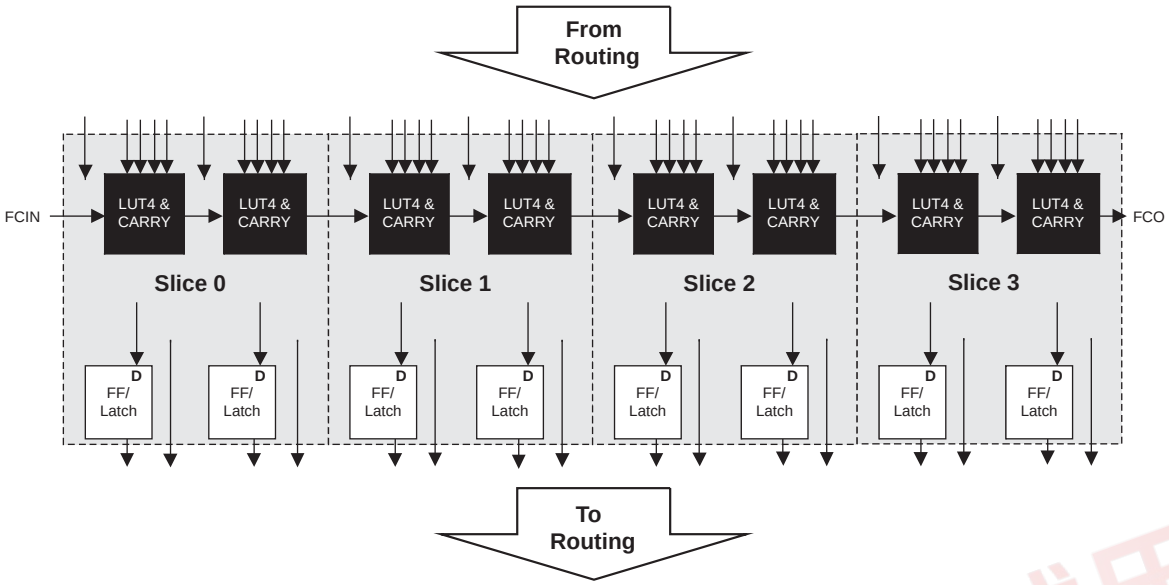
MachXO2 devices provide commonly used hardened functions such as SPI controller, I^2C controller and timer/counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I^2C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

PFU Blocks

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Block Diagram



Slices

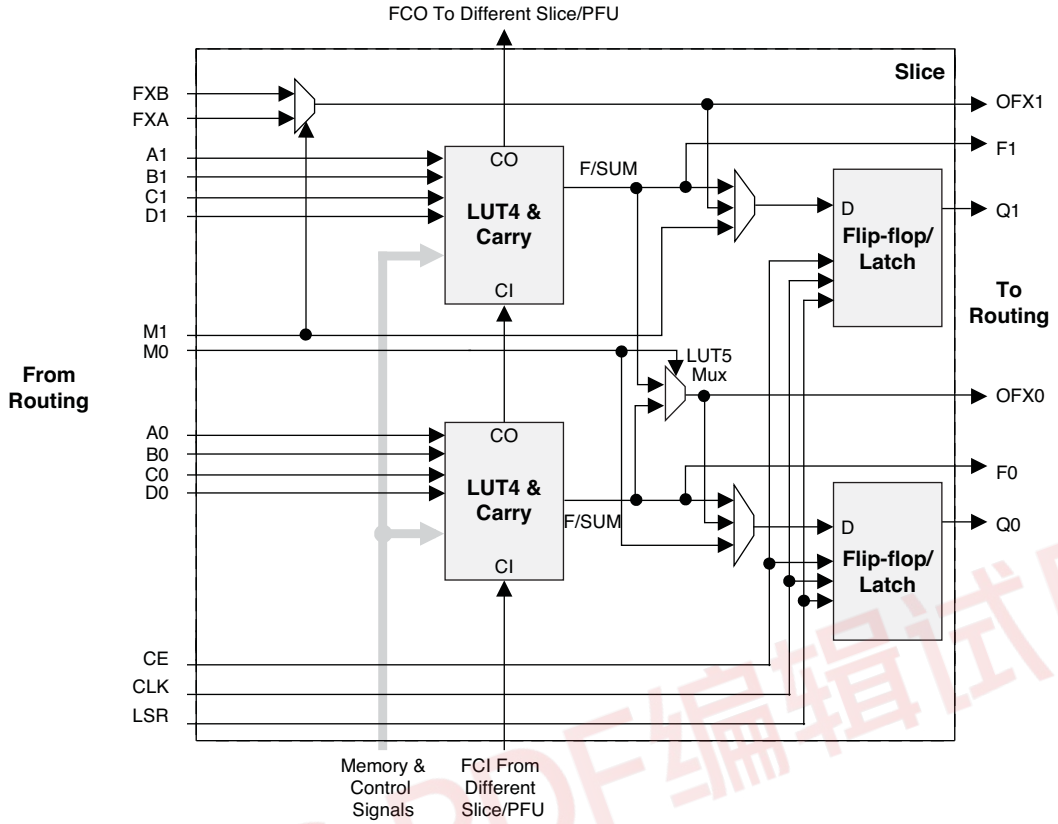
Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU Block	
	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.

Figure 2-4. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multi-purpose input
Input	Control signal	CE	Clock enable
Input	Control signal	LSR	Local set/reset
Input	Control signal	CLK	System clock
Input	Inter-PFU signal	FCIN	Fast carry in[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Fast carry out[1]

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO2 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO2 devices, please see TN1201, Memory Usage Guide for MachXO2 Devices.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

Routing

There are many resources provided in the MachXO2 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Each MachXO2 device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

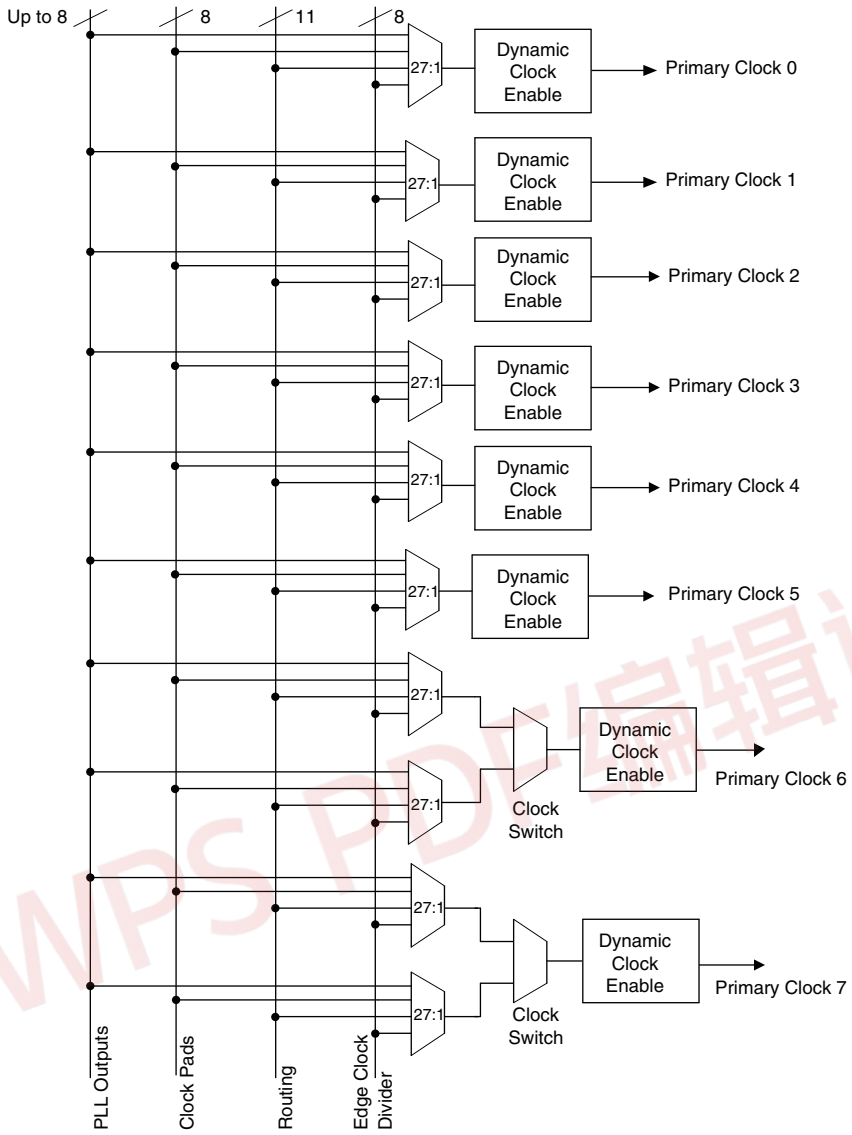
The MachXO2 architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO2-640U, MachXO2-1200/U and higher density devices have two edge clocks each on the top and bottom edges. Lower density devices have no edge clocks. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO2 devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO2 External Switching Characteristics table.

The primary clock signals for the MachXO2-256 and MachXO2-640 are generated from eight 17:1 muxes The available clock sources include eight I/O sources and 9 routing inputs. Primary clock signals for the MachXO2-640U, MachXO2-1200/U and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.

Figure 2-5. Primary Clocks for MachXO2 Devices

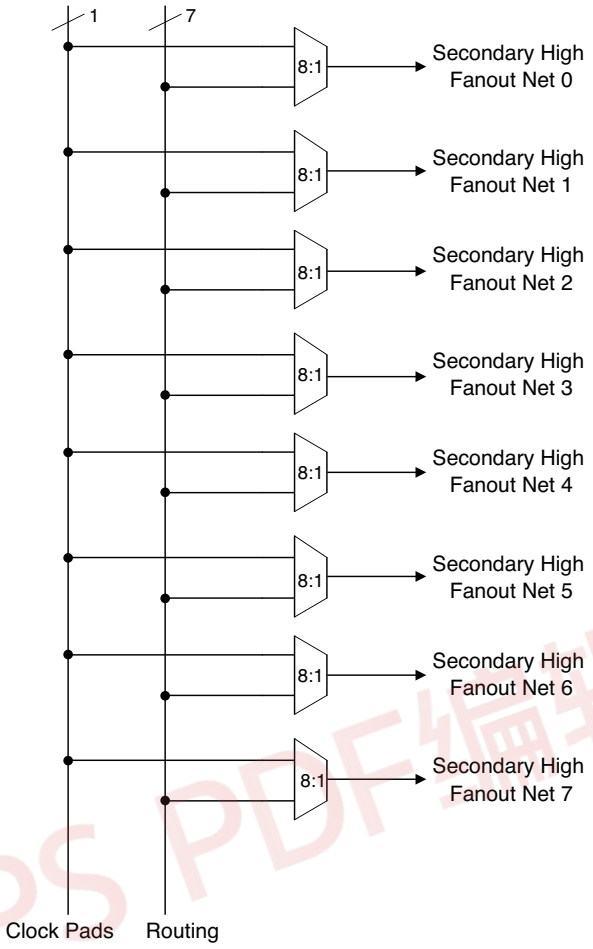


Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO2 External Switching Characteristics table.

Figure 2-6. Secondary High Fanout Nets for MachXO2 Devices



sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The MachXO2-640U, MachXO2-1200/U and larger devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO2 sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO2 clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.

This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the t_{LOCK} parameter has been satisfied.

The MachXO2 also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO2 PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the t_{LOCK} parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

For more details on the PLL and the WISHBONE interface, see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

Figure 2-7. PLL Diagram

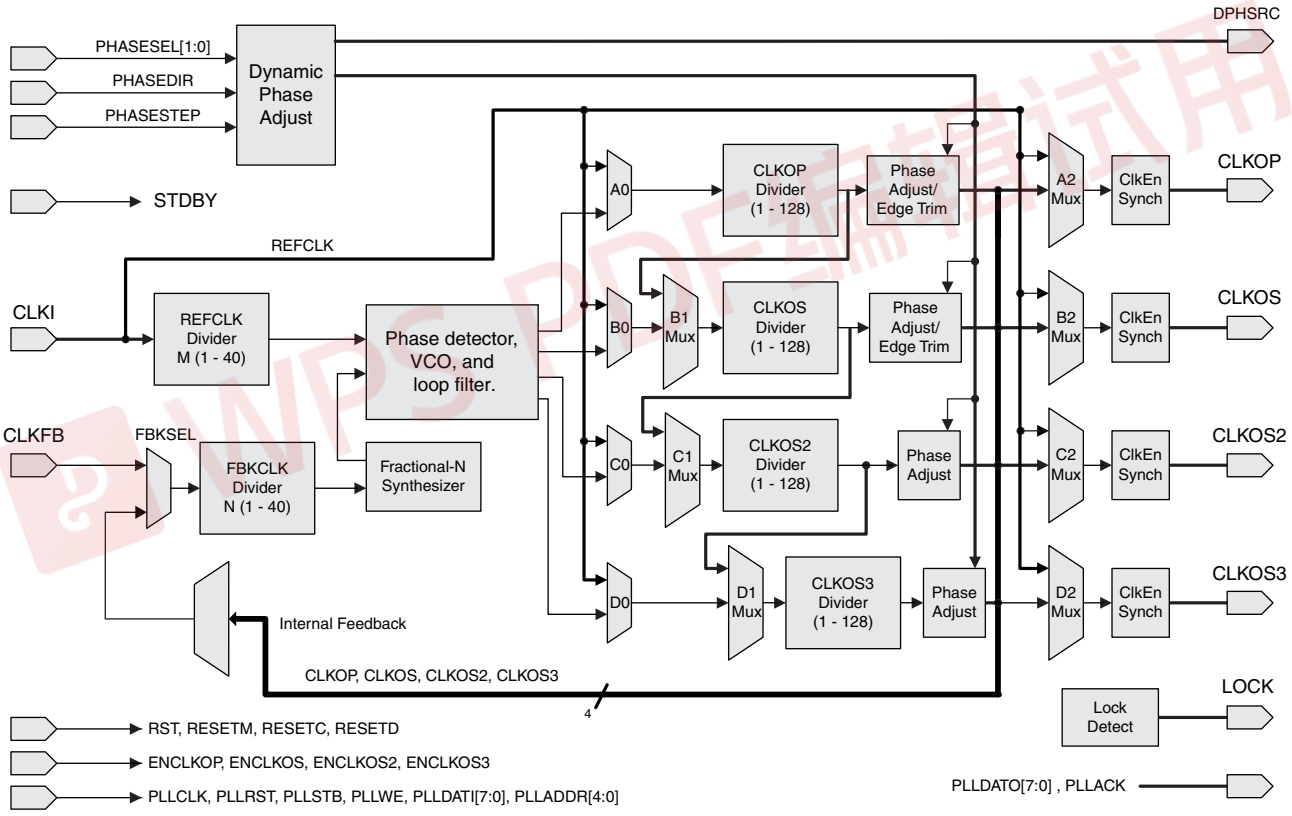


Table 2-4 provides signal descriptions of the PLL block.

Table 2-4. PLL Signal Descriptions

Port Name	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	I	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	I	Dynamic Phase step – toggle shifts VCO phase adjust by one step.

Table 2-4. PLL Signal Descriptions (Continued)

Port Name	I/O	Description
CLKOP	O	Primary PLL output clock (with phase shift adjustment)
CLKOS	O	Secondary PLL output clock (with phase shift adjust)
CLKOS2	O	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	O	Secondary PLL output clock3 (with phase shift adjust)
LOCK	O	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feedback signals.
DPHSRC	O	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset - includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	O	PLL data bus data output
PLLACK	O	PLL data bus acknowledge signal

sysMEM Embedded Block RAM Memory

The MachXO2-640/U and larger devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO2 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

Figure 2-8. sysMEM Memory Primitives

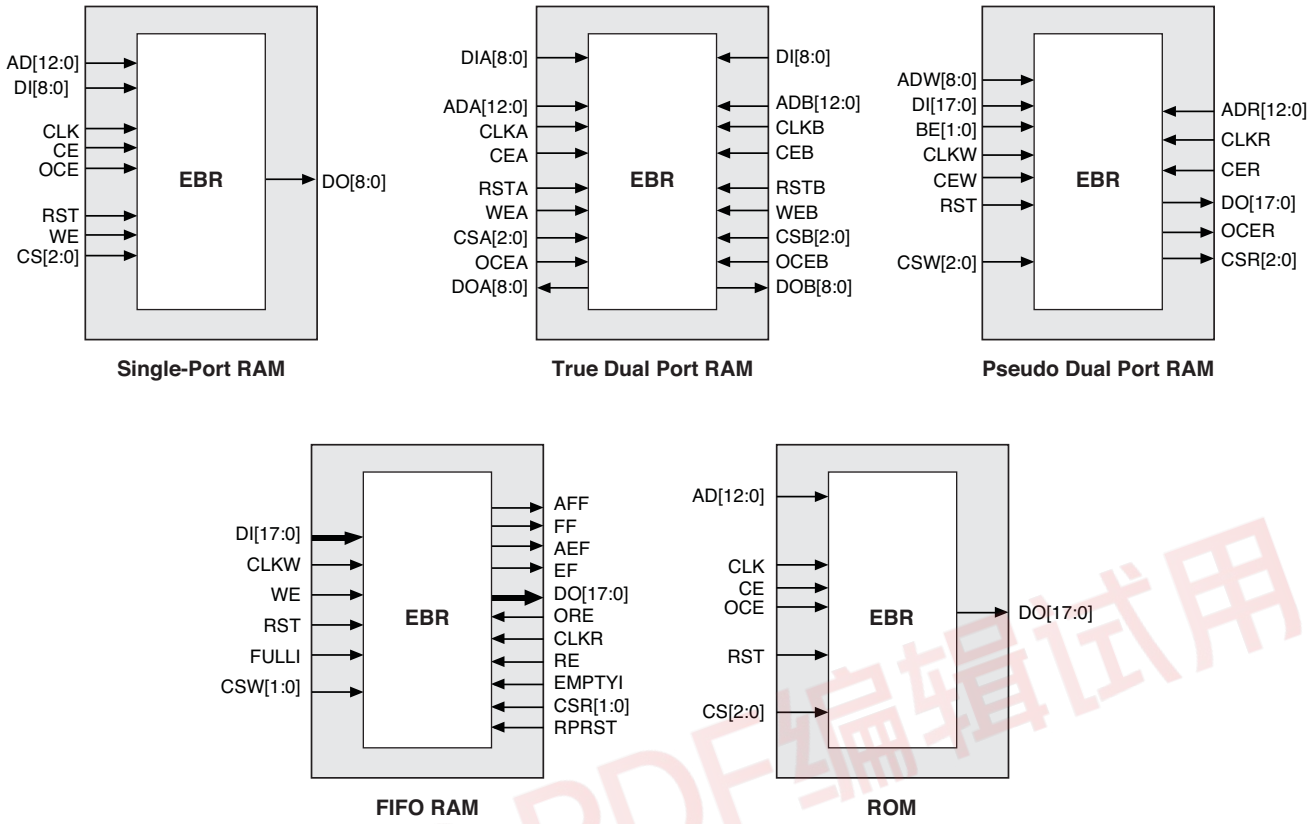


Table 2-6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE[1]	Output Clock Enable	Active High
RST	Reset	Active High
BE[1]	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	—
DI	Data In	—
DO	Data Out	—
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	—
FF	FIFO RAM Full Flag	—
AEF	FIFO RAM Almost Empty Flag	—
EF	FIFO RAM Empty Flag	—
RPRST	FIFO RAM Read Pointer Reset	—

1. Optional signals.
2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.

3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

Table 2-7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

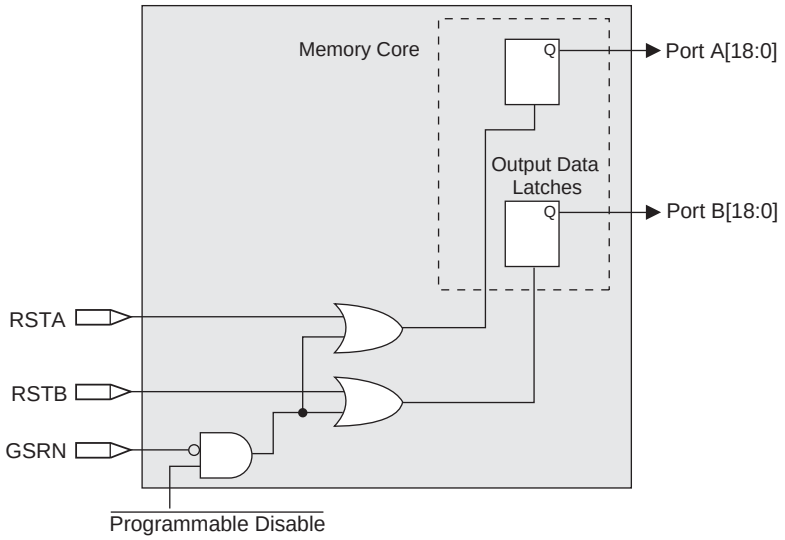
N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

Figure 2-9. Memory Core Reset

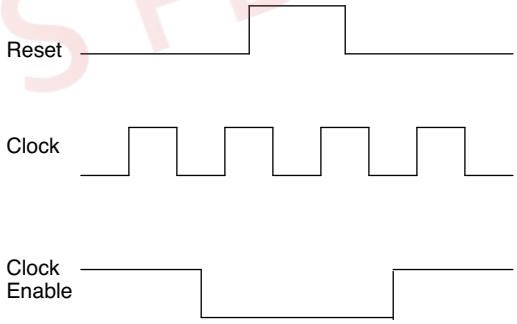


For further information on the sysMEM EBR block, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-10. The reset timing rules apply to the RPReset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For more details refer to TN1201, Memory Usage Guide for MachXO2 Devices.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

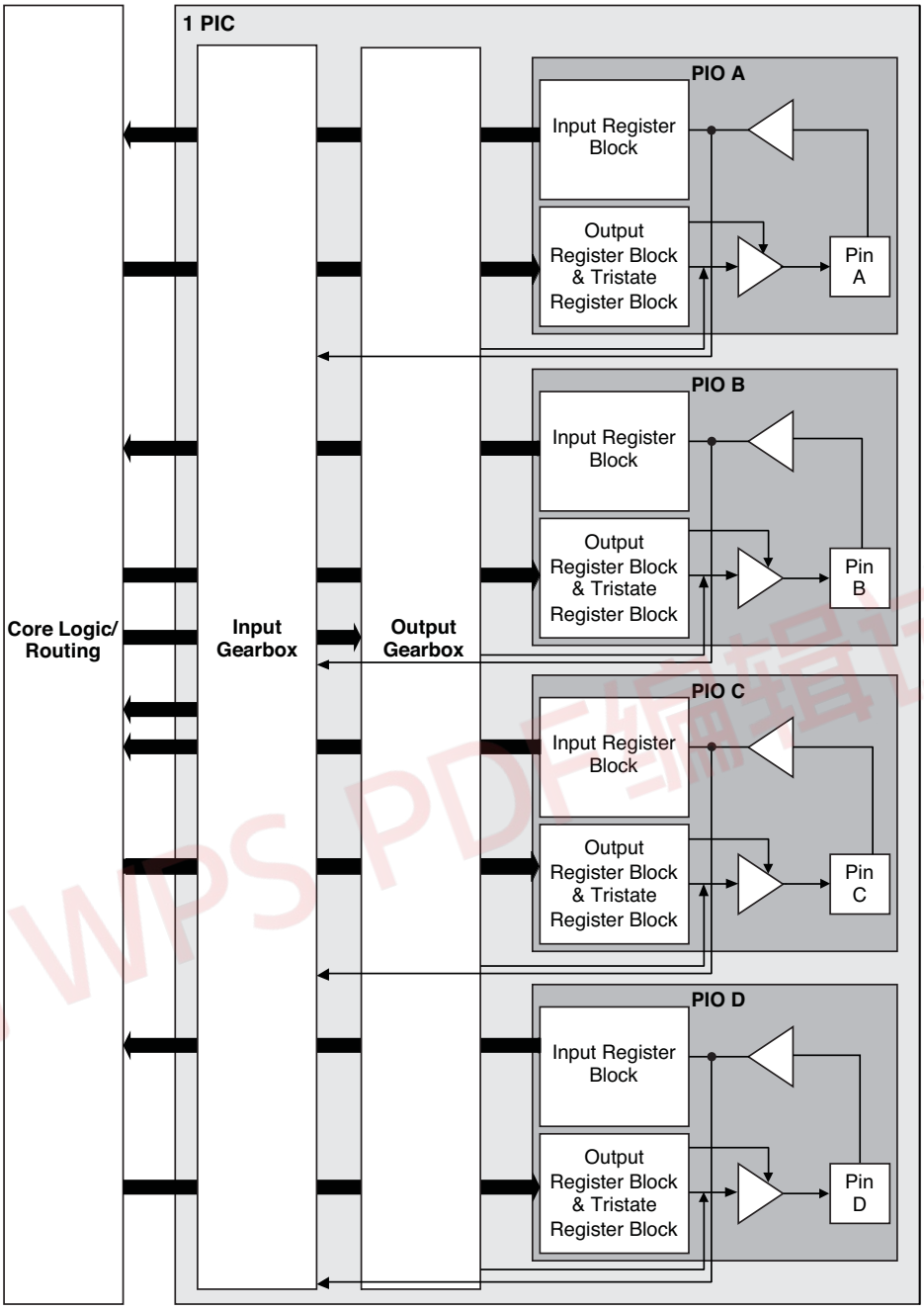
Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO2 devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO2 devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

The MachXO2-640U, MachXO2-1200/U and higher density devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these higher density devices have on-chip differential termination and also provide PCI support.

Figure 2-11. Group of Four Programmable I/O Cells



Notes:
1. Input gearbox is available only in PIC on the bottom edge of MachXO2-640U, MachXO2-1200/U and larger devices.
2. Output gearbox is available only in PIC on the top edge of MachXO2-640U, MachXO2-1200/U and larger devices.

PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Table 2-8. PIO Signal List

Pin Name	I/O Type	Description
CE	Input	Clock Enable
D	Input	Pin input from sysIO buffer.
INDD	Output	Register bypassed input.
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysIO Buffer
TQ	Output	Tri-state output signals to sysIO Buffer
DQSR90[1]	Input	DQS shift 90-degree read clock
DQSW90[1]	Input	DQS shift 90-degree write clock
DDRCLKPOL[1]	Input	DDR input register polarity control signal from DQS
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

1. Available in PIO on right edge only.

Input Register Block

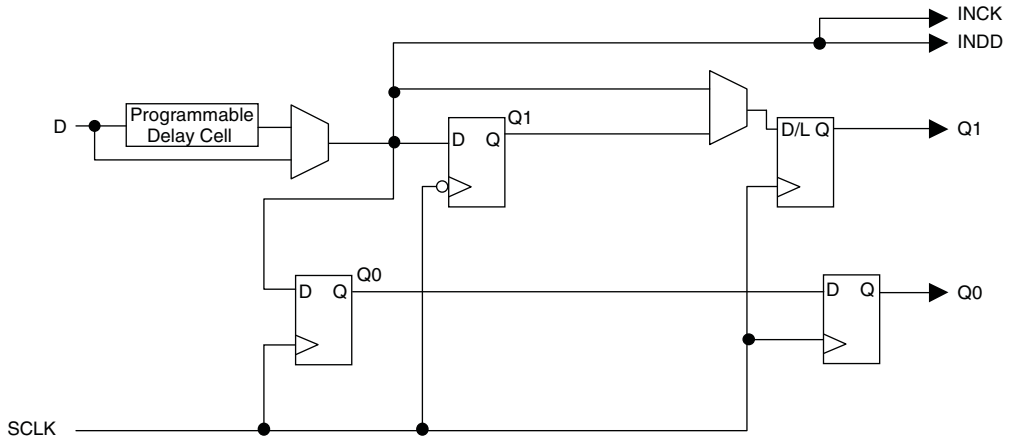
The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition to this functionality, the input register blocks for the PIOs on the right edge include built-in logic to interface to DDR memory.

Figure 2-12 shows the input register block for the PIOs located on the left, top and bottom edges. Figure 2-13 shows the input register block for the PIOs on the right edge.

Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

Figure 2-12. MachXO2 Input Register Block Diagram (PIO on Left, Top and Bottom Edges)



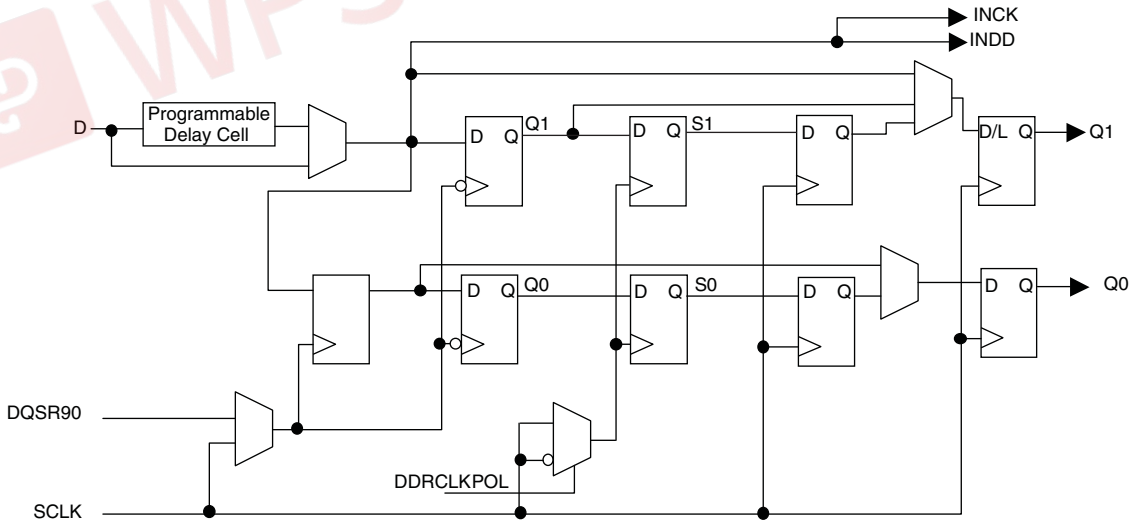
Right Edge

The input register block on the right edge is a superset of the same block on the top, bottom, and left edges. In addition to the modes described above, the input register block on the right edge also supports DDR memory mode.

In DDR memory mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (DQSR90) in the DDR Memory mode creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the DQS domain. The DQSR90 and DDRCLKPOL signals are generated in the DQS read-write block.

Figure 2-13. MachXO2 Input Register Block Diagram (PIO on Right Edge)



Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

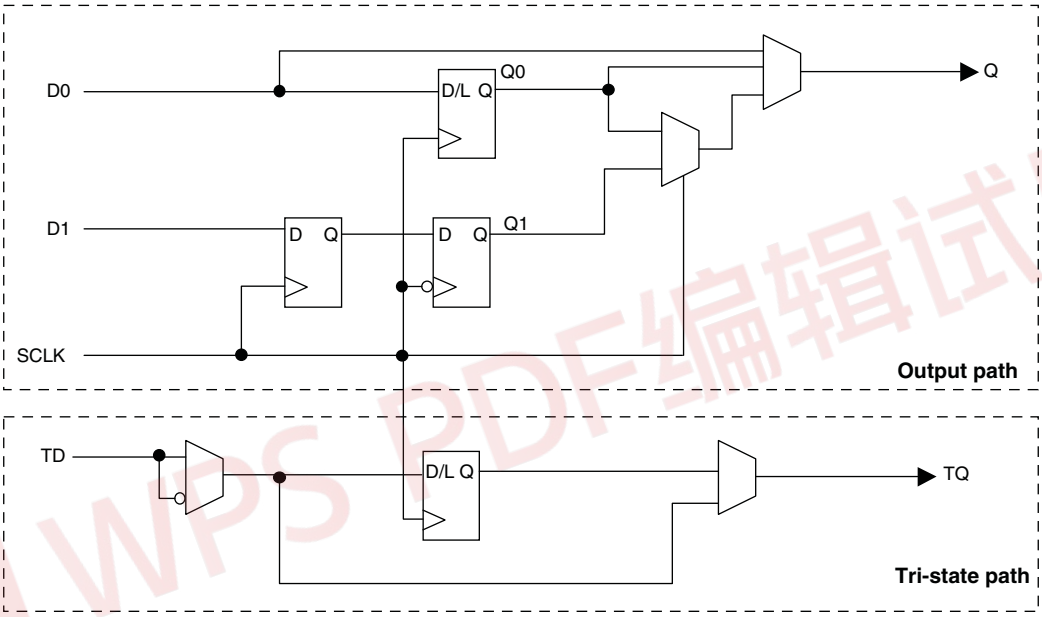
Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-14 shows the output register block on the left, top and bottom edges.

Figure 2-14. MachXO2 Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)



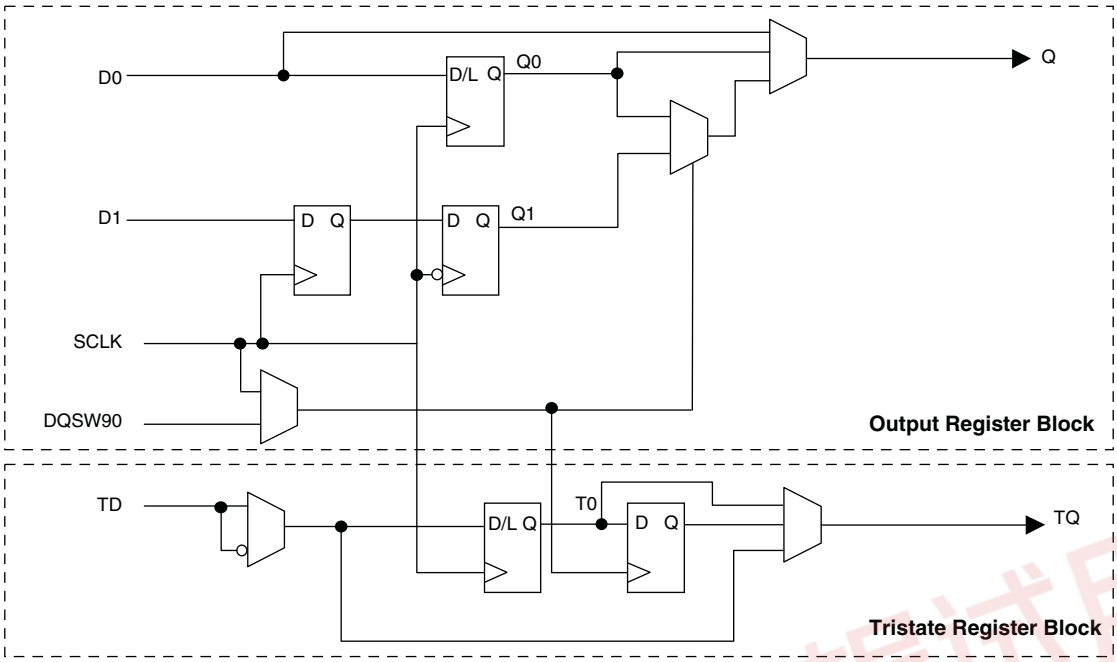
Right Edge

The output register block on the right edge is a superset of the output register on left, top and bottom edges of the device. In addition to supporting SDR and Generic DDR modes, the output register blocks for PIOs on the right edge include additional logic to support DDR-memory interfaces. Operation of this block is similar to that of the output register block on other edges.

In DDR memory mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the DQSW90 signal is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-15 shows the output register block on the right edge.

Figure 2-15. MachXO2 Output Register Block Diagram (PIO on the Right Edges)



Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

The tri-state register blocks on the right edge contain an additional register for DDR memory operation. In DDR memory mode, the register TS input is fed into another register that is clocked using the DQSW90 signal. The output of this register is used as a tri-state control.

Input Gearbox

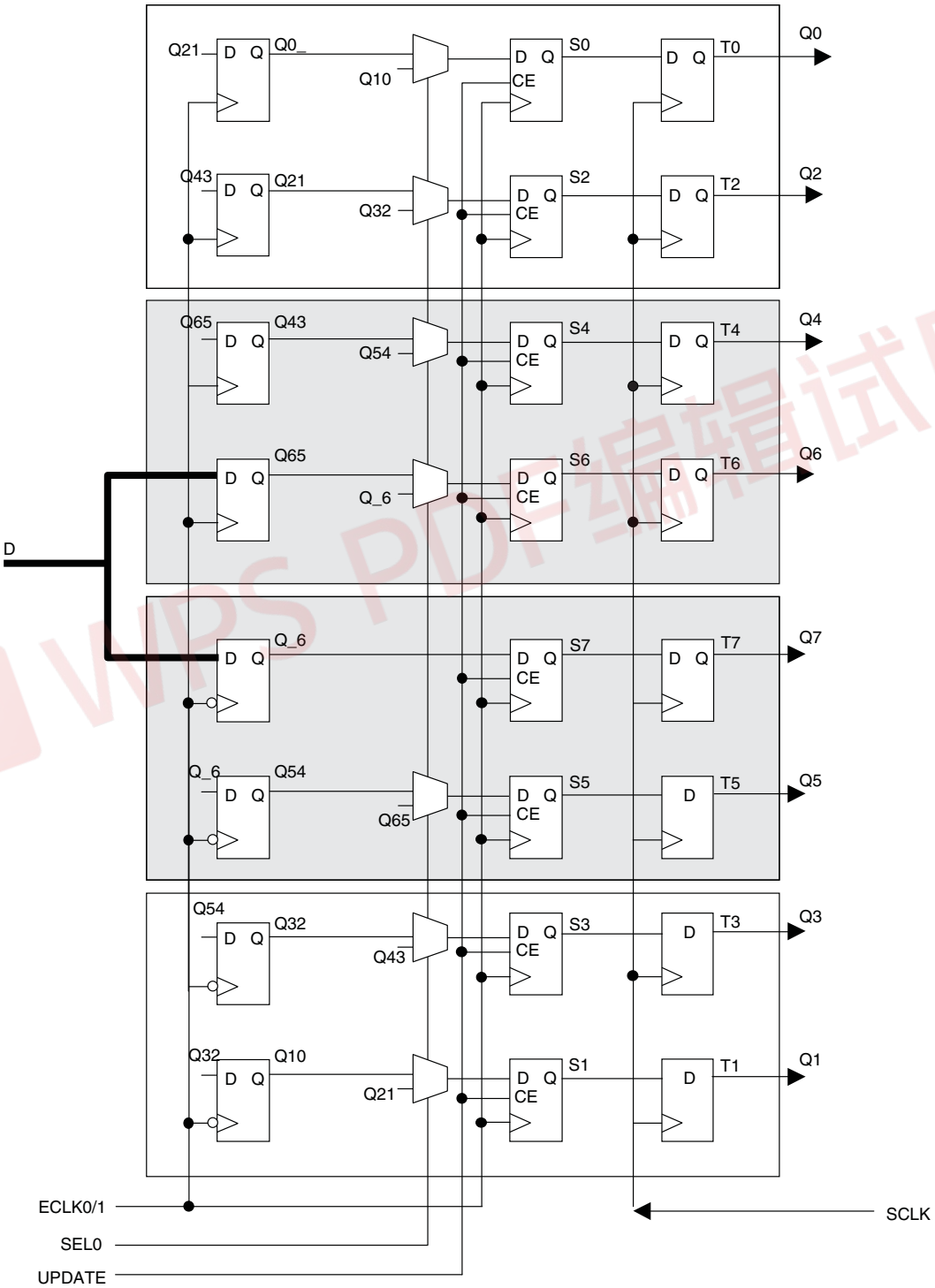
Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

Table 2-9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-16 shows a block diagram of the input gearbox.

Figure 2-16. Input Gearbox



More information on the input gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.

Output Gearbox

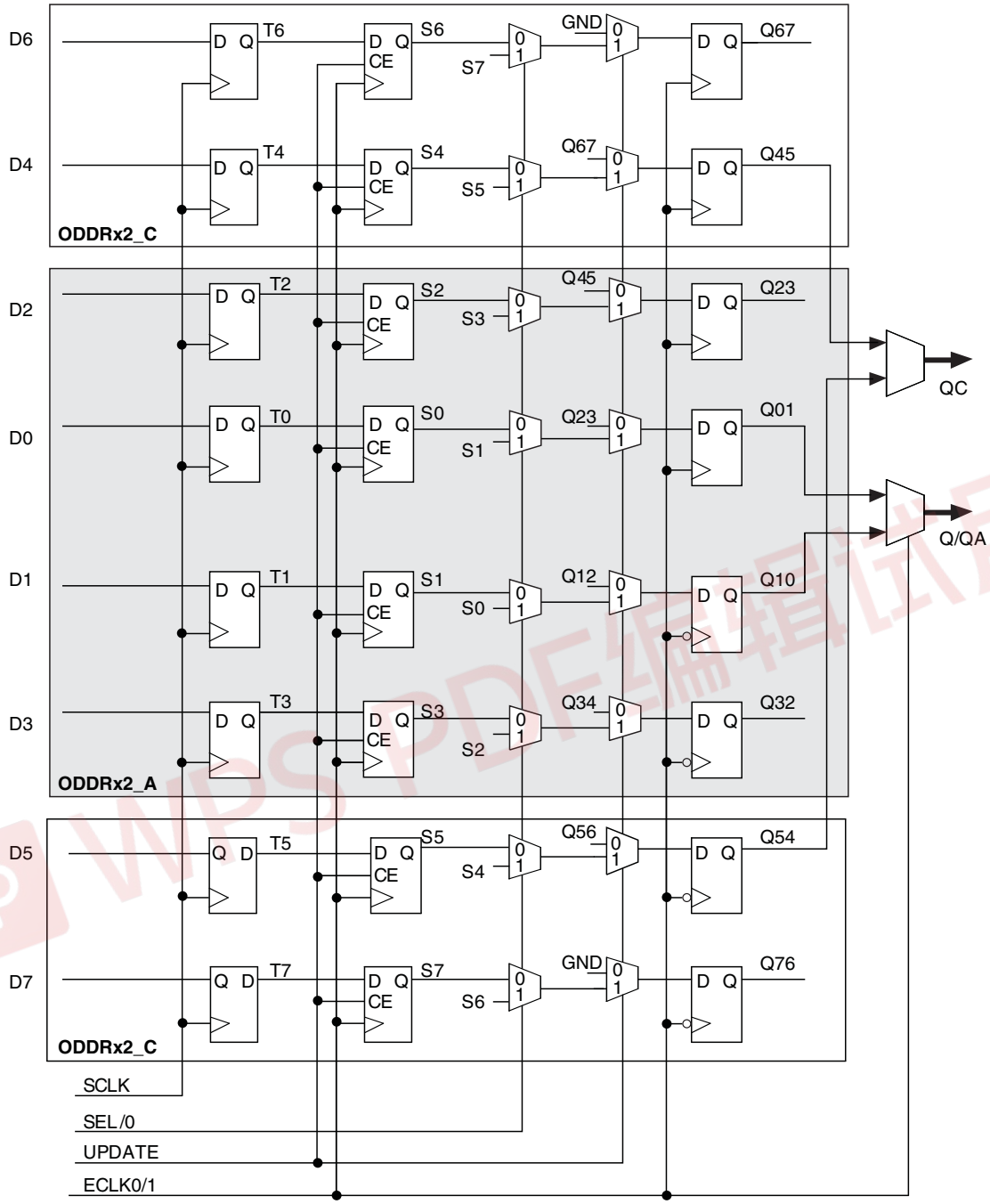
Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

Table 2-10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDRX4(8:1): D[7:0]		
GDDRX2(4:1)(IOL-A): D[3:0]		
GDDRX2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-17 shows the output gearbox block diagram.

Figure 2-17. Output Gearbox



More information on the output gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.

DDR Memory Support

Certain PICs on the right edge of MachXO2-640U, MachXO2-1200/U and larger devices, have additional circuitry to allow the implementation of DDR memory interfaces. There are two groups of 14 or 12 PIOs each on the right edge with additional circuitry to implement DDR memory interfaces. This capability allows the implementation of up to 16-bit wide memory interfaces. One PIO from each group contains a control element, the DQS Read/Write Block, to facilitate the generation of clock and control signals (DQSR90, DQSW90, DDRCLKPOL and DATAVALID). These clock and control signals are distributed to the other PIO in the group through dedicated low skew routing.

DQS Read Write Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Read Write block provides the required clock alignment for DDR memory interfaces. DQSR90 and DQSW90 signals are generated by the DQS Read Write block from the DQS input.

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the read cycle) is unknown. The MachXO2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This circuit changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each read cycle for the correct clock polarity. Prior to the read operation in DDR memories, DQS is in tri-state (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit in the DQS Read Write block detects the first DQS rising edge after the preamble state and generates the DDRCLKPOL signal. This signal is used to control the polarity of the clock to the synchronizing registers.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration signals (6-bit bus) from a DLL on the right edge of the device. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, PCI, SSTL, HSTL, LVDS, BLVDS, MLVDS and LVPECL.

Each bank is capable of supporting multiple I/O standards. In the MachXO2 devices, single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS and PCI), differential (LVDS) and referenced input buffers (SSTL and HSTL) are powered using I/O supply voltage (V_{CCIO}). Each sysIO bank has its own V_{CCIO}. In addition, each bank has a voltage reference, V_{REF}, which allows the use of referenced input buffers independent of the bank V_{CCIO}.

MachXO2-256 and MachXO2-640 devices contain single-ended ratioed input buffers and single-ended output buffers with complementary outputs on all the I/O banks. Note that the single-ended input buffers on these devices do not contain PCI clamps. In addition to the single-ended I/O buffers these two devices also have differential and referenced input buffers on all I/Os. The I/Os are arranged in pairs, the two pads in the pair are described as "T" and "C", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 devices contain three types of sysIO buffer pairs.

1. **Left and Right sysIO Buffer Pairs**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential and referenced input buffers.

2. **Bottom sysIO Buffer Pairs**
   The sysIO buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential and referenced input buffers. Only the I/Os on the bottom banks have programmable PCI clamps and differential input termination. The PCI clamp is enabled after V_{CC} and V_{CCIO} are at valid operating levels and the device has been configured.

3. **Top sysIO Buffer Pairs**
   The sysIO buffer pairs in the top bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential and referenced I/O buffers. Half of the sysIO buffer pairs on the top edge have true differential outputs. The sysIO buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver. The referenced input buffer can also be configured as a differential input buffer.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCIO0} have reached V_{PORUP} level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-down to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to V_{CCIO} as the default functionality). The I/O pins will maintain the blank configuration until V_{CC} and V_{CCIO} (for I/O banks containing configuration I/Os) have reached V_{PORUP} levels at which time the I/Os will take on the user-configured settings only after a proper download/configuration.

Supported Standards

The MachXO2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL, and PCI. The buffer supports the LVTTL, PCI, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO2-640U, MachXO2-1200/U and higher devices support on-chip LVDS output buffers on approximately 50% of the I/Os on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO2 devices. PCI support is provided in the bottom bank of theMachXO2-640U, MachXO2-1200/U and higher density devices. Table 2-11 summarizes the I/O characteristics of the MachXO2 PLDs.

Tables 2-11 and 2-12 show the I/O standards (together with their supply and reference voltages) supported by the MachXO2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1202, MachXO2 sysIO Usage Guide.

Table 2-11. I/O Support Device by Device

	MachXO2-256, MachXO2-640	MachXO2-640U, MachXO2-1200	MachXO2-1200U MachXO2-2000/U, MachXO2-4000, MachXO2-7000
Number of I/O Banks	4	4	6
Type of Input Buffers	Single-ended (all I/O banks) Differential Receivers (all I/O banks)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)
Types of Output Buffers	Single-ended buffers with complementary outputs (all I/O banks)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)
Differential Output Emulation Capability	All I/O banks	All I/O banks	All I/O banks
PCI Clamp Support	No	Clamp on bottom side only	Clamp on bottom side only

Table 2-12. Supported Input Standards

	VCCIO (Typ.)				
Input Standard	**3.3 V**	**2.5 V**	**1.8 V**	**1.5**	**1.2 V**
Single-Ended Interfaces					
LVTTL	✓	✓[2]	✓[2]	✓[2]	
LVCMOS33	✓	✓[2]	✓[2]	✓[2]	
LVCMOS25	✓[2]	✓	✓[2]	✓[2]	
LVCMOS18	✓[2]	✓[2]	✓	✓[2]	
LVCMOS15	✓[2]	✓[2]	✓[2]	✓	✓[2]
LVCMOS12	✓[2]	✓[2]	✓[2]	✓[2]	✓
PCI[1]	✓				
SSTL18 (Class I, Class II)	✓	✓	✓		
SSTL25 (Class I, Class II)	✓	✓			
HSTL18 (Class I, Class II)	✓	✓	✓		
Differential Interfaces					
LVDS	✓	✓			
BLVDS, MVDS, LVPECL, RSDS	✓	✓			
MIPI[3]	✓	✓			
Differential SSTL18 Class I, II	✓	✓	✓		
Differential SSTL25 Class I, II	✓	✓			
Differential HSTL18 Class I, II	✓	✓	✓		

1. Bottom banks of MachXO2-640U, MachXO2-1200/U and higher density devices only.
2. Reduced functionality. Refer to TN1202, MachXO2 sysIO Usage Guide for more detail.
3. These interfaces can be emulated with external resistors in all devices.

Table 2-13. Supported Output Standards

Output Standard	V_{CCIO} (Typ.)
Single-Ended Interfaces	
LVTTL	3.3
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8
LVCMOS15	1.5
LVCMOS12	1.2
LVCMOS33, Open Drain	—
LVCMOS25, Open Drain	—
LVCMOS18, Open Drain	—
LVCMOS15, Open Drain	—
LVCMOS12, Open Drain	—
PCI33	3.3
SSTL25 (Class I)	2.5
SSTL18 (Class I)	1.8
HSTL18(Class I)	1.8
Differential Interfaces	
LVDS[1, 2]	2.5, 3.3
BLVDS, MLVDS, RSDS [2]	2.5
LVPECL[2]	3.3
MIPI[2]	2.5
Differential SSTL18	1.8
Differential SSTL25	2.5
Differential HSTL18	1.8

1. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.

sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO2-1200U, MachXO2-2000/U and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO2-1200 and lower density devices have four banks (one bank per side). Figures 2-18 and 2-19 show the sysIO banks and their associated supplies for all devices.

Figure 2-18. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 Banks

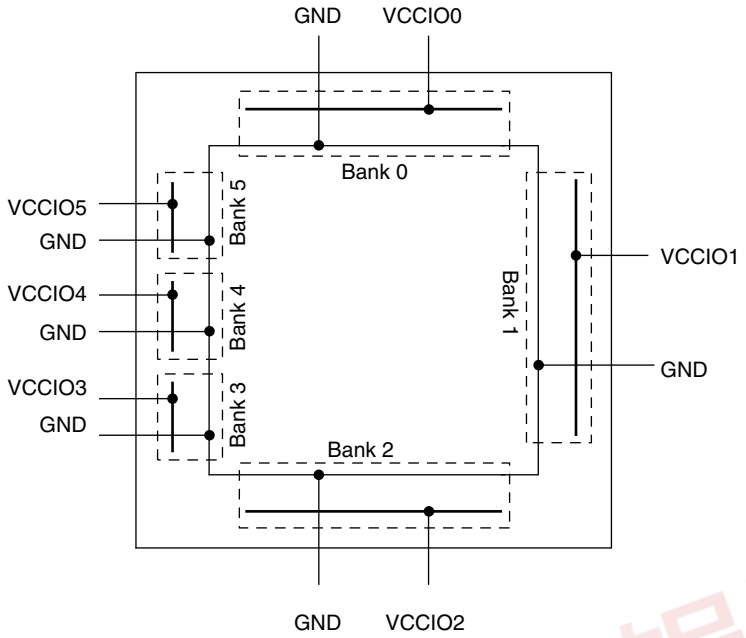
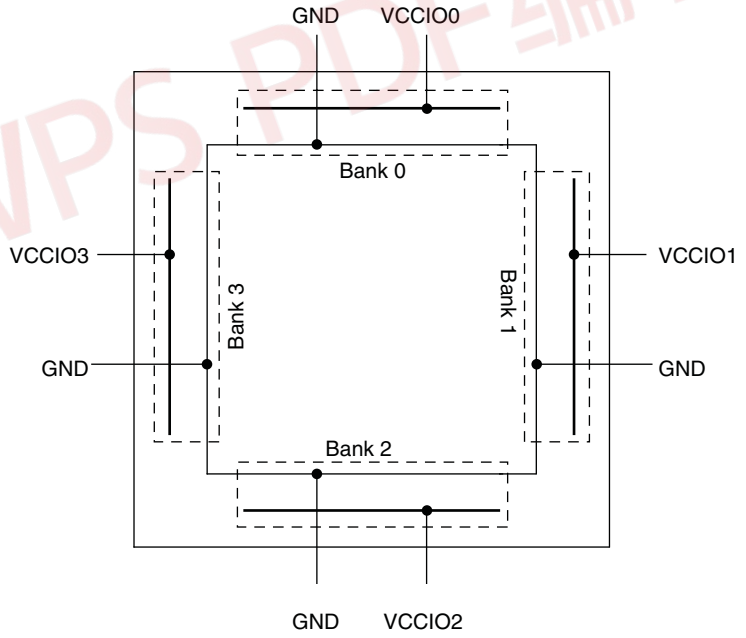


Figure 2-19. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks



Hot Socketing

The MachXO2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO2 ideal for many multiple power supply and hot-swap applications.

On-chip Oscillator

Every MachXO2 device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
2. During configuration, users select a different master clock frequency.
3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-14 lists all the available MCLK frequencies.

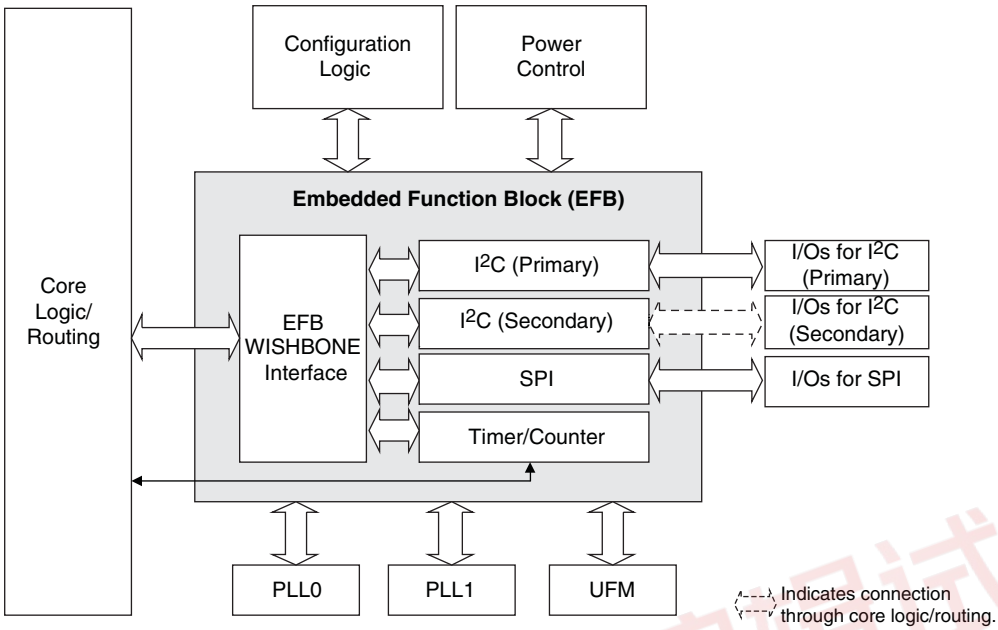
Table 2-14. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

Embedded Hardened IP Functions and User Flash Memory

All MachXO2 devices provide embedded hardened functions such as SPI, I^2C and Timer/Counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2-20.

Figure 2-20. Embedded Function Block Interface



Hardened I²C IP Core

Every MachXO2 device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I²C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface

Figure 2-21. I²C Core Block Diagram

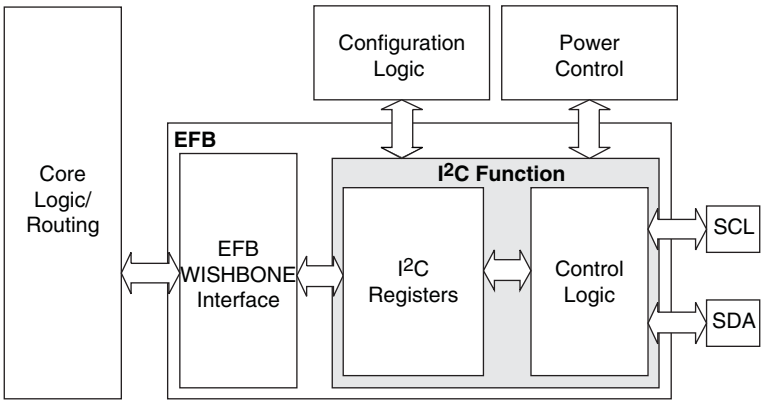


Table 2-15 describes the signals interfacing with the I²C cores.

Table 2-15. I²C Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I²C core. The signal is an output if the I²C core is in master mode. The signal is an input if the I²C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device.
i2c_sda	Bi-directional	Bi-directional data line of the I²C core. The signal is an output when data is transmitted from the I²C core. The signal is an input when data is received into the I²C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device.
i2c_irqo	Output	Interrupt request output signal of the I²C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I²C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.

Hardened SPI IP Core

Every MachXO2 device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO2 devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface

There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology (Appendix B)
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices

Figure 2-22. SPI Core Block Diagram

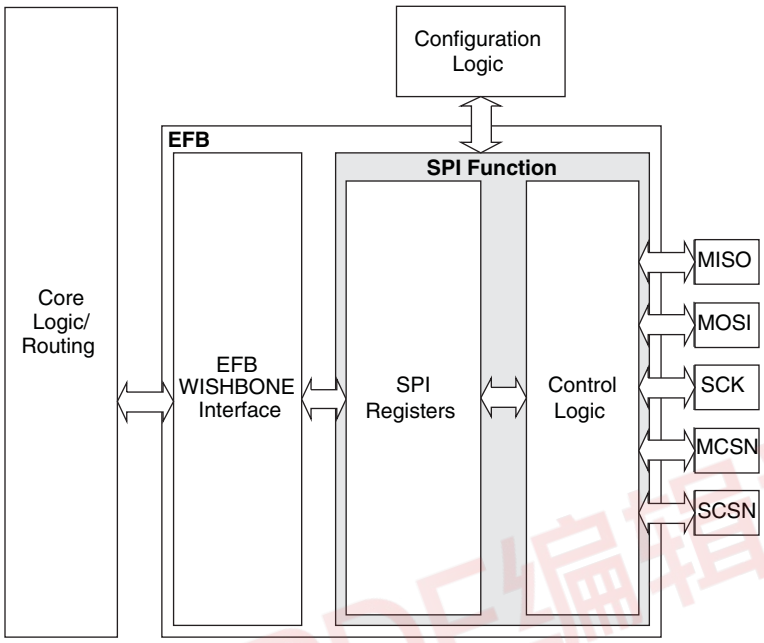


Table 2-16 describes the signals interfacing with the SPI cores.

Table 2-16. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	O	Master	SPI master chip-select output
spi_csn[1..7]	O	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	O	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
ufm_sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the User Flash Memory (UFM).
cfg_stdby	O	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.
cfg_wake	O	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.

Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  - — Watchdog timer
  - — Clear timer on compare match
  - — Fast PWM
  - — Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

Figure 2-23. Timer/Counter Block Diagram

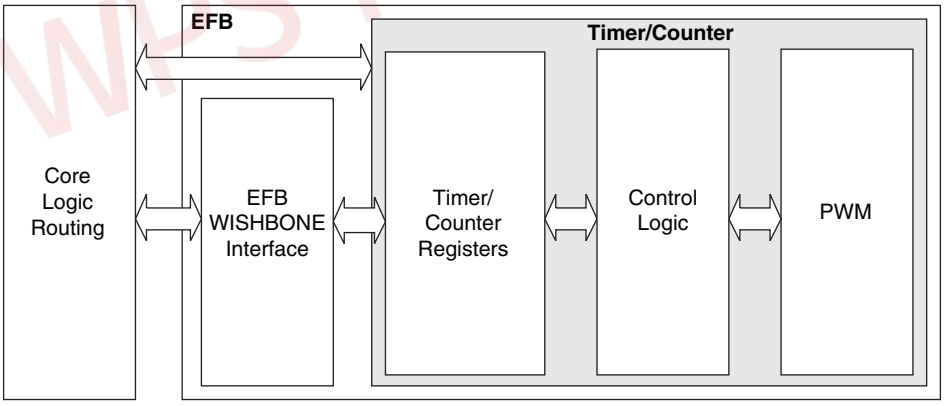


Table 2-17. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	O	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	O	Timer counter output signal

For more details on these embedded functions, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

User Flash Memory (UFM)

MachXO2-640/U and higher density devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I^2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

Standby Mode and Power Saving Options

MachXO2 devices are available in three options for maximum flexibility: ZE, HC and HE devices. The ZE devices have ultra low static and dynamic power consumption. These devices use a 1.2 V core voltage that further reduces power consumption. The HC and HE devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the HE devices operate at 1.2 V V_{CC}.

MachXO2 devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO2 devices support an ultra low power Stand-by mode. While most of these features are available in all three device types, these features are mainly intended for use with MachXO2 ZE devices to manage power consumption.

In the stand-by mode the MachXO2 devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I^2C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO2 devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

Table 2-18. MachXO2 Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe V_{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1198, Power Estimation and Management for MachXO2 Devices.

Power On Reset

MachXO2 devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the V_{PORUP} level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices), V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators (HC devices), V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time ($t_{REFRESH}$) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tristate. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min) they should not shut down the bandgap or POR circuit.

Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I^2C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

1. Internal Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I^2C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, MachXO2 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

TransFR (Transparent Field Reconfiguration)
TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

When implementing background programming of the on-chip Flash, care must be taken for the operation of the PLL. For devices that have two PLLs (XO2-2000U, -4000 and -7000), the system must put the RPLL (Right-side PLL) in reset state during the background Flash programming. More detailed description can be found in TN1204, MachXO2 Programming and Configuration Usage Guide.

Security and One-Time Programmable Mode (OTP)
For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO2 devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile Flash memory spaces. The device can be in one of two modes:

1. Unlocked – Readback of the SRAM configuration and non-volatile Flash memory spaces is allowed.

2. Permanently Locked – The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Dual Boot
MachXO2 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the on-chip Flash. The golden image MUST reside in an external SPI Flash. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Soft Error Detection
The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1206, MachXO2 Soft Error Detection Usage Guide.

TraceID

Each MachXO2 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I^2C, or JTAG interfaces.

Density Shifting

The MachXO2 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO2 migration files.

MachXO2 Family Data Sheet DC and Switching Characteristics

March 2017 Data Sheet DS1035

Absolute Maximum Ratings[1, 2, 3]

	MachXO2 ZE/HE (1.2 V)	MachXO2 HC (2.5 V / 3.3 V)
Supply Voltage V_{CC}	–0.5 V to 1.32 V	–0.5 V to 3.75 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied[4, 5]	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied[4]	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T_J)	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to (V_{IHMAX} + 2) volts is permitted for a duration of <20 ns.
5. The dual function I^2C pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.

Recommended Operating Conditions[1]

Symbol	Parameter	Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V / 3.3 V Devices	2.375	3.6	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	1.14	3.6	V
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature Industrial Operation	–40	100	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

Power Supply Ramp Rates[1]

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.01	—	100	V/ms

1. Assumes monotonic ramp rates.

Power-On-Reset Voltage Levels[1, 2, 3, 4, 5]

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and V_{CCIO0})	0.9	—	1.06	V
$V_{PORUPEXT}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	—	2.1	V
$V_{PORDNBG}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CCINT})	0.75	—	0.93	V
$V_{PORDNBGEXT}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	—	1.33	V
$V_{PORDNSRAM}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CCINT})	—	0.6	—	V
$V_{PORDNSRAMEXT}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	—	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.
3. Note that V_{PORUP} (min.) and $V_{PORDNBG}$ (max.) are in different process corners. For any given process corner $V_{PORDNBG}$ (max.) is always 12.0 mV below V_{PORUP} (min.).
4. $V_{PORUPEXT}$ is for HC devices only. In these devices a separate POR circuit monitors the external V_{CC} power supply.
5. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

Programming/Erase Specifications

Symbol	Parameter	Min.	Max.[1]	Units
$N_{PROGCYC}$	Flash Programming cycles per $t_{RETENTION}$	—	10,000	Cycles
	Flash functional programming cycles	—	100,000	
$t_{RETENTION}$	Data retention at 100 °C junction temperature	10	—	Years
	Data retention at 85 °C junction temperature	20	—	

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Max.	Units
I_{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/–1000	µA

1. Insensitive to sequence of V_{CC} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO}.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

ESD Performance

Please refer to the MachXO2 Product Family Qualification Summary for complete qualification data, including ESD performance.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4]	Input or I/O Leakage	Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX)	—	—	+175	µA
		Clamp OFF and $V_{IN} = V_{CCIO}$	–10	—	10	µA
		Clamp OFF and V_{CCIO} –0.97 V < V_{IN} < V_{CCIO}	–175	—	—	µA
		Clamp OFF and 0 V < V_{IN} < V_{CCIO} –0.97 V	—	—	10	µA
		Clamp OFF and V_{IN} = GND	—	—	10	µA
		Clamp ON and 0 V < V_{IN} < V_{CCIO}	—	—	10	µA
I_{PU}	I/O Active Pull-up Current	0 < V_{IN} < 0.7 V_{CCIO}	–30	—	-309	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) < V_{IN} < V_{CCIO}	30	—	305	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	–30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	305	µA
I_{BHHO}	Bus Hold High Overdrive current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	–309	µA
V_{BHT}[3]	Bus Hold Trip Points		V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	3	5	9	pF
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	3	5.5	7	pF
V_{HYST}	Hysteresis for Schmitt Trigger Inputs[5]	V_{CCIO} = 3.3 V, Hysteresis = Large	—	450	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Large	—	250	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Large	—	125	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Large	—	100	—	mV
		V_{CCIO} = 3.3 V, Hysteresis = Small	—	250	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Small	—	150	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Small	—	60	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Small	—	40	—	mV

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. When V_{IH} is higher than V_{CCIO}, a transient current typically of 30 ns in duration or less with a peak current of 6 mA can occur on the high-to-low transition. For true LVDS output pins in MachXO2-640U, MachXO2-1200/U and larger devices, V_{IH} must be less than or equal to V_{CCIO}.
5. With bus keeper circuit turned on. For more details, refer to TN1202, MachXO2 sysIO Usage Guide.

Static Supply Current – ZE Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO2-256ZE	18	µA
		LCMXO2-640ZE	28	µA
		LCMXO2-1200ZE	56	µA
		LCMXO2-2000ZE	80	µA
		LCMXO2-4000ZE	124	µA
		LCMXO2-7000ZE	189	µA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	1	µA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off. To estimate the impact of turning each of these items on, please refer to the following table or for more detail with your specific design use the Power Calculator tool.
3. Frequency = 0 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Static Power Consumption Contribution of Different Components – ZE Devices

The table below can be used for approximating static power consumption. For a more accurate power analysis for your design please use the Power Calculator tool.

Symbol	Parameter	Typ.	Units
I_{DCBG}	Bandgap DC power contribution	101	µA
I_{DCPOR}	POR DC power contribution	38	µA
$I_{DCIOBANKCONTROLLER}$	DC power contribution per I/O bank controller	143	µA

Static Supply Current – HC/HE Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO2-256HC	1.15	mA
		LCMXO2-640HC	1.84	mA
		LCMXO2-640UHC	3.48	mA
		LCMXO2-1200HC	3.49	mA
		LCMXO2-1200UHC	4.80	mA
		LCMXO2-2000HC	4.80	mA
		LCMXO2-2000UHC	8.44	mA
		LCMXO2-4000HC	8.45	mA
		LCMXO2-7000HC	12.87	mA
		LCMXO2-2000HE	1.39	mA
		LCMXO2-4000HE	2.55	mA
		LCMXO2-7000HE	4.06	mA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
3. Frequency = 0 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Programming and Erase Flash Supply Current – HC/HE Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO2-256HC	14.6	mA
		LCMXO2-640HC	16.1	mA
		LCMXO2-640UHC	18.8	mA
		LCMXO2-1200HC	18.8	mA
		LCMXO2-1200UHC	22.1	mA
		LCMXO2-2000HC	22.1	mA
		LCMXO2-2000UHC	26.8	mA
		LCMXO2-4000HC	26.8	mA
		LCMXO2-7000HC	33.2	mA
		LCMXO2-2000HE	18.3	mA
		LCMXO2-2000UHE	20.4	mA
		LCMXO2-4000HE	20.4	mA
		LCMXO2-7000HE	23.9	mA
I_{CCIO}	Bank Power Supply[6]	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. T_J = 25 °C, power supplies at nominal voltage.
6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

Programming and Erase Flash Supply Current – ZE Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO2-256ZE	13	mA
		LCMXO2-640ZE	14	mA
		LCMXO2-1200ZE	15	mA
		LCMXO2-2000ZE	17	mA
		LCMXO2-4000ZE	18	mA
		LCMXO2-7000ZE	20	mA
I_{CCIO}	Bank Power Supply[6]	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. TJ = 25 °C, power supplies at nominal voltage.
6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.6	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.6	—	—	—
PCI[3]	3.135	3.3	3.6	—	—	—
SSTL25	2.375	2.5	2.625	1.15	1.25	1.35
SSTL18	1.71	1.8	1.89	0.833	0.9	0.969
HSTL18	1.71	1.8	1.89	0.816	0.9	1.08
LVCMOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVCMOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVCMOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVCMOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVCMOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVCMOS12R33[4]	3.135	3.3	3.6	0.45	0.6	0.75
LVCMOS12R25[4]	2.375	2.5	2.625	0.45	0.6	0.75
LVCMOS10R33[4]	3.135	3.3	3.6	0.35	0.5	0.65
LVCMOS10R25[4]	2.375	2.5	2.625	0.35	0.5	0.65
LVDS25[1, 2]	2.375	2.5	2.625	—	—	—
LVDS33[1, 2]	3.135	3.3	3.6	—	—	—
LVPECL[1]	3.135	3.3	3.6	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—
RSDS[1]	2.375	2.5	2.625	—	—	—
SSTL18D	1.71	1.8	1.89	—	—	—
SSTL25D	2.375	2.5	2.625	—	—	—
HSTL18D	1.71	1.8	1.89	—	—	—

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
3. Input on the bottom bank of the MachXO2-640U, MachXO2-1200/U and larger devices only.
4. Supported only for inputs and BIDIs for all ZE devices, and –6 speed grade for HE and HC devices.

sysIO Single-Ended DC Electrical Characteristics[1, 2]

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max.[4] (mA)	I_{OH} Max.[4] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3 LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
							16	–16
							24	–24
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
							16	–16
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.5	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.2	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} – 0.4	4	–2
							8	–6
					0.2	V_{CCIO} – 0.2	0.1	–0.1
PCI	–0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	–0.5
SSTL25 Class I	–0.3	V_{REF} – 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	8	8
SSTL25 Class II	–0.3	V_{REF} – 0.18	V_{REF} + 0.18	3.6	NA	NA	NA	NA
SSTL18 Class I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	3.6	0.40	V_{CCIO} - 0.40	8	8
SSTL18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	3.6	NA	NA	NA	NA
HSTL18 Class I	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	V_{CCIO} - 0.40	8	8
HSTL18 Class II	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS25R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS12R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max.[4] (mA)	I_{OH} Max.[4] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS10R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain

1. MachXO2 devices allow LVCMOS inputs to be placed in I/O banks where V_{CCIO} is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO2 devices do not meet the relevant JEDEC specification are documented in the table below.
2. MachXO2 devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1202, MachXO2 sysIO Usage Guide.
3. The dual function I^2C pins SCL and SDA are limited to a V_{IL} min of –0.25 V or to –0.3 V with a duration of <10 ns.
4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive VCCIO or GND pad connections, or between the last VCCIO or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n * 8 mA. “n” is the number of I/O pads between the two consecutive bank VCCIO or GND connections or between the last VCCIO and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

Input Standard	V_{CCIO} (V)	V_{IL} Max. (V)
LVCMOS 33	1.5	0.685
LVCMOS 25	1.5	0.687
LVCMOS 18	1.5	0.655

sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of MachXO2-640U, MachXO2-1200/U and higher density devices in the MachXO2 PLD family.

LVDS

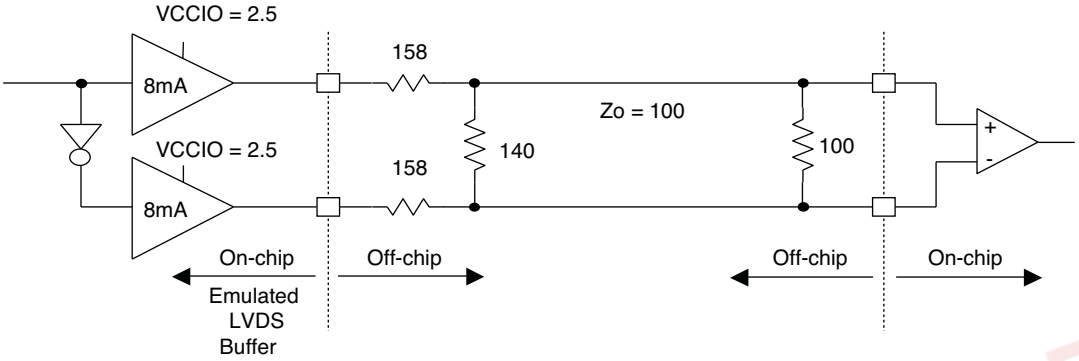
Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO} = 3.3 V	0	—	2.605	V
		V_{CCIO} = 2.5 V	0	—	2.05	V
V_{THD}	Differential Input Threshold		±100	—		mV
V_{CM}	Input Common Mode Voltage	V_{CCIO} = 3.3 V	0.05	—	2.6	V
		V_{CCIO} = 2.5 V	0.05	—	2.0	V
I_{IN}	Input current	Power on	—	—	±10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.375	—	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.90	1.025	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.395	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0 V driver outputs shorted	—	—	24	mA

LVDS Emulation

MachXO2 devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

Figure 3-1. LVDS Using External Resistors (LVDS25E)



Note: All resistors are ±1%.

Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	158	Ohms
R_P	Driver parallel resistor	140	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	6.03	mA

BLVDS

The MachXO2 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

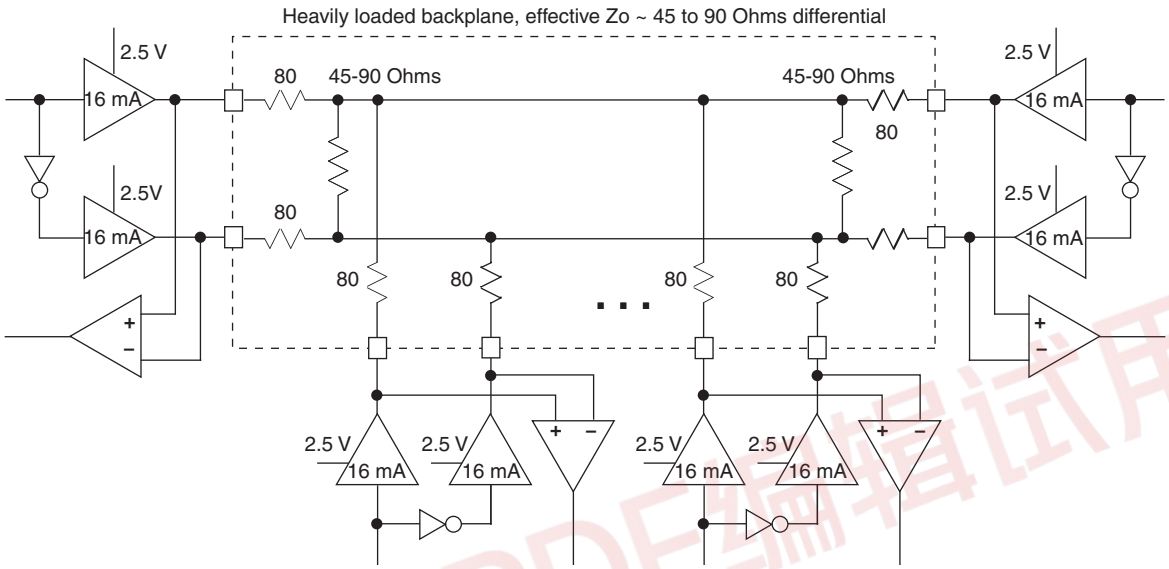


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	20	20	Ohms
R_S	Driver series resistance	80	80	Ohms
R_{TLEFT}	Left end termination	45	90	Ohms
R_{TRIGHT}	Right end termination	45	90	Ohms
V_{OH}	Output high voltage	1.376	1.480	V
V_{OL}	Output low voltage	1.124	1.020	V
V_{OD}	Output differential voltage	0.253	0.459	V
V_{CM}	Output common mode voltage	1.250	1.250	V
I_{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.

LVPECL

The MachXO2 family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

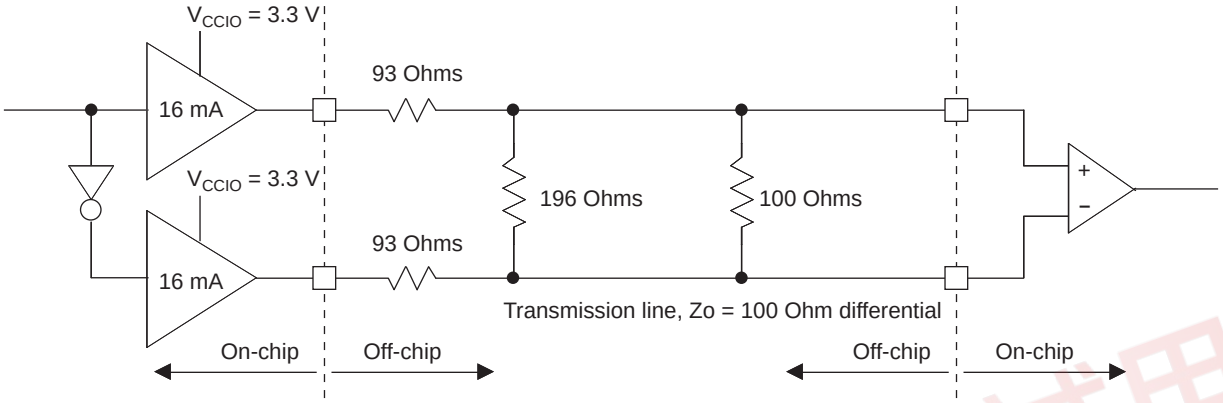


Table 3-3. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	93	Ohms
R_P	Driver parallel resistor	196	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	2.05	V
V_{OL}	Output low voltage	1.25	V
V_{OD}	Output differential voltage	0.80	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	12.11	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

RSDS

The MachXO2 family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

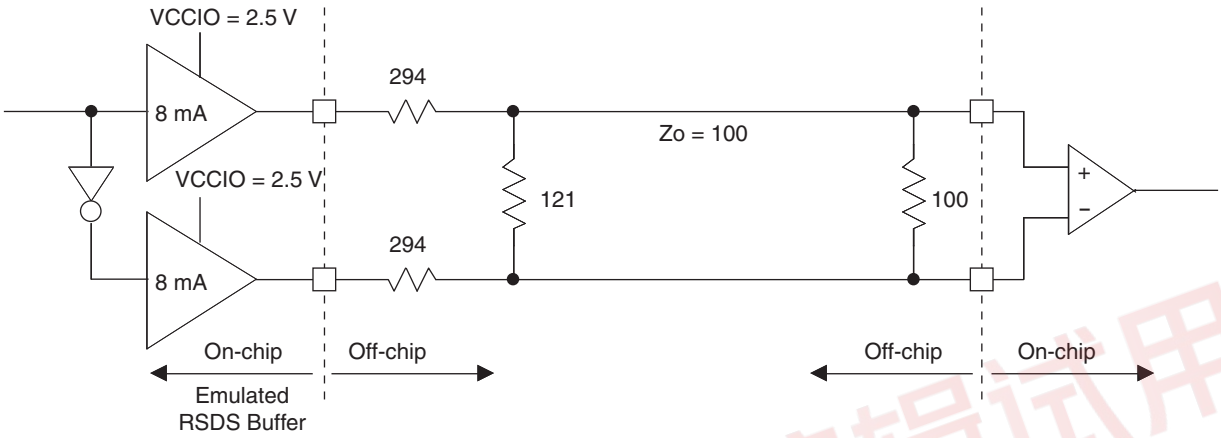


Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	294	Ohms
R_P	Driver parallel resistor	121	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	Ohms
I_{DC}	DC output current	3.66	mA

Typical Building Block Function Performance – HC/HE Devices[1]

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	-6 Timing	Units
Basic Functions		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

Register-to-Register Performance

Function	-6 Timing	Units
Basic Functions		
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

Typical Building Block Function Performance – ZE Devices[1]

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–3 Timing	Units
Basic Functions		
16-bit decoder	13.9	ns
4:1 MUX	10.9	ns
16:1 MUX	12.0	ns

Register-to-Register Performance

Function	–3 Timing	Units
Basic Functions		
16:1 MUX	191	MHz
16-bit adder	134	MHz
16-bit counter	148	MHz
64-bit counter	77	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	90	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	214	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
LVDS25	400	MHz
LVDS25E	150	MHz
RSDS25	150	MHz
RSDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
SSTL25_I	150	MHz
SSTL25_II	150	MHz
SSTL25D_I	150	MHz
SSTL25D_II	150	MHz
SSTL18_I	150	MHz
SSTL18_II	150	MHz
SSTL18D_I	150	MHz
SSTL18D_II	150	MHz
HSTL18_I	150	MHz
HSTL18_II	150	MHz
HSTL18D_I	150	MHz
HSTL18D_II	150	MHz
PCI33	134	MHz
LVTTL33	150	MHz
LVTTL33D	150	MHz
LVCMOS33	150	MHz
LVCMOS33D	150	MHz
LVCMOS25	150	MHz
LVCMOS25D	150	MHz
LVCMOS25R33	150	MHz
LVCMOS18	150	MHz
LVCMOS18D	150	MHz
LVCMOS18R33	150	MHz
LVCMOS18R25	150	MHz
LVCMOS15	150	MHz
LVCMOS15D	150	MHz
LVCMOS15R33	150	MHz
LVCMOS15R25	150	MHz
LVCMOS12	91	MHz
LVCMOS12D	91	MHz

MachXO2 External Switching Characteristics – HC/HE Devices[1, 2, 3, 4, 5, 6, 7]

Over Recommended Operating Conditions

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f_{MAX_PRI}[8]	Frequency for Primary Clock Tree	All MachXO2 devices	—	388	—	323	—	269	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	0.5	—	0.6	—	0.7	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO2-256HC-HE	—	912	—	939	—	975	ps
		MachXO2-640HC-HE	—	844	—	871	—	908	ps
		MachXO2-1200HC-HE	—	868	—	902	—	951	ps
		MachXO2-2000HC-HE	—	867	—	897	—	941	ps
		MachXO2-4000HC-HE	—	865	—	892	—	931	ps
		MachXO2-7000HC-HE	—	902	—	942	—	989	ps
Edge Clock									
f_{MAX_EDGE}[8]	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	400	—	333	—	278	MHz
Pin-LUT-Pin Propagation Delay									
t_{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	—	6.72	—	6.96	—	7.24	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t_{CO}	Clock to Output – PIO Output Register	MachXO2-256HC-HE	—	7.13	—	7.30	—	7.57	ns
		MachXO2-640HC-HE	—	7.15	—	7.30	—	7.57	ns
		MachXO2-1200HC-HE	—	7.44	—	7.64	—	7.94	ns
		MachXO2-2000HC-HE	—	7.46	—	7.66	—	7.96	ns
		MachXO2-4000HC-HE	—	7.51	—	7.71	—	8.01	ns
		MachXO2-7000HC-HE	—	7.54	—	7.75	—	8.06	ns
t_{SU}	Clock to Data Setup – PIO Input Register	MachXO2-256HC-HE	–0.06	—	–0.06	—	–0.06	—	ns
		MachXO2-640HC-HE	–0.06	—	–0.06	—	–0.06	—	ns
		MachXO2-1200HC-HE	–0.17	—	–0.17	—	–0.17	—	ns
		MachXO2-2000HC-HE	–0.20	—	–0.20	—	–0.20	—	ns
		MachXO2-4000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-7000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	MachXO2-256HC-HE	1.75	—	1.95	—	2.16	—	ns
		MachXO2-640HC-HE	1.75	—	1.95	—	2.16	—	ns
		MachXO2-1200HC-HE	1.88	—	2.12	—	2.36	—	ns
		MachXO2-2000HC-HE	1.89	—	2.13	—	2.37	—	ns
		MachXO2-4000HC-HE	1.94	—	2.18	—	2.43	—	ns
		MachXO2-7000HC-HE	1.98	—	2.23	—	2.49	—	ns

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-256HC-HE	1.42	—	1.59	—	1.96	—	ns
		MachXO2-640HC-HE	1.41	—	1.58	—	1.96	—	ns
		MachXO2-1200HC-HE	1.63	—	1.79	—	2.17	—	ns
		MachXO2-2000HC-HE	1.61	—	1.76	—	2.13	—	ns
		MachXO2-4000HC-HE	1.66	—	1.81	—	2.19	—	ns
		MachXO2-7000HC-HE	1.53	—	1.67	—	2.03	—	ns
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-256HC-HE	–0.24	—	–0.24	—	–0.24	—	ns
		MachXO2-640HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-1200HC-HE	–0.24	—	–0.24	—	–0.24	—	ns
		MachXO2-2000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000HC-HE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-7000HC-HE	–0.21	—	–0.21	—	–0.21	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices	—	388	—	323	—	269	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
t_{COE}	Clock to Output – PIO Output Register	MachXO2-1200HC-HE	—	7.53	—	7.76	—	8.10	ns
		MachXO2-2000HC-HE	—	7.53	—	7.76	—	8.10	ns
		MachXO2-4000HC-HE	—	7.45	—	7.68	—	8.00	ns
		MachXO2-7000HC-HE	—	7.53	—	7.76	—	8.10	ns
t_{SUE}	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
		MachXO2-2000HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
		MachXO2-4000HC-HE	–0.16	—	–0.16	—	–0.16	—	ns
		MachXO2-7000HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
t_{HE}	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	1.97	—	2.24	—	2.52	—	ns
		MachXO2-2000HC-HE	1.97	—	2.24	—	2.52	—	ns
		MachXO2-4000HC-HE	1.89	—	2.16	—	2.43	—	ns
		MachXO2-7000HC-HE	1.97	—	2.24	—	2.52	—	ns
t_{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	1.56	—	1.69	—	2.05	—	ns
		MachXO2-2000HC-HE	1.56	—	1.69	—	2.05	—	ns
		MachXO2-4000HC-HE	1.74	—	1.88	—	2.25	—	ns
		MachXO2-7000HC-HE	1.66	—	1.81	—	2.17	—	ns
t_{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-2000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000HC-HE	–0.34	—	–0.34	—	–0.34	—	ns
		MachXO2-7000HC-HE	–0.29	—	–0.29	—	–0.29	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t_{COPLL}	Clock to Output – PIO Output Register	MachXO2-1200HC-HE	—	5.97	—	6.00	—	6.13	ns
		MachXO2-2000HC-HE	—	5.98	—	6.01	—	6.14	ns
		MachXO2-4000HC-HE	—	5.99	—	6.02	—	6.16	ns
		MachXO2-7000HC-HE	—	6.02	—	6.06	—	6.20	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	0.36	—	0.36	—	0.65	—	ns
		MachXO2-2000HC-HE	0.36	—	0.36	—	0.63	—	ns
		MachXO2-4000HC-HE	0.35	—	0.35	—	0.62	—	ns
		MachXO2-7000HC-HE	0.34	—	0.34	—	0.59	—	ns

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HPLL}	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	0.41	—	0.48	—	0.55	—	ns
		MachXO2-2000HC-HE	0.42	—	0.49	—	0.56	—	ns
		MachXO2-4000HC-HE	0.43	—	0.50	—	0.58	—	ns
		MachXO2-7000HC-HE	0.46	—	0.54	—	0.62	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	2.88	—	3.19	—	3.72	—	ns
		MachXO2-2000HC-HE	2.87	—	3.18	—	3.70	—	ns
		MachXO2-4000HC-HE	2.96	—	3.28	—	3.81	—	ns
		MachXO2-7000HC-HE	3.05	—	3.35	—	3.87	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-2000HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-4000HC-HE	–0.87	—	–0.87	—	–0.87	—	ns
		MachXO2-7000HC-HE	–0.91	—	–0.91	—	–0.91	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.317	—	0.344	—	0.368	UI
t_{DVE}	Input Data Hold After CLK		0.742	—	0.702	—	0.668	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	All MachXO2 devices, all sides	0.566	—	0.560	—	0.538	—	ns
t_{HO}	Input Data Hold After CLK		0.778	—	0.879	—	1.090	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.316	—	0.342	—	0.364	UI
t_{DVE}	Input Data Hold After CLK		0.710	—	0.675	—	0.679	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.233	—	0.219	—	0.198	—	ns
t_{HO}	Input Data Hold After CLK		0.287	—	0.287	—	0.344	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only.[11]	—	0.290	—	0.320	—	0.345	UI
t_{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	0.703	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only.[11]	0.233	—	0.219	—	0.198	—	ns
t_{HO}	Input Data Hold After ECLK		0.287	—	0.287	—	0.344	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1)[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only.[11]	—	0.290	—	0.320	—	0.345	UI
t_{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	0.703	—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	All MachXO2 devices, all sides.	—	0.520	—	0.550	—	0.580	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.520	—	0.550	—	0.580	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK frequency		—	150	—	125	—	104	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	All MachXO2 devices, all sides.	1.210	—	1.510	—	1.870	—	ns
t_{DVA}	Output Data Valid After CLK Output		1.210	—	1.510	—	1.870	—	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		—	150	—	125	—	104	MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.535	—	0.670	—	0.830	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	0.830	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.455	—	0.570	—	0.710	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.455	—	0.570	—	0.710	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[9, 12]									
t_{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.160	—	0.180	—	0.200	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.160	—	0.180	—	0.200	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.369	—	0.395	—	0.421	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.529	—	0.530	—	0.527	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM LPDDR Serial Data Speed		—	280	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	140	—	125	—	104	MHz
f_{LPDDR}	LPDDR Data Transfer Rate		0	280	0	250	0	208	Mbps
DDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.350	—	0.387	—	0.414	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.545	—	0.538	—	0.532	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	150	—	125	—	104	MHz
f_{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps
DDR2[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.360	—	0.378	—	0.406	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.555	—	0.549	—	0.542	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	150	—	125	—	104	MHz
f_{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
7. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps (–6), 113 ps (–5), 120 ps (–4).
8. This number for general purpose usage. Duty cycle tolerance is +/– 10%.
9. Duty cycle is +/–5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32 QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

MachXO2 External Switching Characteristics – ZE Devices[1, 2, 3, 4, 5, 6, 7]

Over Recommended Operating Conditions

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f_{MAX_PRI}[8]	Frequency for Primary Clock Tree	All MachXO2 devices	—	150	—	125	—	104	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	1.00	—	1.20	—	1.40	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO2-256ZE	—	1250	—	1272	—	1296	ps
		MachXO2-640ZE	—	1161	—	1183	—	1206	ps
		MachXO2-1200ZE	—	1213	—	1267	—	1322	ps
		MachXO2-2000ZE	—	1204	—	1250	—	1296	ps
		MachXO2-4000ZE	—	1195	—	1233	—	1269	ps
		MachXO2-7000ZE	—	1243	—	1268	—	1296	ps
Edge Clock									
f_{MAX_EDGE}[8]	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	210	—	175	—	146	MHz
Pin-LUT-Pin Propagation Delay									
t_{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	—	9.35	—	9.78	—	10.21	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t_{CO}	Clock to Output – PIO Output Register	MachXO2-256ZE	—	10.46	—	10.86	—	11.25	ns
		MachXO2-640ZE	—	10.52	—	10.92	—	11.32	ns
		MachXO2-1200ZE	—	11.24	—	11.68	—	12.12	ns
		MachXO2-2000ZE	—	11.27	—	11.71	—	12.16	ns
		MachXO2-4000ZE	—	11.28	—	11.78	—	12.28	ns
		MachXO2-7000ZE	—	11.22	—	11.76	—	12.30	ns
t_{SU}	Clock to Data Setup – PIO Input Register	MachXO2-256ZE	–0.21	—	–0.21	—	–0.21	—	ns
		MachXO2-640ZE	–0.22	—	–0.22	—	–0.22	—	ns
		MachXO2-1200ZE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-2000ZE	–0.27	—	–0.27	—	–0.27	—	ns
		MachXO2-4000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-7000ZE	–0.33	—	–0.33	—	–0.33	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	MachXO2-256ZE	3.96	—	4.25	—	4.65	—	ns
		MachXO2-640ZE	4.01	—	4.31	—	4.71	—	ns
		MachXO2-1200ZE	3.95	—	4.29	—	4.73	—	ns
		MachXO2-2000ZE	3.94	—	4.29	—	4.74	—	ns
		MachXO2-4000ZE	3.96	—	4.36	—	4.87	—	ns
		MachXO2-7000ZE	3.93	—	4.37	—	4.91	—	ns

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-256ZE	2.62	—	2.91	—	3.14	—	ns
		MachXO2-640ZE	2.56	—	2.85	—	3.08	—	ns
		MachXO2-1200ZE	2.30	—	2.57	—	2.79	—	ns
		MachXO2-2000ZE	2.25	—	2.50	—	2.70	—	ns
		MachXO2-4000ZE	2.39	—	2.60	—	2.76	—	ns
		MachXO2-7000ZE	2.17	—	2.33	—	2.43	—	ns
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-256ZE	–0.44	—	–0.44	—	–0.44	—	ns
		MachXO2-640ZE	–0.43	—	–0.43	—	–0.43	—	ns
		MachXO2-1200ZE	–0.28	—	–0.28	—	–0.28	—	ns
		MachXO2-2000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-4000ZE	–0.34	—	–0.34	—	–0.34	—	ns
		MachXO2-7000ZE	–0.21	—	–0.21	—	–0.21	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices	—	150	—	125	—	104	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
t_{COE}	Clock to Output – PIO Output Register	MachXO2-1200ZE	—	11.10	—	11.51	—	11.91	ns
		MachXO2-2000ZE	—	11.10	—	11.51	—	11.91	ns
		MachXO2-4000ZE	—	10.89	—	11.28	—	11.67	ns
		MachXO2-7000ZE	—	11.10	—	11.51	—	11.91	ns
t_{SUE}	Clock to Data Setup – PIO Input Register	MachXO2-1200ZE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-2000ZE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000ZE	–0.15	—	–0.15	—	–0.15	—	ns
		MachXO2-7000ZE	–0.23	—	–0.23	—	–0.23	—	ns
t_{HE}	Clock to Data Hold – PIO Input Register	MachXO2-1200ZE	3.81	—	4.11	—	4.52	—	ns
		MachXO2-2000ZE	3.81	—	4.11	—	4.52	—	ns
		MachXO2-4000ZE	3.60	—	3.89	—	4.28	—	ns
		MachXO2-7000ZE	3.81	—	4.11	—	4.52	—	ns
t_{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200ZE	2.78	—	3.11	—	3.40	—	ns
		MachXO2-2000ZE	2.78	—	3.11	—	3.40	—	ns
		MachXO2-4000ZE	3.11	—	3.48	—	3.79	—	ns
		MachXO2-7000ZE	2.94	—	3.30	—	3.60	—	ns
t_{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200ZE	–0.29	—	-0.29	—	–0.29	—	ns
		MachXO2-2000ZE	–0.29	—	-0.29	—	–0.29	—	ns
		MachXO2-4000ZE	–0.46	—	-0.46	—	–0.46	—	ns
		MachXO2-7000ZE	–0.37	—	-0.37	—	–0.37	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t_{COPLL}	Clock to Output – PIO Output Register	MachXO2-1200ZE	—	7.95	—	8.07	—	8.19	ns
		MachXO2-2000ZE	—	7.97	—	8.10	—	8.22	ns
		MachXO2-4000ZE	—	7.98	—	8.10	—	8.23	ns
		MachXO2-7000ZE	—	8.02	—	8.14	—	8.26	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO2-1200ZE	0.85	—	0.85	—	0.89	—	ns
		MachXO2-2000ZE	0.84	—	0.84	—	0.86	—	ns
		MachXO2-4000ZE	0.84	—	0.84	—	0.85	—	ns
		MachXO2-7000ZE	0.83	—	0.83	—	0.81	—	ns

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HPLL}	Clock to Data Hold – PIO Input Register	MachXO2-1200ZE	0.66	—	0.68	—	0.80	—	ns
		MachXO2-2000ZE	0.68	—	0.70	—	0.83	—	ns
		MachXO2-4000ZE	0.68	—	0.71	—	0.84	—	ns
		MachXO2-7000ZE	0.73	—	0.74	—	0.87	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200ZE	5.14	—	5.69	—	6.20	—	ns
		MachXO2-2000ZE	5.11	—	5.67	—	6.17	—	ns
		MachXO2-4000ZE	5.27	—	5.84	—	6.35	—	ns
		MachXO2-7000ZE	5.15	—	5.71	—	6.23	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200ZE	–1.36	—	–1.36	—	–1.36	—	ns
		MachXO2-2000ZE	–1.35	—	–1.35	—	–1.35	—	ns
		MachXO2-4000ZE	–1.43	—	–1.43	—	–1.43	—	ns
		MachXO2-7000ZE	–1.41	—	–1.41	—	–1.41	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.382	—	0.401	—	0.417	UI
t_{DVE}	Input Data Hold After CLK		0.670	—	0.684	—	0.693	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	All MachXO2 devices, all sides	1.319	—	1.412	—	1.462	—	ns
t_{HO}	Input Data Hold After CLK		0.717	—	1.010	—	1.340	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.361	—	0.346	—	0.334	UI
t_{DVE}	Input Data Hold After CLK		0.602	—	0.625	—	0.648	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.472	—	0.672	—	0.865	—	ns
t_{HO}	Input Data Hold After CLK		0.363	—	0.501	—	0.743	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input - GDDRX4_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.307	—	0.316	—	0.326	UI
t_{DVE}	Input Data Hold After ECLK		0.662	—	0.650	—	0.649	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.434	—	0.535	—	0.630	—	ns
t_{HO}	Input Data Hold After ECLK		0.385	—	0.395	—	0.463	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz
7:1 LVDS Inputs – GDDR71_RX.ECLK.7.1[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.307	—	0.316	—	0.326	UI
t_{DVE}	Input Data Hold After ECLK		0.662	—	0.650	—	0.649	—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	210	—	176	—	146	MHz
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	60	—	50	—	42	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	All MachXO2 devices, all sides	—	0.850	—	0.910	—	0.970	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.850	—	0.910	—	0.970	ns
f_{DATA}	DDRX1 Output Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK frequency		—	70	—	58	—	49	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	All MachXO2 devices, all sides	2.720	—	3.380	—	4.140	—	ns
t_{DVA}	Output Data Valid After CLK Output		2.720	—	3.380	—	4.140	—	ns
f_{DATA}	DDRX1 Output Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		—	70	—	58	—	49	MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	—	0.270	—	0.300	—	0.330	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.270	—	0.300	—	0.330	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	1.445	—	1.760	—	2.140	—	ns
t_{DVA}	Output Data Valid After CLK Output		1.445	—	1.760	—	2.140	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	—	0.270	—	0.300	—	0.330	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.270	—	0.300	—	0.330	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	0.873	—	1.067	—	1.319	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.873	—	1.067	—	1.319	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[9, 12]									
t_{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.240	—	0.270	—	0.300	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.240	—	0.270	—	0.300	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	420	—	352	—	292	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	210	—	176	—	146	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	60	—	50	—	42	MHz

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.349	—	0.381	—	0.396	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.630	—	0.613	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM LPDDR Serial Data Speed		—	120	—	110	—	96	Mbps
f_{SCLK}	SCLK Frequency		—	60	—	55	—	48	MHz
f_{LPDDR}	LPDDR Data Transfer Rate		0	120	0	110	0	96	Mbps
DDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.347	—	0.374	—	0.393	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.637	—	0.616	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f_{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f_{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps
DDR2[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.372	—	0.394	—	0.410	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.690	—	0.658	—	0.618	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f_{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f_{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
7. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 167 ps (–3), 182 ps (–2), 195 ps (–1).
8. This number for general purpose usage. Duty cycle tolerance is +/–10%.
9. Duty cycle is +/– 5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

Figure 3-5. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms

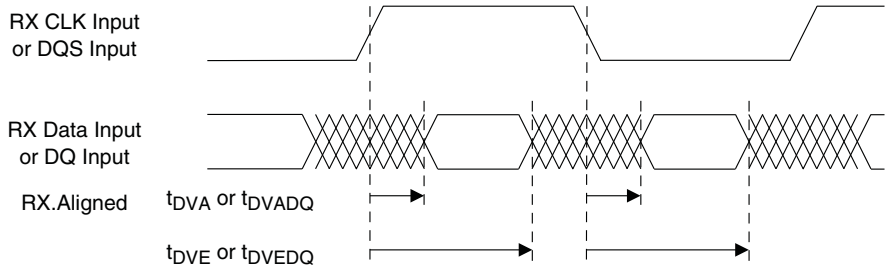


Figure 3-6. Receiver RX.CLK.Centered Waveforms

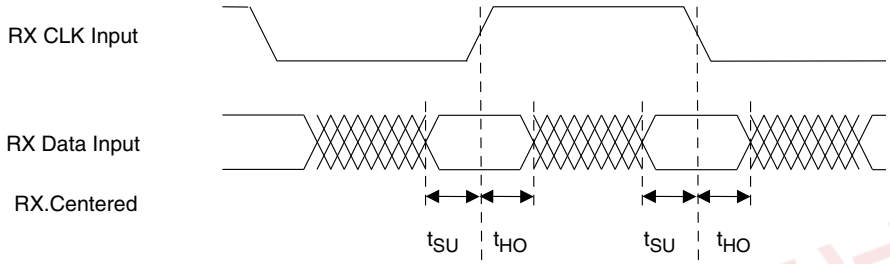


Figure 3-7. Transmitter TX.CLK.Aligned Waveforms

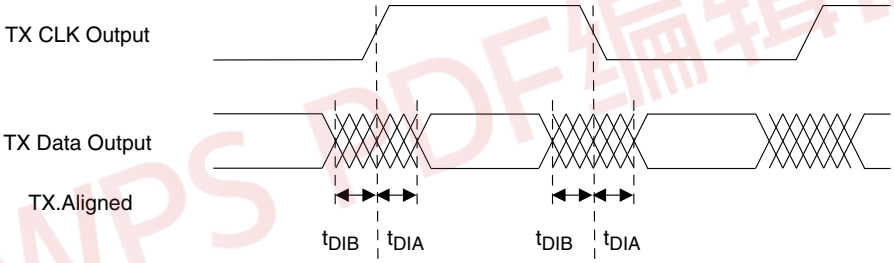


Figure 3-8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms

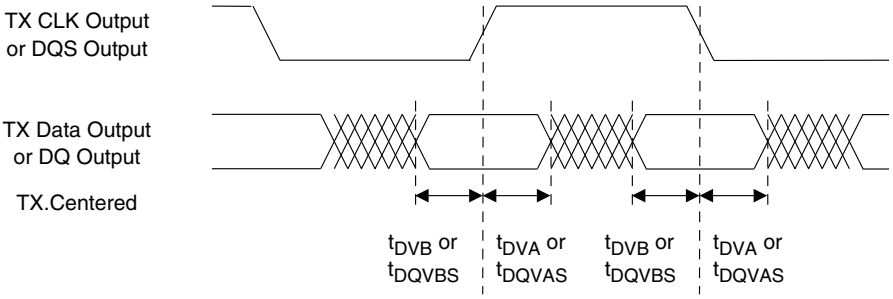


Figure 3-9. GDDR71 Video Timing Waveforms

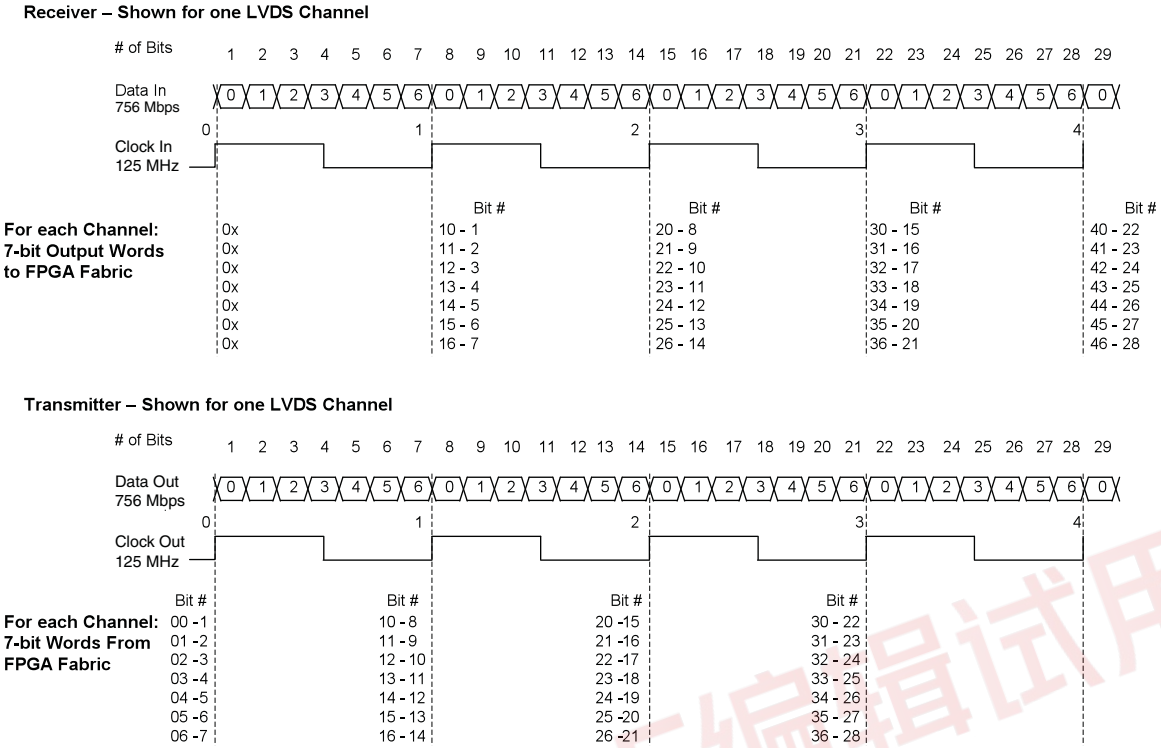


Figure 3-10. Receiver GDDR71_RX. Waveforms

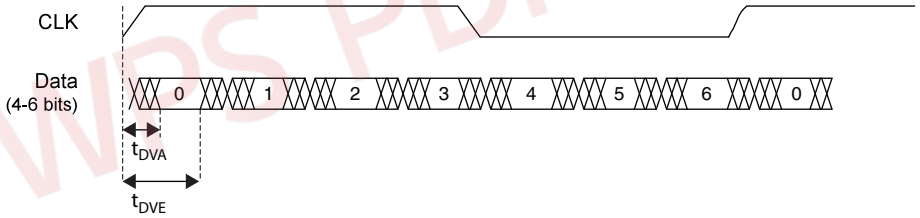
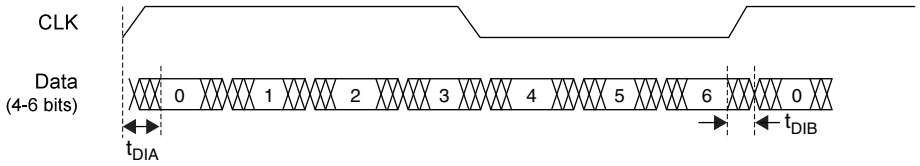


Figure 3-11. Transmitter GDDR71_TX. Waveforms



sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)		1.5625	400	MHz
f_{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f_{VCO}	PLL VCO Frequency		200	800	MHz
f_{PFD}	Phase Detector Input Frequency		7	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Without duty trim selected[3]	45	55	%
t_{DT_TRIM}[7]	Edge Duty Trim Accuracy		–75	75	%
t_{PH}[4]	Output Phase Accuracy		–6	6	%
t_{OPJIT}[1, 8]	Output Clock Period Jitter	f_{OUT} > 100 MHz	—	150	ps p-p
		f_{OUT} < 100 MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} > 100 MHz	—	180	ps p-p
		f_{OUT} < 100 MHz	—	0.009	UIPP
	Output Clock Phase Jitter	f_{PFD} > 100 MHz	—	160	ps p-p
		f_{PFD} < 100 MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	230	ps p-p
		f_{OUT} < 100 MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	230	ps p-p
		f_{OUT} < 100 MHz	—	0.12	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	–120	120	ps
t_W	Output Clock Pulse Width	At 90% or 10%[3]	0.9	—	ns
t_{LOCK}[2, 5]	PLL Lock-in Time		—	15	ms
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[6]	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{STABLE}[5]	STANDBY High to PLL Stable		—	15	ms
t_{RST}	RST/RESETM Pulse Width		1	—	ns
t_{RSTREC}	RST Recovery Time		1	—	ns
t_{RST_DIV}	RESETC/D Pulse Width		10	—	ns
t_{RSTREC_DIV}	RESETC/D Recovery Time		1	—	ns
$t_{ROTATE-SETUP}$	PHASESTEP Setup Time		10	—	ns

sysCLOCK PLL Timing (Continued)

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
t_{ROTATE_WD}	PHASESTEP Pulse Width		4	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide for more details.
5. At minimum $f_{PFD.}$ As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

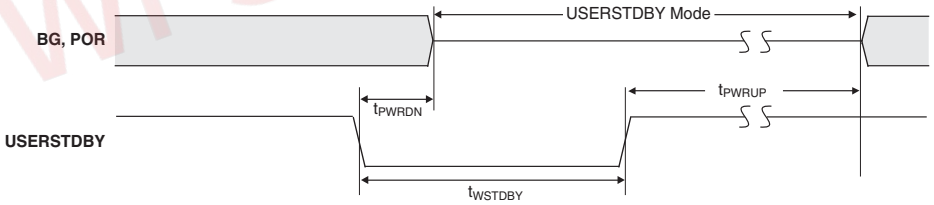
MachXO2 Oscillator Output Frequency

Symbol	Parameter	Min.	Typ.	Max	Units
f_{MAX}	Oscillator Output Frequency (Commercial Grade Devices, 0 to 85°C)	125.685	133	140.315	MHz
	Oscillator Output Frequency (Industrial Grade Devices, –40 °C to 100 °C)	124.355	133	141.645	MHz
t_{DT}	Output Clock Duty Cycle	43	50	57	%
t_{OPJIT}[1]	Output Clock Period Jitter	0.01	0.012	0.02	UIPP
$t_{STABLEOSC}$	STDBY Low to Oscillator Stable	0.01	0.05	0.1	µs

1. Output Clock Period Jitter specified at 133 MHz. The values for lower frequencies will be smaller UIPP. The typical value for 133 MHz is 95 ps and for 2.08 MHz the typical value is 1.54 ns.

MachXO2 Standby Mode Timing – HC/HE Devices

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	USERSTDBY High to Stop	All	—	—	9	ns
t_{PWRUP}	USERSTDBY Low to Power Up	LCMXO2-256		—		µs
		LCMXO2-640		—		µs
		LCMXO2-640U		—		µs
		LCMXO2-1200	20	—	50	µs
		LCMXO2-1200U		—		µs
		LCMXO2-2000		—		µs
		LCMXO2-2000U		—		µs
		LCMXO2-4000		—		µs
		LCMXO2-7000		—		µs
t_{WSTDBY}	USERSTDBY Pulse Width	All	18	—	—	ns



MachXO2 Standby Mode Timing – ZE Devices

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	USERSTDBY High to Stop	All	—	—	13	ns
t_{PWRUP}	USERSTDBY Low to Power Up	LCMXO2-256		—		µs
		LCMXO2-640		—		µs
		LCMXO2-1200	20	—	50	µs
		LCMXO2-2000		—		µs
		LCMXO2-4000		—		µs
		LCMXO2-7000		—		µs
t_{WSTDBY}	USERSTDBY Pulse Width	All	19	—	—	ns
$t_{BNDGAPSTBL}$	USERSTDBY High to Bandgap Stable	All	—	—	15	ns

Flash Download Time[1, 2]

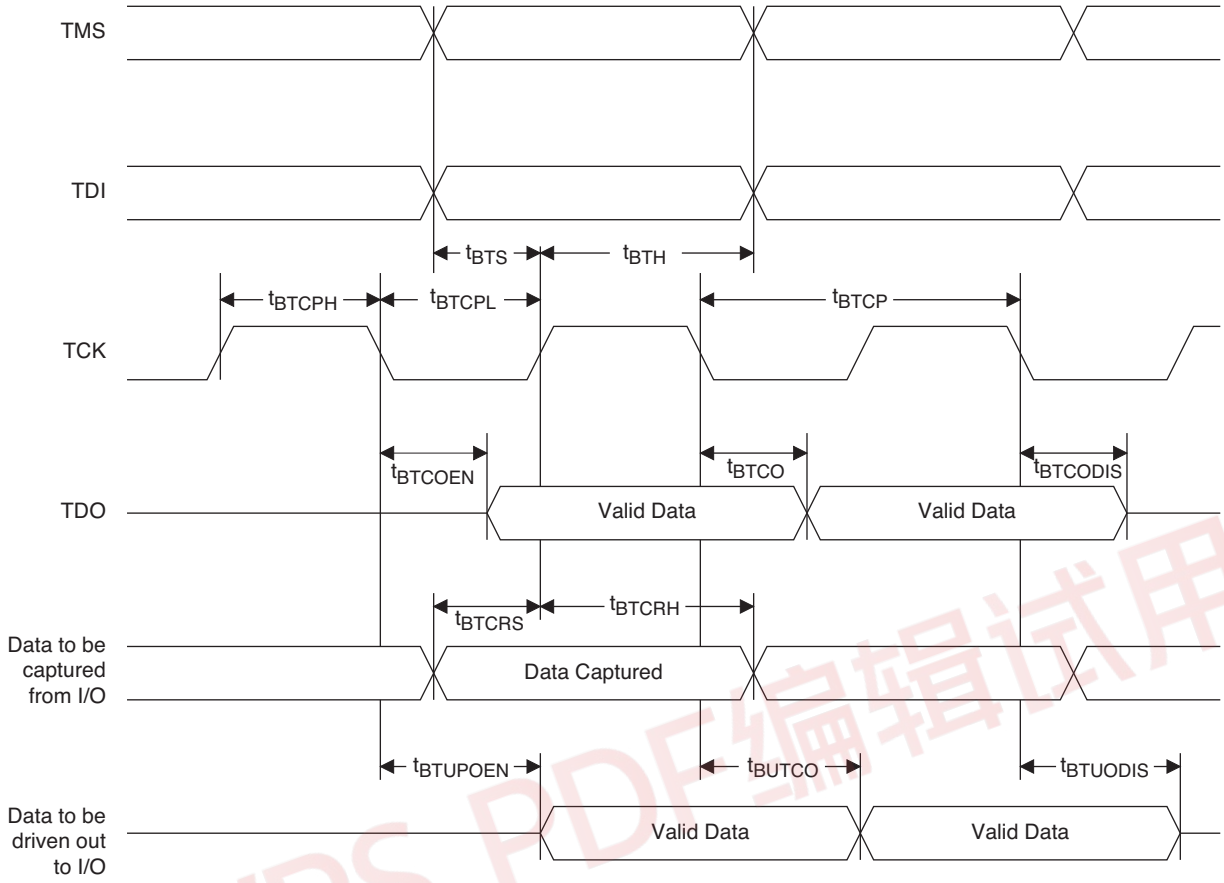
Symbol	Parameter	Device	Typ.	Units
$t_{REFRESH}$	POR to Device I/O Active	LCMXO2-256	0.6	ms
		LCMXO2-640	1.0	ms
		LCMXO2-640U	1.9	ms
		LCMXO2-1200	1.9	ms
		LCMXO2-1200U	1.4	ms
		LCMXO2-2000	1.4	ms
		LCMXO2-2000U	2.4	ms
		LCMXO2-4000	2.4	ms
		LCMXO2-7000	3.8	ms

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.
2. The Flash download time is measured starting from the maximum voltage of POR trip point.

JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	20	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-12. JTAG Port Timing Waveforms



sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Modes					
t_{PRGM}	PROGRAMN low pulse accept		55	—	ns
t_{PRGMJ}	PROGRAMN low pulse rejection		—	25	ns
t_{INITL}	INITN low time	LCMXO2-256	—	30	µs
		LCMXO2-640	—	35	µs
		LCMXO2-640U/ LCMXO2-1200	—	55	µs
		LCMXO2-1200U/ LCMXO2-2000	—	70	µs
		LCMXO2-2000U/ LCMXO2-4000	—	105	µs
		LCMXO2-7000	—	130	µs
$t_{DPPINIT}$	PROGRAMN low to INITN low		—	150	ns
$t_{DPPDONE}$	PROGRAMN low to DONE low		—	150	ns
t_{IODISS}	PROGRAMN low to I/O disable		—	120	ns
Slave SPI					
f_{MAX}	CCLK clock frequency		—	66	MHz
t_{CCLKH}	CCLK clock pulse width high		7.5	—	ns
t_{CCLKL}	CCLK clock pulse width low		7.5	—	ns
t_{STSU}	CCLK setup time		2	—	ns
t_{STH}	CCLK hold time		0	—	ns
t_{STCO}	CCLK falling edge to valid output		—	10	ns
t_{STOZ}	CCLK falling edge to valid disable		—	10	ns
t_{STOV}	CCLK falling edge to valid enable		—	10	ns
t_{SCS}	Chip select high time		25	—	ns
t_{SCSS}	Chip select setup time		3	—	ns
t_{SCSH}	Chip select hold time		3	—	ns
Master SPI					
f_{MAX}	MCLK clock frequency		—	133	MHz
t_{MCLKH}	MCLK clock pulse width high		3.75	—	ns
t_{MCLKL}	MCLK clock pulse width low		3.75	—	ns
t_{STSU}	MCLK setup time		5	—	ns
t_{STH}	MCLK hold time		1	—	ns
t_{CSSPI}	INITN high to chip select low		100	200	ns
t_{MCLK}	INITN high to first MCLK edge		0.75	1	µs

I²C Port Timing Specifications[1, 2]

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCL clock frequency	—	400	kHz

1. MachXO2 supports the following modes:
   • Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
   • Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
2. Refer to the I²C specification for timing requirements.

SPI Port Timing Specifications[1]

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCK clock frequency	—	45	MHz

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

Switching Test Conditions

Figure 3-13 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-5.

Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards

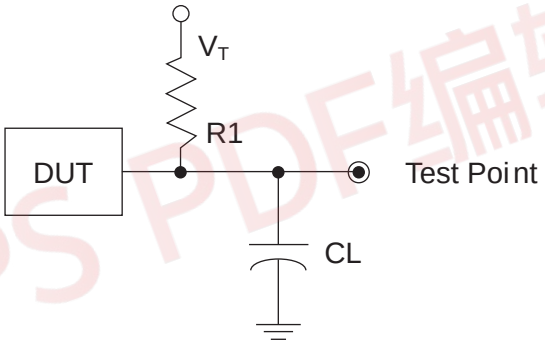


Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R1	CL	Timing Ref.	VT
LVTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5 V	V_{OL}
LVTTL and LVCMOS 3.3 (Z -> L)			1.5 V	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVTTL + LVCMOS (H -> Z)			V_{OH} – 0.15 V	V_{OL}
LVTTL + LVCMOS (L -> Z)			V_{OL} – 0.15 V	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the group to which the pad is connected. Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic. During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.
NC	—	No connect.
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together. For QFN 48 package, the exposed die pad is the device ground.
VCC	—	V_{CC} – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIOx	—	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.
PLL and Clock Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)		
[LOC]_GPLL[T, C]_IN	—	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.
Test and Programming (Dual function pins used for test access port and during sysCONFIG™)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
JTAGENB	I	Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then: If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O. If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.
Configuration (Dual function pins used during sysCONFIG)		
PROGRAMN	I	Initiates configuration sequence when asserted low. During configuration, or when reserved as PROGRAMN in user mode, this pin always has an active pull-up.

Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, or when reserved as INITn in user mode, this pin has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress. During configuration, or when reserved as DONE in user mode, this pin has an active pull-up.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.
SCL	I/O	Slave I^2C clock input and master I^2C clock output.
SDA	I/O	Slave I^2C data input and master I^2C data output.

Pinout Information Summary

	MachXO2-256					MachXO2-640			MachXO2-640U
	32 QFN[1]	48 QFN[3]	64 ucBGA	100 TQFP	132 csBGA	48 QFN[3]	100 TQFP	132 csBGA	144 TQFP
General Purpose I/O per Bank									
Bank 0	8	10	9	13	13	10	18	19	27
Bank 1	2	10	12	14	14	10	20	20	26
Bank 2	9	10	11	14	14	10	20	20	28
Bank 3	2	10	12	14	14	10	20	20	26
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Single Ended I/O	21	40	44	55	55	40	78	79	107
Differential I/O per Bank									
Bank 0	4	5	5	7	7	5	9	10	14
Bank 1	1	5	6	7	7	5	10	10	13
Bank 2	4	5	5	7	7	5	10	10	14
Bank 3	1	5	6	7	7	5	10	10	13
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Differential I/O	10	20	22	28	28	20	39	40	54
Dual Function I/O	22	25	27	29	29	25	29	29	33
High-speed Differential I/O									
Bank 0	0	0	0	0	0	0	0	0	7
Gearboxes									
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	0	0	0	0	0	0	0	0	7
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	0	0	0	0	0	0	0	0	7
DQS Groups									
Bank 1	0	0	0	0	0	0	0	0	2
VCCIO Pins									
Bank 0	2	2	2	2	2	2	2	2	3
Bank 1	1	1	2	2	2	1	2	2	3
Bank 2	2	2	2	2	2	2	2	2	3
Bank 3	1	1	2	2	2	1	2	2	3
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
VCC	2	2	2	2	2	2	2	2	4
GND[2]	2	1	8	8	8	1	8	10	12
NC	0	0	1	26	58	0	3	32	8
Reserved for Configuration	1	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	32	49	64	100	132	49	100	132	144

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.
2. For 48 QFN package, exposed die pad is the device ground.
3. 48-pin QFN information is 'Advanced'.

	MachXO2-1200					MachXO2-1200U
	100 TQFP	132 csBGA	144 TQFP	25 WLCSP	32 QFN[1]	256 ftBGA
General Purpose I/O per Bank						
Bank 0	18	25	27	11	9	50
Bank 1	21	26	26	0	2	52
Bank 2	20	28	28	7	9	52
Bank 3	20	25	26	0	2	16
Bank 4	0	0	0	0	0	16
Bank 5	0	0	0	0	0	20
Total General Purpose Single Ended I/O	79	104	107	18	22	206
Differential I/O per Bank						
Bank 0	9	13	14	5	4	25
Bank 1	10	13	13	0	1	26
Bank 2	10	14	14	2	4	26
Bank 3	10	12	13	0	1	8
Bank 4	0	0	0	0	0	8
Bank 5	0	0	0	0	0	10
Total General Purpose Differential I/O	39	52	54	7	10	103
Dual Function I/O	31	33	33	18	22	33
High-speed Differential I/O						
Bank 0	4	7	7	0	0	14
Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	4	7	7	0	0	14
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	5	7	7	0	2	14
DQS Groups						
Bank 1	1	2	2	0	0	2
VCCIO Pins						
Bank 0	2	3	3	1	2	4
Bank 1	2	3	3	0	1	4
Bank 2	2	3	3	1	2	4
Bank 3	3	3	3	0	1	1
Bank 4	0	0	0	0	0	2
Bank 5	0	0	0	0	0	1
VCC	2	4	4	2	2	8
GND	8	10	12	2	2	24
NC	1	1	8	0	0	1
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	100	132	144	25	32	256

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.

	MachXO2-2000						MachXO2-2000U
	49 WLCSP	100 TQFP	132 csBGA	144 TQFP	256 caBGA	256 ftBGA	484 ftBGA
General Purpose I/O per Bank							
Bank 0	19	18	25	27	50	50	70
Bank 1	0	21	26	28	52	52	68
Bank 2	13	20	28	28	52	52	72
Bank 3	0	6	7	8	16	16	24
Bank 4	0	6	8	10	16	16	16
Bank 5	6	8	10	10	20	20	28
Total General Purpose Single-Ended I/O	38	79	104	111	206	206	278
Differential I/O per Bank							
Bank 0	7	9	13	14	25	25	35
Bank 1	0	10	13	14	26	26	34
Bank 2	6	10	14	14	26	26	36
Bank 3	0	3	3	4	8	8	12
Bank 4	0	3	4	5	8	8	8
Bank 5	3	4	5	5	10	10	14
Total General Purpose Differential I/O	16	39	52	56	103	103	139
Dual Function I/O	24	31	33	33	33	33	37
High-speed Differential I/O							
Bank 0	5	4	8	9	14	14	18
Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	4	8	9	14	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	10	14	14	14	14	18
DQS Groups							
Bank 1	0	1	2	2	2	2	2
VCCIO Pins							
Bank 0	2	2	3	3	4	4	10
Bank 1	0	2	3	3	4	4	10
Bank 2	1	2	3	3	4	4	10
Bank 3	0	1	1	1	1	1	3
Bank 4	0	1	1	1	2	2	4
Bank 5	1	1	1	1	1	1	3
VCC	2	2	4	4	8	8	12
GND	4	8	10	12	24	24	48
NC	0	1	1	4	1	1	105
Reserved for Configuration	1	1	1	1	v	1	1
Total Count of Bonded Pins	39	100	132	144	256	256	484

	MachXO2-4000							
	84 QFN	132 csBGA	144 TQFP	184 csBGA	256 caBGA	256 ftBGA	332 caBGA	484 fpBGA
General Purpose I/O per Bank								
Bank 0	27	25	27	37	50	50	68	70
Bank 1	10	26	29	37	52	52	68	68
Bank 2	22	28	29	39	52	52	70	72
Bank 3	0	7	9	10	16	16	24	24
Bank 4	9	8	10	12	16	16	16	16
Bank 5	0	10	10	15	20	20	28	28
Total General Purpose Single Ended I/O	68	104	114	150	206	206	274	278
Differential I/O per Bank								
Bank 0	13	13	14	18	25	25	34	35
Bank 1	4	13	14	18	26	26	34	34
Bank 2	11	14	14	19	26	26	35	36
Bank 3	0	3	4	4	8	8	12	12
Bank 4	4	4	5	6	8	8	8	8
Bank 5	0	5	5	7	10	10	14	14
Total General Purpose Differential I/O	32	52	56	72	103	103	137	139
Dual Function I/O	28	37	37	37	37	37	37	37
High-speed Differential I/O								
Bank 0	8	8	9	8	18	18	18	18
Gearboxes								
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	8	8	9	9	18	18	18	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	11	14	14	12	18	18	18	18
DQS Groups								
Bank 1	1	2	2	2	2	2	2	2
VCCIO Pins								
Bank 0	3	3	3	3	4	4	4	10
Bank 1	1	3	3	3	4	4	4	10
Bank 2	2	3	3	3	4	4	4	10
Bank 3	1	1	1	1	1	1	2	3
Bank 4	1	1	1	1	2	2	1	4
Bank 5	1	1	1	1	1	1	2	3
VCC	4	4	4	4	8	8	8	12
GND	4	10	12	16	24	24	27	48
NC	1	1	1	1	1	1	5	105
Reserved for configuration	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	84	132	144	184	256	256	332	484

	MachXO2-7000					
	144 TQFP	**256 caBGA**	**256 ftBGA**	**332 caBGA**	**400 caBGA**	**484 fpBGA**
General Purpose I/O per Bank						
Bank 0	27	50	50	68	83	82
Bank 1	29	52	52	70	84	84
Bank 2	29	52	52	70	84	84
Bank 3	9	16	16	24	28	28
Bank 4	10	16	16	16	24	24
Bank 5	10	20	20	30	32	32
Total General Purpose Single Ended I/O	114	206	206	278	335	334
Differential I/O per Bank						
Bank 0	14	25	25	34	42	41
Bank 1	14	26	26	35	42	42
Bank 2	14	26	26	35	42	42
Bank 3	4	8	8	12	14	14
Bank 4	5	8	8	8	12	12
Bank 5	5	10	10	15	16	16
Total General Purpose Differential I/O	56	103	103	139	168	167
Dual Function I/O	37	37	37	37	37	37
High-speed Differential I/O						
Bank 0	9	20	20	21	21	21
Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	9	20	20	21	21	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	14	20	20	21	21	21
DQS Groups						
Bank 1	2	2	2	2	2	2
VCCIO Pins						
Bank 0	3	4	4	4	5	10
Bank 1	3	4	4	4	5	10
Bank 2	3	4	4	4	5	10
Bank 3	1	1	1	2	2	3
Bank 4	1	2	2	1	2	4
Bank 5	1	1	1	2	2	3
VCC	4	8	8	8	10	12
GND	12	24	24	27	33	48
NC	1	1	1	1	0	49
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	144	256	256	332	400	484

For Further Information

For further information regarding logic signal connections for various packages please refer to the MachXO2 Device Pinout Files.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Users must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1198, Power Estimation and Management for MachXO2 Devices
- The Power Calculator tool is included with the Lattice design tools, or as a standalone download from www.latticesemi.com/software

MachXO2 Family Data Sheet Ordering Information

March 2017 Data Sheet DS1035

MachXO2 Part Number Description

LCMXO2 – XXXX X X X – X XXXXXX X XX XX

Device Family
MachXO2 PLD

Logic Capacity
256 = 256 LUTs
640 = 640 LUTs
1200 = 1280 LUTs
2000 = 2112 LUTs
4000 = 4320 LUTs
7000 = 6864 LUTs

I/O Count
Blank = Standard Device
U = Ultra High I/O Device

Power/Performance
Z = Low Power
H = High Performance

Supply Voltage
C = 2.5 V / 3.3 V
E = 1.2 V

Speed
1 = Slowest
2
3 = Fastest
} Low Power

4 = Slowest
5
6 = Fastest
} High Performance

Device Status
Blank = Production Device
ES = Engineering Sample
R1 = Production Release 1 Device
1K = WLCSP Package, 1,000 parts per reel

Shipping Method
Blank = Trays
TR = Tape and Reel

Grade
C = Commercial
I = Industrial

Package
UWG25 = 25-Ball Halogen-Free WLCSP (0.4 mm Pitch)
SG32 = 32-Pin Halogen-Free QFN (0.5 mm Pitch)
SG48 = 48-Pin Halogen-Free QFN (0.5 mm Pitch)
UWG49 = 49-ball Halogen-Free WLCSP (0.4 mm Pitch)
UMG64 = 64-Ball Halogen-Free ucBGA (0.4 mm Pitch)
QN84 = 84-Pin Halogen-Free QFN (0.5 mm Pitch)
TG100 = 100-Pin Halogen-Free TQFP
TG144 = 144-Pin Halogen-Free TQFP
MG132 = 132-Ball Halogen-Free csBGA (0.5 mm Pitch)
MG184 = 184-Ball Halogen-Free csBGA (0.5 mm Pitch)
BG256 = 256-Ball Halogen-Free caBGA (0.8 mm Pitch)
FTG256 = 256-Ball Halogen-Free ftBGA (1.0 mm Pitch)
BG332 = 332-Ball Halogen-Free caBGA (0.8 mm Pitch)
FG484 = 484-Ball Halogen-Free fpBGA (1.0 mm Pitch)

* 48-pin QFN information is 'Advanced'.

Ordering Information

MachXO2 devices have top-side markings, for commercial and industrial grades, as shown below:

Notes:

1. Markings are abbreviated for small packages.

2. See PCN 05A-12 for information regarding a change to the top-side mark logo.

Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32C	256	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-256ZE-2SG32C	256	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-256ZE-3SG32C	256	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-256ZE-1UMG64C	256	1.2 V	–1	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-2UMG64C	256	1.2 V	–2	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-3UMG64C	256	1.2 V	–3	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-1TG100C	256	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-2TG100C	256	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-3TG100C	256	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-1MG132C	256	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-2MG132C	256	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-3MG132C	256	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100C	640	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-2TG100C	640	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-3TG100C	640	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-1MG132C	640	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-2MG132C	640	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-3MG132C	640	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1SG32C	1280	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-2SG32C	1280	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-3SG32C	1280	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-1TG100C	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100C	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100C	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132C	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132C	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132C	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144C	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144C	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144C	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1TG100C	2112	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-2TG100C	2112	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-3TG100C	2112	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-1MG132C	2112	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-2MG132C	2112	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-3MG132C	2112	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-1TG144C	2112	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-2TG144C	2112	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-3TG144C	2112	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-1BG256C	2112	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-2BG256C	2112	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-3BG256C	2112	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-1FTG256C	2112	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-2000ZE-2FTG256C	2112	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-2000ZE-3FTG256C	2112	1.2 V	–3	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000ZE-1QN84C	4320	1.2 V	–1	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-2QN84C	4320	1.2 V	–2	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-3QN84C	4320	1.2 V	–3	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-1MG132C	4320	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-2MG132C	4320	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-3MG132C	4320	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-1TG144C	4320	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-2TG144C	4320	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-3TG144C	4320	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-1BG256C	4320	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-2BG256C	4320	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-3BG256C	4320	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-1FTG256C	4320	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-2FTG256C	4320	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-3FTG256C	4320	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-1BG332C	4320	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-2BG332C	4320	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-3BG332C	4320	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-1FG484C	4320	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-4000ZE-2FG484C	4320	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-4000ZE-3FG484C	4320	1.2 V	–3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144C	6864	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-2TG144C	6864	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-3TG144C	6864	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-1BG256C	6864	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-2BG256C	6864	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-3BG256C	6864	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-1FTG256C	6864	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-2FTG256C	6864	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-3FTG256C	6864	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-1BG332C	6864	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-2BG332C	6864	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-3BG332C	6864	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-1FG484C	6864	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-2FG484C	6864	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-3FG484C	6864	1.2 V	–3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100CR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100CR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100CR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132CR1[1]	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132CR1[1]	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132CR1[1]	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144CR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144CR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144CR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200ZE-speed package CR1” are the same as the “LCMXO2-1200ZE-speed package C” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32C	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	COM
LCMXO2-256HC-5SG32C	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	COM
LCMXO2-256HC-6SG32C	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	COM
LCMXO2-256HC-4SG48C	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	COM
LCMXO2-256HC-5SG48C	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	COM
LCMXO2-256HC-6SG48C	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	COM
LCMXO2-256HC-4UMG64C	256	2.5 V / 3.3 V	–4	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-5UMG64C	256	2.5 V / 3.3 V	–5	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-6UMG64C	256	2.5 V / 3.3 V	–6	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-4TG100C	256	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-256HC-5TG100C	256	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-256HC-6TG100C	256	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-256HC-4MG132C	256	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-256HC-5MG132C	256	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-256HC-6MG132C	256	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48C	640	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	COM
LCMXO2-640HC-5SG48C	640	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	COM
LCMXO2-640HC-6SG48C	640	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	COM
LCMXO2-640HC-4TG100C	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-640HC-5TG100C	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-640HC-6TG100C	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-640HC-4MG132C	640	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-640HC-5MG132C	640	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-640HC-6MG132C	640	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144C	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-5TG144C	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-6TG144C	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32C	1280	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	COM
LCMXO2-1200HC-5SG32C	1280	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	COM
LCMXO2-1200HC-6SG32C	1280	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	COM
LCMXO2-1200HC-4TG100C	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100C	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100C	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132C	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132C	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132C	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144C	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144C	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144C	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256C	1280	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-1200UHC-5FTG256C	1280	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-1200UHC-6FTG256C	1280	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100C	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-5TG100C	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-6TG100C	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-4MG132C	2112	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-5MG132C	2112	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-6MG132C	2112	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-4TG144C	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-5TG144C	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-6TG144C	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-4BG256C	2112	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-5BG256C	2112	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-6BG256C	2112	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-4FTG256C	2112	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HC-5FTG256C	2112	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HC-6FTG256C	2112	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484C	2112	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-5FG484C	2112	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-6FG484C	2112	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84C	4320	2.5 V / 3.3 V	–4	Halogen-Free QFN	84	COM
LCMXO2-4000HC-5QN84C	4320	2.5 V / 3.3 V	–5	Halogen-Free QFN	84	COM
LCMXO2-4000HC-6QN84C	4320	2.5 V / 3.3 V	–6	Halogen-Free QFN	84	COM
LCMXO2-4000HC-4MG132C	4320	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-5MG132C	4320	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-6MG132C	4320	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-4TG144C	4320	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-5TG144C	4320	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-6TG144C	4320	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-4BG256C	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-5BG256C	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-6BG256C	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-4FTG256C	4320	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-5FTG256C	4320	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-6FTG256C	4320	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-4BG332C	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-5BG332C	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-6BG332C	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-4FG484C	4320	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-5FG484C	4320	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-6FG484C	4320	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144C	6864	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-5TG144C	6864	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-6TG144C	6864	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-4BG256C	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-5BG256C	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-6BG256C	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-4FTG256C	6864	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-5FTG256C	6864	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-6FTG256C	6864	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-4BG332C	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-5BG332C	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-6BG332C	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-4FG400C	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-5FG400C	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-6FG400C	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-4FG484C	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-5FG484C	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-6FG484C	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100CR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100CR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100CR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132CR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132CR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132CR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144CR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144CR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144CR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200HC-speed package CR1” are the same as the “LCMXO2-1200HC-speed package C” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100C	2112	1.2 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-5TG100C	2112	1.2 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-6TG100C	2112	1.2 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-4TG144C	2112	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-5TG144C	2112	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-6TG144C	2112	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-4MG132C	2112	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-5MG132C	2112	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-6MG132C	2112	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-4BG256C	2112	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-5BG256C	2112	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-6BG256C	2112	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-4FTG256C	2112	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-5FTG256C	2112	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-6FTG256C	2112	1.2 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484C	2112	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-5FG484C	2112	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-6FG484C	2112	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4TG144C	4320	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-5TG144C	4320	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-6TG144C	4320	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-4MG132C	4320	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-5MG132C	4320	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-6MG132C	4320	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-4BG256C	4320	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4MG184C	4320	1.2 V	–4	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5MG184C	4320	1.2 V	–5	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-6MG184C	4320	1.2 V	–6	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5BG256C	4320	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-6BG256C	4320	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4FTG256C	4320	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-5FTG256C	4320	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-6FTG256C	4320	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-4BG332C	4320	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-5BG332C	4320	1.2 V	–5	Halogen-Free caBGA	332	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-6BG332C	4320	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-4FG484C	4320	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-5FG484C	4320	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-6FG484C	4320	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144C	6864	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-5TG144C	6864	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-6TG144C	6864	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-4BG256C	6864	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-5BG256C	6864	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-6BG256C	6864	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-4FTG256C	6864	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-5FTG256C	6864	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-6FTG256C	6864	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-4BG332C	6864	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-5BG332C	6864	1.2 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-6BG332C	6864	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-4FG484C	6864	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-5FG484C	6864	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-6FG484C	6864	1.2 V	–6	Halogen-Free fpBGA	484	COM

Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32I	256	1.2 V	–1	Halogen-Free QFN	32	IND
LCMXO2-256ZE-2SG32I	256	1.2 V	–2	Halogen-Free QFN	32	IND
LCMXO2-256ZE-3SG32I	256	1.2 V	–3	Halogen-Free QFN	32	IND
LCMXO2-256ZE-1UMG64I	256	1.2 V	–1	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-2UMG64I	256	1.2 V	–2	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-3UMG64I	256	1.2 V	–3	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-1TG100I	256	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-2TG100I	256	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-3TG100I	256	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-1MG132I	256	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-2MG132I	256	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-3MG132I	256	1.2 V	–3	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100I	640	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-2TG100I	640	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-3TG100I	640	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-1MG132I	640	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-2MG132I	640	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-3MG132I	640	1.2 V	–3	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1UWG25ITR[1]	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR50[3]	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR1K[2]	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1SG32I	1280	1.2 V	–1	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-2SG32I	1280	1.2 V	–2	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-3SG32I	1280	1.2 V	–3	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-1TG100I	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100I	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100I	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132I	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132I	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132I	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144I	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144I	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144I	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1UWG49ITR[1]	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR50[3]	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR1K[2]	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1TG100I	2112	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-2TG100I	2112	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-3TG100I	2112	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-1MG132I	2112	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-2MG132I	2112	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-3MG132I	2112	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-1TG144I	2112	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-2TG144I	2112	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-3TG144I	2112	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-1BG256I	2112	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-2BG256I	2112	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-3BG256I	2112	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-1FTG256I	2112	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-2FTG256I	2112	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-3FTG256I	2112	1.2 V	–3	Halogen-Free ftBGA	256	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000ZE-1QN84I	4320	1.2 V	–1	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-2QN84I	4320	1.2 V	–2	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-3QN84I	4320	1.2 V	–3	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-1MG132I	4320	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-2MG132I	4320	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-3MG132I	4320	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-1TG144I	4320	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-2TG144I	4320	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-3TG144I	4320	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-1BG256I	4320	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-2BG256I	4320	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-3BG256I	4320	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-1FTG256I	4320	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-2FTG256I	4320	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-3FTG256I	4320	1.2 V	–3	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-1BG332I	4320	1.2 V	–1	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-2BG332I	4320	1.2 V	–2	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-3BG332I	4320	1.2 V	–3	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-1FG484I	4320	1.2 V	–1	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-2FG484I	4320	1.2 V	–2	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-3FG484I	4320	1.2 V	–3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144I	6864	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-2TG144I	6864	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-3TG144I	6864	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-1BG256I	6864	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-2BG256I	6864	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-3BG256I	6864	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-1FTG256I	6864	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-2FTG256I	6864	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-3FTG256I	6864	1.2 V	–3	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-1BG332I	6864	1.2 V	–1	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-2BG332I	6864	1.2 V	–2	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-3BG332I	6864	1.2 V	–3	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-1FG484I	6864	1.2 V	–1	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-2FG484I	6864	1.2 V	–2	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-3FG484I	6864	1.2 V	–3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100IR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100IR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100IR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132IR1[1]	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132IR1[1]	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132IR1[1]	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144IR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144IR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144IR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200ZE-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32I	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	IND
LCMXO2-256HC-5SG32I	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	IND
LCMXO2-256HC-6SG32I	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	IND
LCMXO2-256HC-4SG48I	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	IND
LCMXO2-256HC-5SG48I	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	IND
LCMXO2-256HC-6SG48I	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	IND
LCMXO2-256HC-4UMG64I	256	2.5 V / 3.3 V	–4	Halogen-Free ucBGA	64	IND
LCMXO2-256HC-5UMG64I	256	2.5 V / 3.3 V	–5	Halogen-Free ucBGA	64	IND
LCMXO2-256HC-6UMG64I	256	2.5 V / 3.3 V	–6	Halogen-Free ucBGA	64	IND
LCMXO2-256HC-4TG100I	256	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-256HC-5TG100I	256	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-256HC-6TG100I	256	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-256HC-4MG132I	256	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-256HC-5MG132I	256	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-256HC-6MG132I	256	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48I	640	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	IND
LCMXO2-640HC-5SG48I	640	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	IND
LCMXO2-640HC-6SG48I	640	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	IND
LCMXO2-640HC-4TG100I	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-640HC-5TG100I	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-640HC-6TG100I	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-640HC-4MG132I	640	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-640HC-5MG132I	640	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-640HC-6MG132I	640	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144I	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-640UHC-5TG144I	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-640UHC-6TG144I	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32I	1280	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	IND
LCMXO2-1200HC-5SG32I	1280	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	IND
LCMXO2-1200HC-6SG32I	1280	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	IND
LCMXO2-1200HC-4TG100I	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100I	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100I	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132I	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132I	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132I	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144I	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144I	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144I	1280	2.5 V/ 3.3 V	–6	Halogen-Free TQFP	144	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256I	1280	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-5FTG256I	1280	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-6FTG256I	1280	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100I	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-5TG100I	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-6TG100I	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-4MG132I	2112	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-5MG132I	2112	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-6MG132I	2112	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-4TG144I	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-5TG144I	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-6TG144I	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-4BG256I	2112	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-5BG256I	2112	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-6BG256I	2112	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-4FTG256I	2112	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-5FTG256I	2112	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-6FTG256I	2112	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484I	2112	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-5FG484I	2112	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-6FG484I	2112	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84I	4320	2.5 V / 3.3 V	–4	Halogen-Free QFN	84	IND
LCMXO2-4000HC-5QN84I	4320	2.5 V / 3.3 V	–5	Halogen-Free QFN	84	IND
LCMXO2-4000HC-6QN84I	4320	2.5 V / 3.3 V	–6	Halogen-Free QFN	84	IND
LCMXO2-4000HC-4TG144I	4320	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-5TG144I	4320	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-6TG144I	4320	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-4MG132I	4320	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-5MG132I	4320	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-6MG132I	4320	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-4BG256I	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-5BG256I	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-6BG256I	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-4FTG256I	4320	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-5FTG256I	4320	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-6FTG256I	4320	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-4BG332I	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-5BG332I	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-6BG332I	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-4FG484I	4320	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-5FG484I	4320	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-6FG484I	4320	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144I	6864	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-5TG144I	6864	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-6TG144I	6864	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-4BG256I	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-5BG256I	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-6BG256I	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-4FTG256I	6864	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-5FTG256I	6864	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-6FTG256I	6864	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-4BG332I	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-5BG332I	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-6BG332I	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-4FG400I	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-5FG400I	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-6FG400I	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-4FG484I	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-5FG484I	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-6FG484I	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100IR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100IR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100IR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132IR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132IR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132IR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144IR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144IR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144IR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200HC-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High Performance Industrial Grade Devices Without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100I	2112	1.2 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-5TG100I	2112	1.2 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-6TG100I	2112	1.2 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-4MG132I	2112	1.2 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-5MG132I	2112	1.2 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-6MG132I	2112	1.2 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-4TG144I	2112	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-5TG144I	2112	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-6TG144I	2112	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-4BG256I	2112	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-5BG256I	2112	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-6BG256I	2112	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-4FTG256I	2112	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-5FTG256I	2112	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-6FTG256I	2112	1.2 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484I	2112	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-5FG484I	2112	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-6FG484I	2112	1.2 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4MG132I	4320	1.2 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-5MG132I	4320	1.2 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-6MG132I	4320	1.2 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-4TG144I	4320	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-5TG144I	4320	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-6TG144I	4320	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-4MG184I	4320	1.2 V	–4	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-5MG184I	4320	1.2 V	–5	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-6MG184I	4320	1.2 V	–6	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-4BG256I	4320	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-5BG256I	4320	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-6BG256I	4320	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-4FTG256I	4320	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-5FTG256I	4320	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-6FTG256I	4320	1.2 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-4BG332I	4320	1.2 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-5BG332I	4320	1.2 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-6BG332I	4320	1.2 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-4FG484I	4320	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-5FG484I	4320	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-6FG484I	4320	1.2 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144I	6864	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-5TG144I	6864	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-6TG144I	6864	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-4BG256I	6864	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-5BG256I	6864	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-6BG256I	6864	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-4FTG256I	6864	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-5FTG256I	6864	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-6FTG256I	6864	1.2 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-4BG332I	6864	1.2 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-5BG332I	6864	1.2 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-6BG332I	6864	1.2 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-4FG484I	6864	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-5FG484I	6864	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-6FG484I	6864	1.2 V	–6	Halogen-Free fpBGA	484	IND

R1 Device Specifications

The LCMXO2-1200ZE/HC "R1" devices have the same specifications as their Standard (non-R1) counterparts except as listed below. For more details on the R1 to Standard migration refer to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard Non-R1) Devices.

- The User Flash Memory (UFM) cannot be programmed through the internal WISHBONE interface. It can still be programmed through the JTAG/SPI/I^{2}C ports.
- The on-chip differential input termination resistor value is higher than intended. It is approximately 200Ω as opposed to the intended 100Ω. It is recommended to use external termination resistors for differential inputs. The on-chip termination resistors can be disabled through Lattice design software.
- Soft Error Detection logic may not produce the correct result when it is run for the first time after configuration. To use this feature, discard the result from the first operation. Subsequent operations will produce the correct result.
- Under certain conditions, IIH exceeds data sheet specifications. The following table provides more details:

Condition	Clamp	Pad Rising IIH Max.	Pad Falling IIH Min.	Steady State Pad High IIH	Steady State Pad Low IIL
VPAD > VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD = VCCIO	ON	10 µA	–10 µA	10 µA	10 µA
VPAD = VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD < VCCIO	OFF	10 µA	–10 µA	10 µA	10 µA

- The user SPI interface does not operate correctly in some situations. During master read access and slave write access, the last byte received does not generate the RRDY interrupt.
- In GDDRX2, GDDRX4 and GDDR71 modes, ECLKSYNC may have a glitch in the output under certain conditions, leading to possible loss of synchronization.
- When using the hard I^{2}C IP core, the I^{2}C status registers I2C_1_SR and I2C_2_SR may not update correctly.
- PLL Lock signal will glitch high when coming out of standby. This glitch lasts for about 10 µsec before returning low.
- Dual boot only available on HC devices, requires tying VCC and VCCIO2 to the same 3.3 V or 2.5 V supply.

MachXO2 Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the MachXO2 family are available on the Lattice web site.

- TN1198, Power Estimation and Management for MachXO2 Devices
- TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide
- TN1201, Memory Usage Guide for MachXO2 Devices
- TN1202, MachXO2 sysIO Usage Guide
- TN1203, Implementing High-Speed Interfaces with MachXO2 Devices
- TN1204, MachXO2 Programming and Configuration Usage Guide
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices
- TN1206, MachXO2 SRAM CRC Error Detection Usage Guide
- TN1207, Using TraceID in MachXO2 Devices
- TN1074, PCB Layout Recommendations for BGA Packages
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices
- AN8066, Boundary Scan Testability with Lattice sysIO Capability
- MachXO2 Device Pinout Files
- Thermal Management document
- Lattice design tools

For further information on interface standards, refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, LVDS, DDR, DDR2, LPDDR): www.jedec.org
- PCI: www.pcisig.com

MachXO2 Family Data Sheet Revision History

March 2017 **Data Sheet DS1035**

Date	Version	Section	Change Summary
March 2017	3.3	DC and Switching Characteristics	Updated the Absolute Maximum Ratings section. Added standards.
			Updated the sysIO Recommended Operating Conditions section. Added standards.
			Updated the sysIO Single-Ended DC Electrical Characteristics section. Added standards.
			Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA}. The parameter descriptions were also modified.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA}. The parameter descriptions were also modified.
			Updated the sysCONFIG Port Timing Specifications section. Corrected the t_{INITL} units from ns to µs.
		Pinout Information	Updated the Signal Descriptions section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals.
			Updated the Pinout Information Summary section. Added footnote to MachXO2-1200 32 QFN.
		Ordering Information	Updated the MachXO2 Part Number Description section. Corrected the MG184, BG256, FTG256 package information. Added “(0.8 mm Pitch)” to BG332.
			Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. — Updated LCMXO2-1200ZE-1UWG25ITR50 footnote. — Corrected footnote numbering typo. — Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2-2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s.

Date	Version	Section	Change Summary
May 2016	3.2	All	Moved designation for 84 QFN package information from 'Advanced' to 'Final'.
		Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added ‘Advanced’ 48 QFN package. — Revised footnote 6. — Added footnote 9.
		DC and Switching Characteristics	Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Added footnote 12.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Added footnote 12.
		Pinout Information	Updated the Signal Descriptions section. Added information on GND signal.
			Updated the Pinout Information Summary section. — Added ‘Advanced’ MachXO2-256 48 QFN values. — Added ‘Advanced’ MachXO2-640 48 QFN values. — Added footnote to GND. — Added footnotes 2 and 3.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added ‘Advanced’ SG48 package and revised footnote.
			Updated the Ordering Information section. — Added part numbers for ‘Advanced’ QFN 48 package.
March 2016	3.1	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 32 QFN value for XO2-1200. — Added 84 QFN (7 mm x 7 mm, 0.5 mm) package. — Modified package name to 100-pin TQFP. — Modified package name to 144-pin TQFP. — Added footnote.
		Architecture	Updated the Typical I/O Behavior During Power-up section. Removed reference to TN1202.
		DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications section. Revised $t_{DPPDONE}$ and $t_{DPPINIT}$ Max. values per PCN 03A-16, released March 2016.
		Pinout Information	Updated the Pinout Information Summary section. — Added MachXO2-1200 32 QFN values. — Added ‘Advanced’ MachXO2-4000 84 QFN values.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added ‘Advanced’ QN84 package and footnote.
			Updated the Ordering Information section. — Added part numbers for 1280 LUTs QFN 32 package. — Added part numbers for 4320 LUTs QFN 84 package.
March 2015	3.0	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Changed 64-ball ucBGA dimension.
		Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.

Date	Version	Section	Change Summary
December 2014	2.9	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Removed XO2-4000U data. — Removed 400-ball ftBGA. — Removed 25-ball WLCSP value for XO2-2000U.
		DC and Switching Characteristics	Updated the Recommended Operating Conditions section. Adjusted Max. values for V_{CC} and V_{CCIO}.
			Updated the sysIO Recommended Operating Conditions section. Adjusted Max. values for LVCMOS 3.3, LVTTL, PCI, LVDS33 and LVPECL.
		Pinout Information	Updated the Pinout Information Summary section. Removed MachXO2-4000U.
		Ordering Information	Updated the MachXO2 Part Number Description section. Removed BG400 package.
			Updated the High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
			Updated the High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
November 2014	2.8	Introduction	Updated the Features section. — Revised I/Os under Flexible Logic Architecture. — Revised standby power under Ultra Low Power Devices. — Revise input frequency range under Flexible On-Chip Clocking.
			Updated Table 1-1, MachXO2 Family Selection Guide. — Added XO2-4000U data. — Removed HE and ZE device options for XO2-4000. — Added 400-ball ftBGA.
		Pinout Information	Updated the Pinout Information Summary section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added BG400 package.
			Updated the Ordering Information section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400 part numbers.
October 2014	2.7	Ordering Information	Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Fixed typo in LCMXO2-2000ZE-1UWG49ITR part number package.
		Architecture	Updated the Supported Standards section. Added MIPI information to Table 2-12. Supported Input Standards and Table 2-13. Supported Output Standards.
		DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition.
			Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition.
			Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.
July 2014	2.6	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics[1, 2] section. Updated footnote 4.
			Updated Register-to-Register Performance section. Updated footnote.
		Ordering Information	Updated UW49 package to UWG49 in MachXO2 Part Number Description.
			Updated LCMXO2-2000ZE-1UWG49CTR package in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging.

Date	Version	Section	Change Summary
May 2014	2.5	Architecture	Updated TransFR (Transparent Field Reconfiguration) section. Updated TransFR description for PLL use during background Flash programming.
February 2014	02.4	Introduction	Included the 49 WLCSP package in the MachXO2 Family Selection Guide table.
		Architecture	Added information to Standby Mode and Power Saving Options section.
		Pinout Information	Added the XO2-2000 49 WLCSP in the Pinout Information Summary table.
		Ordering Information	Added UW49 package in MachXO2 Part Number Description.
			Added and LCMXO2-2000ZE-1UWG49CTR in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging section.
			Added and LCMXO2-2000ZE-1UWG49ITR in Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section.
December 2013	02.3	Architecture	Updated information on CLKOS output divider in sysCLOCK Phase Locked Loops (PLLs) section.
		DC and Switching Characteristics	Updated Static Supply Current – ZE Devices table.
			Updated footnote 4 in sysIO Single-Ended DC Electrical Characteristics table; Updated V_{IL} Max. (V) data for LVCMOS 25 and LVCMOS 28.
			Updated V_{OS} test condition in sysIO Differential Electrical Characteristics - LVDS table.
September 2013	02.2	Architecture	Removed I^2C Clock-Stretching feature per PCN #10A-13.
			Removed information on PDPR memory in RAM Mode section.
			Updated Supported Input Standards table.
		DC and Switching Characteristics	Updated Power-On-Reset Voltage Levels table.
June 2013	02.1	Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.
			sysCLOCK Phase Locked Loops (PLLs) section – Added missing cross reference to sysCLOCK PLL Timing table.
		DC and Switching Characteristics	Added slew rate information to footnote 2 of the MachXO2 External Switching Characteristics – HC/HE Devices and the MachXO2 External Switching Characteristics – ZE Devices tables.
			Power-On-Reset Voltage Levels table – Added symbols.

Date	Version	Section	Change Summary
January 2013	02.0	Introduction	Updated the total number IOs to include JTAGENB.
		Architecture	Supported Output Standards table – Added 3.3 V_{CCIO} (Typ.) to LVDS row.
			Changed SRAM CRC Error Detection to Soft Error Detection.
		DC and Switching Characteristics	Power Supply Ramp Rates table – Updated Units column for t_{RAMP} symbol.
			Added new Maximum sysIO Buffer Performance table.
			sysCLOCK PLL Timing table – Updated Min. column values for f_{IN}, f_{OUT}, f_{OUT2} and f_{PFD} parameters. Added t_{SPO} parameter. Updated footnote 6.
			MachXO2 Oscillator Output Frequency table – Updated symbol name for $t_{STABLEOSC.}$
			DC Electrical Characteristics table – Updated conditions for $I_{IL,}$ I_{IH} symbols.
			Corrected parameters tDQVBS and tDQVAS
			Corrected MachXO2 ZE parameters tDVADQ and tDVEDQ
		Pinout Information	Included the MachXO2-4000HE 184 csBGA package.
		Ordering Information	Updated part number.
April 2012	01.9	Architecture	Removed references to TN1200.
		Ordering Information	Updated the Device Status portion of the MachXO2 Part Number Description to include the 50 parts per reel for the WLCSP package.
			Added new part number and footnote 2 for LCMXO2-1200ZE-1UWG25ITR50.
			Updated footnote 1 for LCMXO2-1200ZE-1UWG25ITR.
		Supplemental Information	Removed references to TN1200.
March 2012	01.8	Introduction	Added 32 QFN packaging information to Features bullets and MachXO2 Family Selection Guide table.
		DC and Switching Characteristics	Changed ‘STANDBY’ to ‘USERSTDBY’ in Standby Mode timing diagram.
		Pinout Information	Removed footnote from Pin Information Summary tables.
			Added 32 QFN package to Pin Information Summary table.
		Ordering Information	Updated Part Number Description and Ordering Information tables for 32 QFN package.
			Updated topside mark diagram in the Ordering Information section.

Date	Version	Section	Change Summary
February 2012	01.7	All	Updated document with new corporate logo.
	01.6	—	Data sheet status changed from preliminary to final.
		Introduction	MachXO2 Family Selection Guide table – Removed references to 49-ball WLCSP.
		DC and Switching Characteristics	Updated Flash Download Time table.
			Modified Storage Temperature in the Absolute Maximum Ratings section.
			Updated I_{DK} max in Hot Socket Specifications table.
			Modified Static Supply Current tables for ZE and HC/HE devices.
			Updated Power Supply Ramp Rates table.
			Updated Programming and Erase Supply Current tables.
			Updated data in the External Switching Characteristics table.
			Corrected Absolute Maximum Ratings for Dedicated Input Voltage Applied for LCMXO2 HC.
			DC Electrical Characteristics table – Minor corrections to conditions for I_{IL}, I_{IH}.
		Pinout Information	Removed references to 49-ball WLCSP.
			Signal Descriptions table – Updated description for GND, VCC, and VCCIOx.
			Updated Pin Information Summary table – Number of VCCIOs, GNDs, VCCs, and Total Count of Bonded Pins for MachXO2-256, 640, and 640U and Dual Function I/O for MachXO2-4000 332caBGA.
		Ordering Information	Removed references to 49-ball WLCSP
August 2011	01.5	DC and Switching Characteristics	Updated ESD information.
		Ordering Information	Updated footnote for ordering WLCSP devices.
	01.4	Architecture	Updated information in Clock/Control Distribution Network and sysCLOCK Phase Locked Loops (PLLs).
		DC and Switching Characteristics	Updated I_{IL} and I_{IH} conditions in the DC Electrical Characteristics table.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Updated Pin Information Summary table: Dual Function I/O, DQS Groups Bank 1, Total General Purpose Single-Ended I/O, Differential I/O Per Bank, Total Count of Bonded Pins, Gearboxes. Added column of data for MachXO2-2000 49 WLCSP.
		Ordering Information	Updated R1 Device Specifications text section with information on migration from MachXO2-1200-R1 to Standard (non-R1) devices.
			Corrected Supply Voltage typo for part numbers: LCMX02-2000UHE-4FG484I, LCMX02-2000UHE-5FG484I, LCMX02-2000UHE-6FG484I.
			Added footnote for WLCSP package parts.
		Supplemental Information	Removed reference to Stand-alone Power Calculator for MachXO2 Devices. Added reference to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices.

Date	Version	Section	Change Summary
May 2011	01.3	Multiple	Replaced “SED” with “SRAM CRC Error Detection” throughout the document.
		DC and Switching Characteristics	Added footnote 1 to Program Erase Specifications table.
		Pinout Information	Updated Pin Information Summary tables.
			Signal name SO/SISPISO changed to SO/SPISO in the Signal Descriptions table.
April 2011	01.2	—	Data sheet status changed from Advance to Preliminary.
		Introduction	Updated MachXO2 Family Selection Guide table.
		Architecture	Updated Supported Input Standards table.
			Updated sysMEM Memory Primitives diagram.
			Added differential SSTL and HSTL IO standards.
		DC and Switching Characteristics	Updates following parameters: POR voltage levels, DC electrical characteristics, static supply current for ZE/HE/HC devices, static power consumption contribution of different components – ZE devices, programming and erase Flash supply current.
			Added VREF specifications to sysIO recommended operating conditions.
			Updating timing information based on characterization.
			Added differential SSTL and HSTL IO standards.
		Ordering Information	Added Ordering Part Numbers for R1 devices, and devices in WLCSP packages.
			Added R1 device specifications.
January 2011	01.1	All	Included ultra-high I/O devices.
		DC and Switching Characteristics	Recommended Operating Conditions table – Added footnote 3.
			DC Electrical Characteristics table – Updated data for I_{IL}, I_{IH}. V_{HYST} typical values updated.
			Generic DDRX2 Outputs with Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB}.
			Generic DDRX4 Outputs with Clock and Data Aligned at Pin (GDDRX4_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB}.
			Power-On-Reset Voltage Levels table - clarified note 3.
			Clarified VCCIO related recommended operating conditions specifications.
			Added power supply ramp rate requirements.
			Added Power Supply Ramp Rates table.
			Updated Programming/Erase Specifications table.
			Removed references to V_{CCP}.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Removed references to V_{CCP}.
November 2010	01.0	—	Initial release.

MachXO2™ Family Data Sheet

DS1035 Version 3.3, March 2017

MachXO2 Family Data Sheet Introduction

May 2016 Data Sheet DS1035

Features

- **Flexible Logic Architecture**
  - Six devices with 256 to 6864 LUT4s and 18 to 334 I/Os
- **Ultra Low Power Devices**
  - Advanced 65 nm low power process
  - As low as 22 µW standby power
  - Programmable low swing differential I/Os
  - Stand-by mode and other power saving options
- **Embedded and Distributed Memory**
  - Up to 240 kbits sysMEM™ Embedded Block RAM
  - Up to 54 kbits Distributed RAM
  - Dedicated FIFO control logic
- **On-Chip User Flash Memory**
  - Up to 256 kbits of User Flash Memory
  - 100,000 write cycles
  - Accessible through WISHBONE, SPI, I^2C and JTAG interfaces
  - Can be used as soft processor PROM or as Flash memory
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated gearing logic
  - 7:1 Gearing for Display I/Os
  - Generic DDR, DDRX2, DDRX4
  - Dedicated DDR/DDR2/LPDDR memory with DQS support
- **High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - PCI
    - LVDS, Bus-LVDS, MLVDS, RSDS, LVPECL
    - SSTL 25/18
    - HSTL 18
    - Schmitt trigger inputs, up to 0.5 V hysteresis
  - I/Os support hot socketing
  - On-chip differential termination
  - Programmable pull-up or pull-down mode
- **Flexible On-Chip Clocking**
  - Eight primary clocks
  - Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
  - Up to two analog PLLs per device with fractional-n frequency synthesis
    - Wide input frequency range (7 MHz to 400 MHz)
- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - Single-chip, secure solution
  - Programmable through JTAG, SPI or I^2C
  - Supports background programming of non-volatile memory
  - Optional dual boot with external SPI memory
- **TransFR™ Reconfiguration**
  - In-field logic update while system operates
- **Enhanced System Level Support**
  - On-chip hardened functions: SPI, I^2C, timer/counter
  - On-chip oscillator with 5.5% accuracy
  - Unique TraceID for system tracking
  - One Time Programmable (OTP) mode
  - Single power supply with extended operating range
  - IEEE Standard 1149.1 boundary scan
  - IEEE 1532 compliant in-system programming
- **Broad Range of Package Options**
  - TQFP, WLCSP, ucBGA, csBGA, caBGA, ftBGA, fpBGA, QFN package options
  - Small footprint package options
    - As small as 2.5 mm x 2.5 mm
  - Density migration supported
  - Advanced halogen-free packaging

Table 1-1. MachXO2™ Family Selection Guide

		XO2-256	XO2-640	XO2-640U[1]	XO2-1200	XO2-1200U[1]	XO2-2000	XO2-2000U[1]	XO2-4000	XO2-7000
LUTs		256	640	640	1280	1280	2112	2112	4320	6864
Distributed RAM (kbits)		2	5	5	10	10	16	16	34	54
EBR SRAM (kbits)		0	18	64	64	74	74	92	92	240
Number of EBR SRAM Blocks (9 kbits/block)		0	2	7	7	8	8	10	10	26
UFM (kbits)		0	24	64	64	80	80	96	96	256
Device Options:	HC[2]	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	HE[3]						Yes	Yes	Yes	Yes
	ZE[4]	Yes	Yes		Yes		Yes		Yes	Yes
Number of PLLs		0	0	1	1	1	1	2	2	2
Hardened Functions:	I2C	2	2	2	2	2	2	2	2	2
	SPI	1	1	1	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1	1	1	1
Packages						**IO**				
25-ball WLCSP[5] (2.5 mm x 2.5 mm, 0.4 mm)					18					
32 QFN[6] (5 mm x 5 mm, 0.5 mm)		21			21					
48 QFN[8, 9] (7 mm x 7 mm, 0.5 mm)		40	40							
49-ball WLCSP[5] (3.2 mm x 3.2 mm, 0.4 mm)							38			
64-ball ucBGA (4 mm x 4 mm, 0.4 mm)		44								
84 QFN[7] (7 mm x 7 mm, 0.5 mm)									68	
100-pin TQFP (14 mm x 14 mm)		55	78		79		79			
132-ball csBGA (8 mm x 8 mm, 0.5 mm)		55	79		104		104		104	
144-pin TQFP (20 mm x 20 mm)				107	107		111		114	114
184-ball csBGA[7] (8 mm x 8 mm, 0.5 mm)									150	
256-ball caBGA (14 mm x 14 mm, 0.8 mm)							206		206	206
256-ball ftBGA (17 mm x 17 mm, 1.0 mm)						206	206		206	206
332-ball caBGA (17 mm x 17 mm, 0.8 mm)									274	278
484-ball ftBGA (23 mm x 23 mm, 1.0 mm)								278	278	334

1. Ultra high I/O device.
2. High performance with regulator – VCC = 2.5 V, 3.3 V
3. High performance without regulator – V_{CC} = 1.2 V
4. Low power without regulator – V_{CC} = 1.2 V
5. WLCSP package only available for ZE devices.
6. 32 QFN package only available for HC and ZE devices.
7. 184 csBGA package only available for HE devices.
8. 48-pin QFN information is ‘Advanced’.
9. 48 QFN package only available for HC devices.

Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I^2C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external V_{CC} supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V_{CC} supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I^2C port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

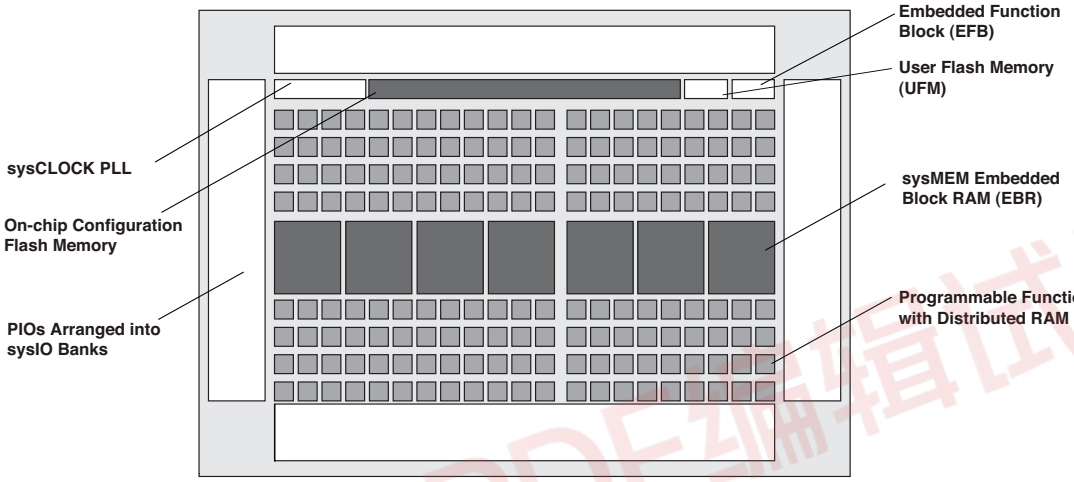
Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

Architecture Overview

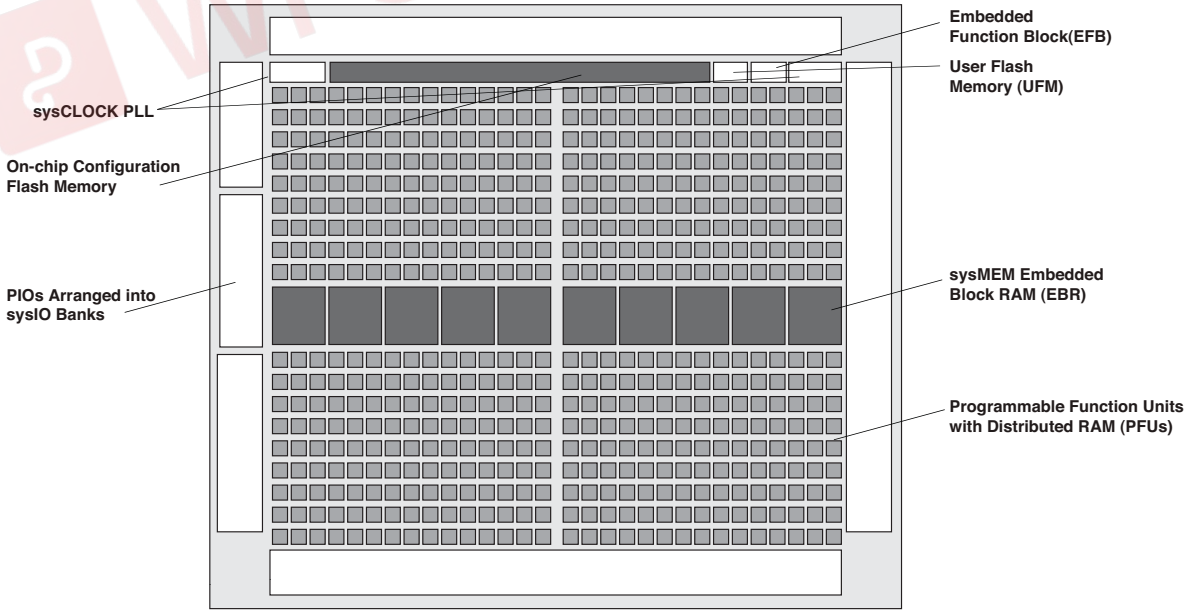
The MachXO2 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.

Figure 2-1. Top View of the MachXO2-1200 Device



Note: MachXO2-256, and MachXO2-640/U are similar to MachXO2-1200. MachXO2-256 has a lower LUT count and no PLL or EBR blocks. MachXO2-640 has no PLL, a lower LUT count and two EBR blocks. MachXO2-640U has a lower LUT count, one PLL and seven EBR blocks.

Figure 2-2. Top View of the MachXO2-4000 Device



Note: MachXO2-1200U, MachXO2-2000/U and MachXO2-7000 are similar to MachXO2-4000. MachXO2-1200U and MachXO2-2000 have a lower LUT count, one PLL, and eight EBR blocks. MachXO2-2000U has a lower LUT count, two PLLs, and 10 EBR blocks. MachXO2-7000 has a higher LUT count, two PLLs, and 26 EBR blocks.

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2-640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

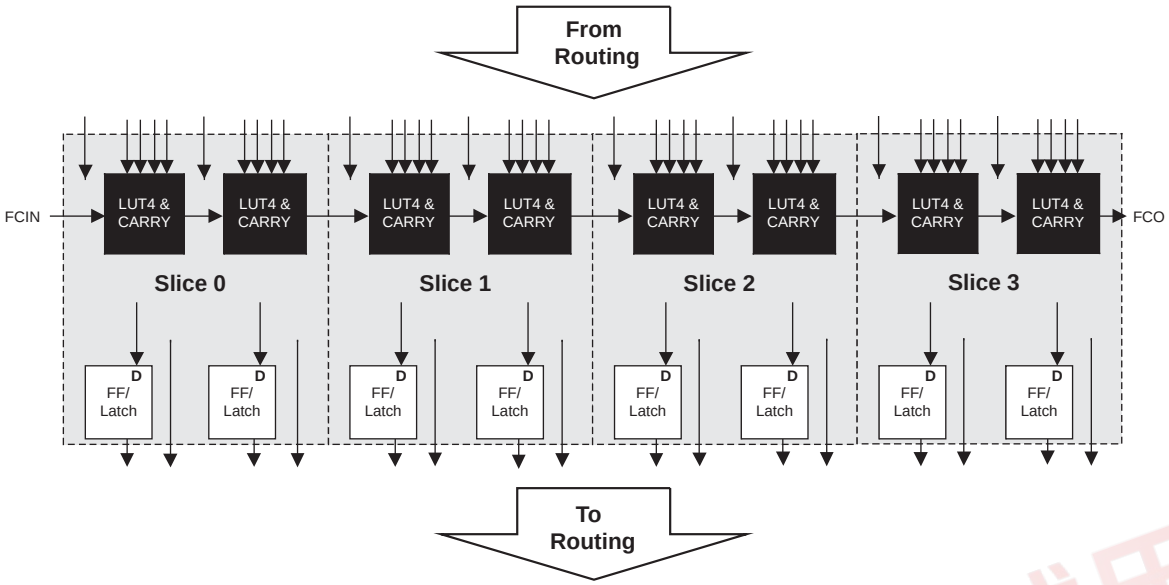
MachXO2 devices provide commonly used hardened functions such as SPI controller, I^2C controller and timer/counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I^2C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

PFU Blocks

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Block Diagram



Slices

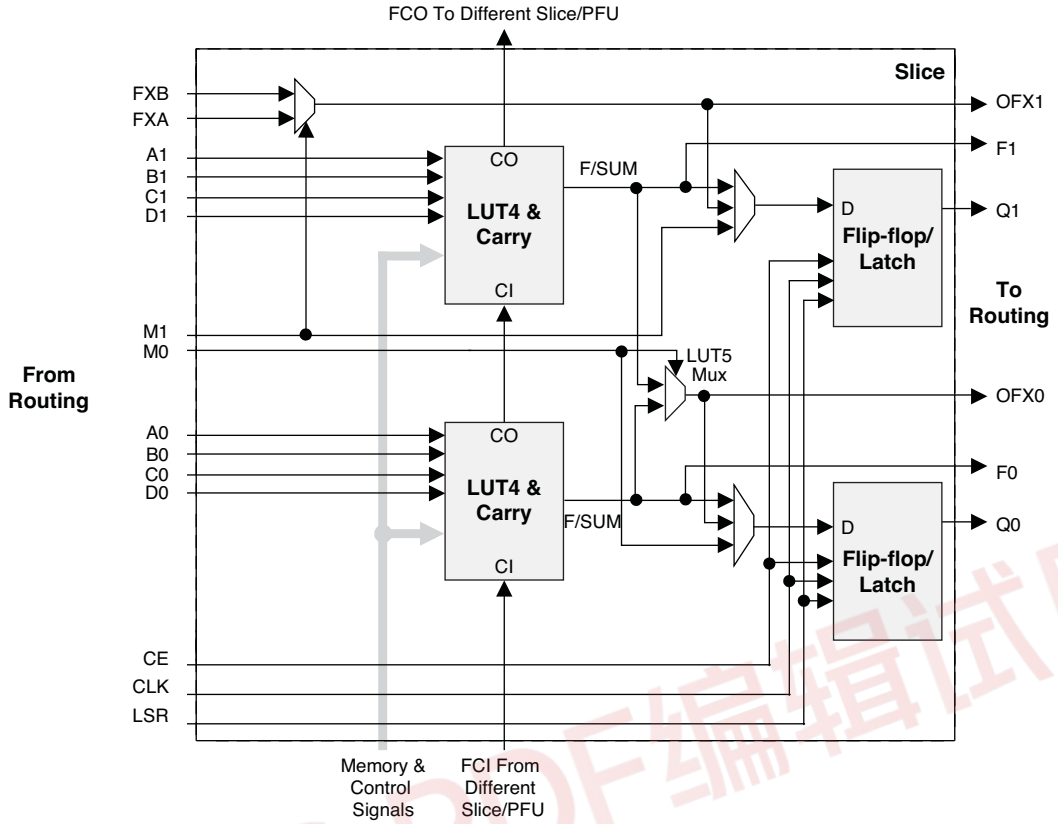
Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU Block	
	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.

Figure 2-4. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multi-purpose input
Input	Control signal	CE	Clock enable
Input	Control signal	LSR	Local set/reset
Input	Control signal	CLK	System clock
Input	Inter-PFU signal	FCIN	Fast carry in[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Fast carry out[1]

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO2 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO2 devices, please see TN1201, Memory Usage Guide for MachXO2 Devices.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

Routing

There are many resources provided in the MachXO2 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Each MachXO2 device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

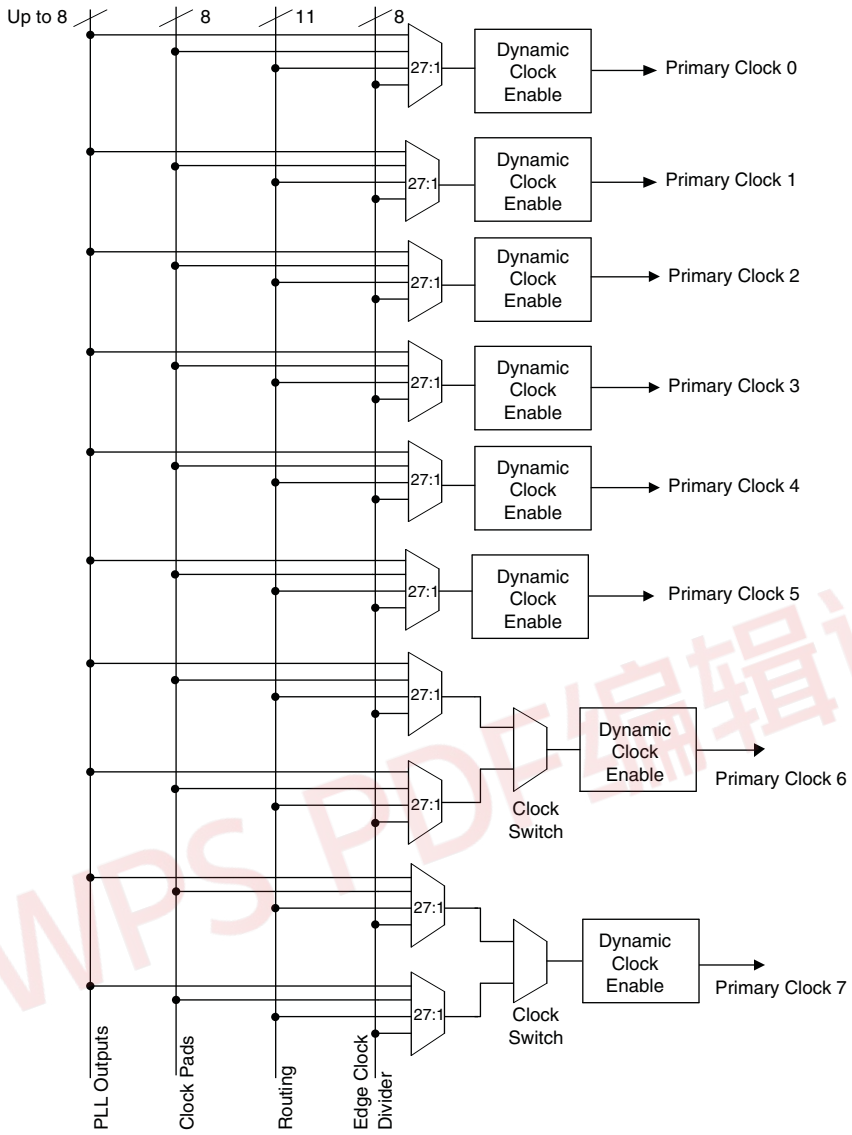
The MachXO2 architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO2-640U, MachXO2-1200/U and higher density devices have two edge clocks each on the top and bottom edges. Lower density devices have no edge clocks. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO2 devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO2 External Switching Characteristics table.

The primary clock signals for the MachXO2-256 and MachXO2-640 are generated from eight 17:1 muxes The available clock sources include eight I/O sources and 9 routing inputs. Primary clock signals for the MachXO2-640U, MachXO2-1200/U and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.

Figure 2-5. Primary Clocks for MachXO2 Devices

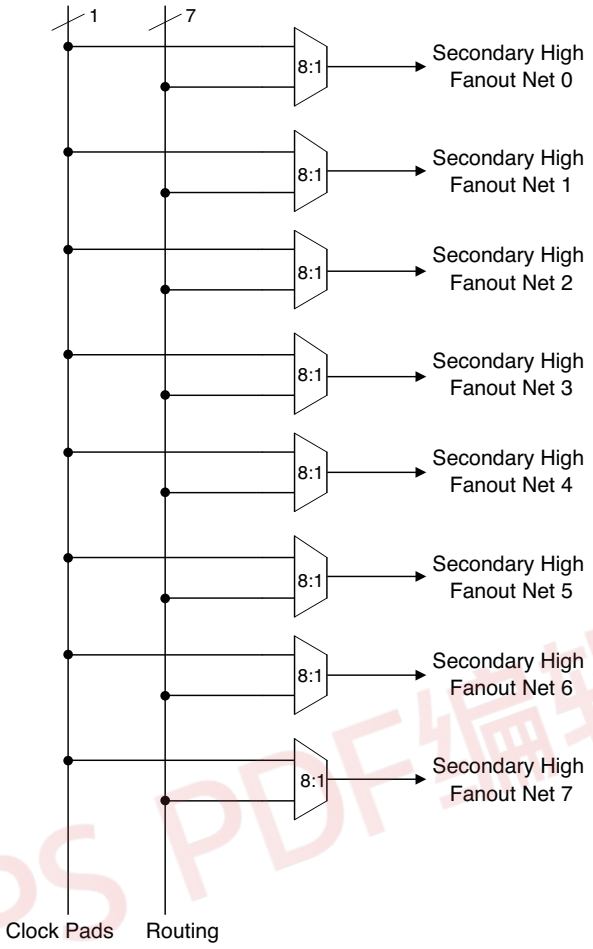


Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO2 External Switching Characteristics table.

Figure 2-6. Secondary High Fanout Nets for MachXO2 Devices



sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The MachXO2-640U, MachXO2-1200/U and larger devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO2 sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO2 clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.

This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the t_{LOCK} parameter has been satisfied.

The MachXO2 also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO2 PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the t_{LOCK} parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

For more details on the PLL and the WISHBONE interface, see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

Figure 2-7. PLL Diagram

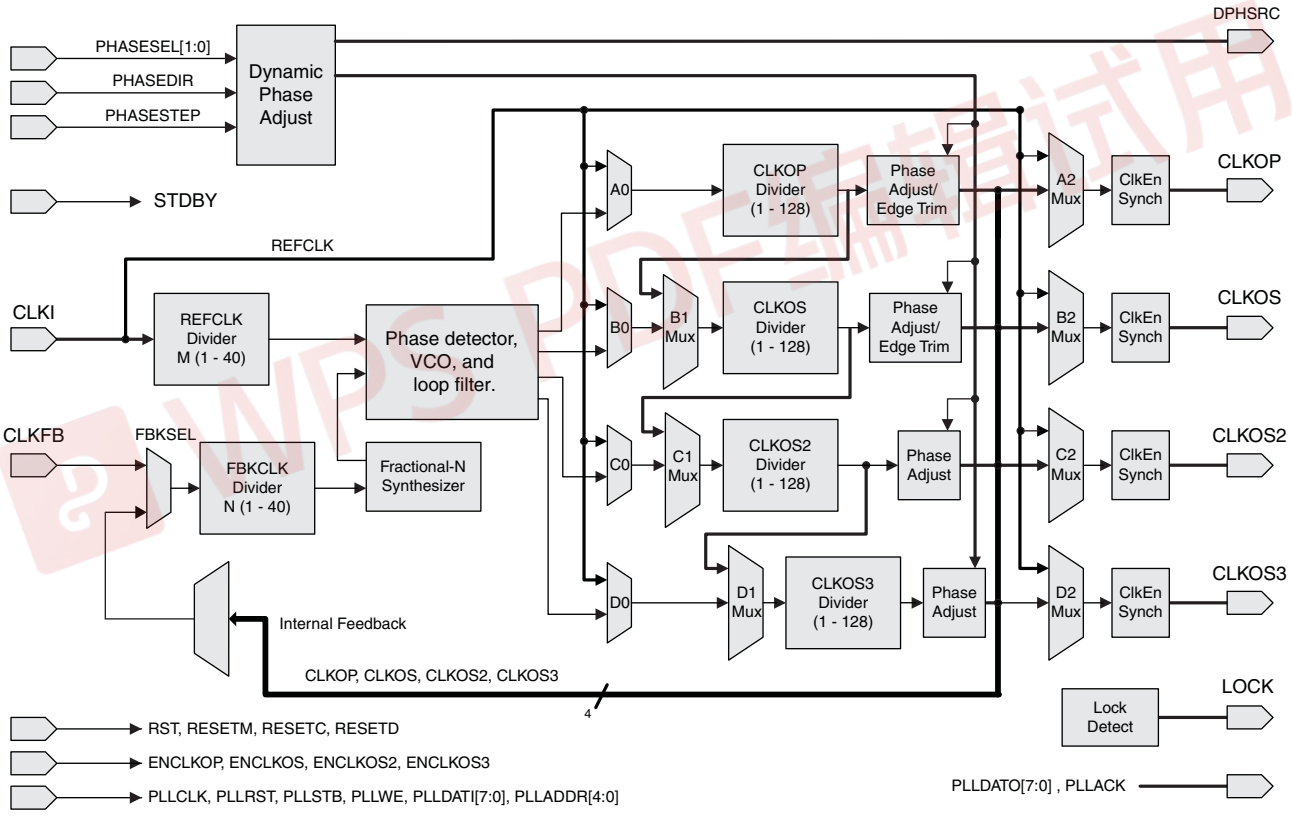


Table 2-4 provides signal descriptions of the PLL block.

Table 2-4. PLL Signal Descriptions

Port Name	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	I	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	I	Dynamic Phase step – toggle shifts VCO phase adjust by one step.

Table 2-4. PLL Signal Descriptions (Continued)

Port Name	I/O	Description
CLKOP	O	Primary PLL output clock (with phase shift adjustment)
CLKOS	O	Secondary PLL output clock (with phase shift adjust)
CLKOS2	O	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	O	Secondary PLL output clock3 (with phase shift adjust)
LOCK	O	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feedback signals.
DPHSRC	O	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset - includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	O	PLL data bus data output
PLLACK	O	PLL data bus acknowledge signal

sysMEM Embedded Block RAM Memory

The MachXO2-640/U and larger devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO2 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

Figure 2-8. sysMEM Memory Primitives

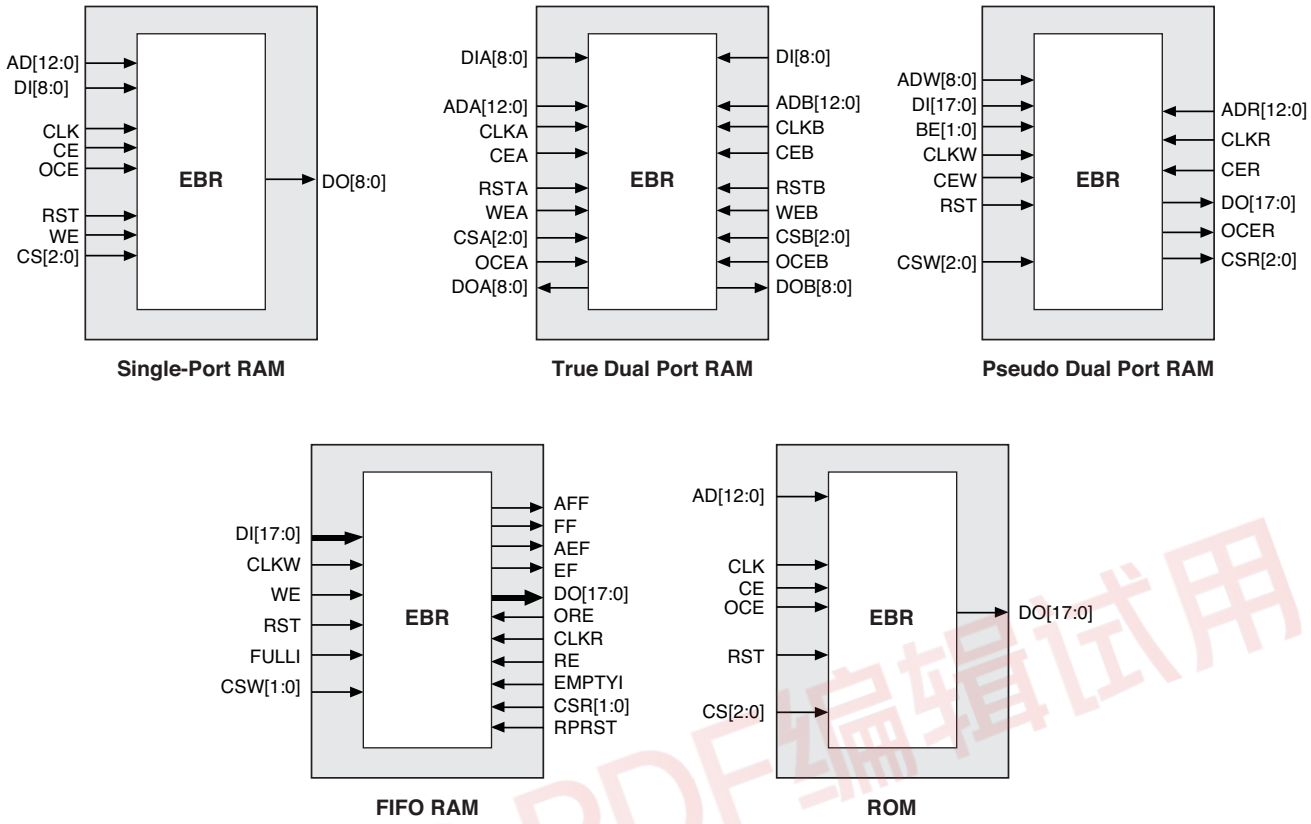


Table 2-6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE[1]	Output Clock Enable	Active High
RST	Reset	Active High
BE[1]	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	—
DI	Data In	—
DO	Data Out	—
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	—
FF	FIFO RAM Full Flag	—
AEF	FIFO RAM Almost Empty Flag	—
EF	FIFO RAM Empty Flag	—
RPRST	FIFO RAM Read Pointer Reset	—

1. Optional signals.
2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.

3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

Table 2-7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

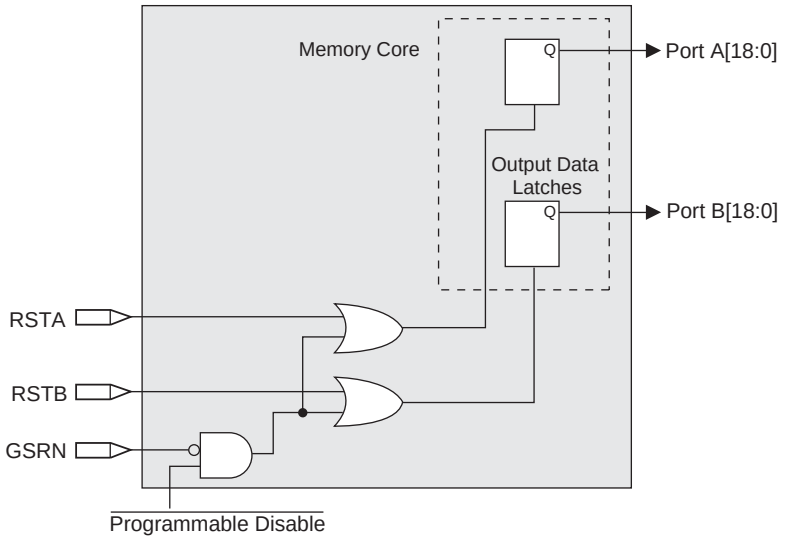
N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

Figure 2-9. Memory Core Reset

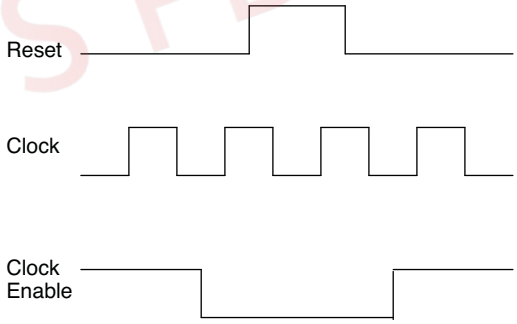


For further information on the sysMEM EBR block, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-10. The reset timing rules apply to the RPReset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For more details refer to TN1201, Memory Usage Guide for MachXO2 Devices.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

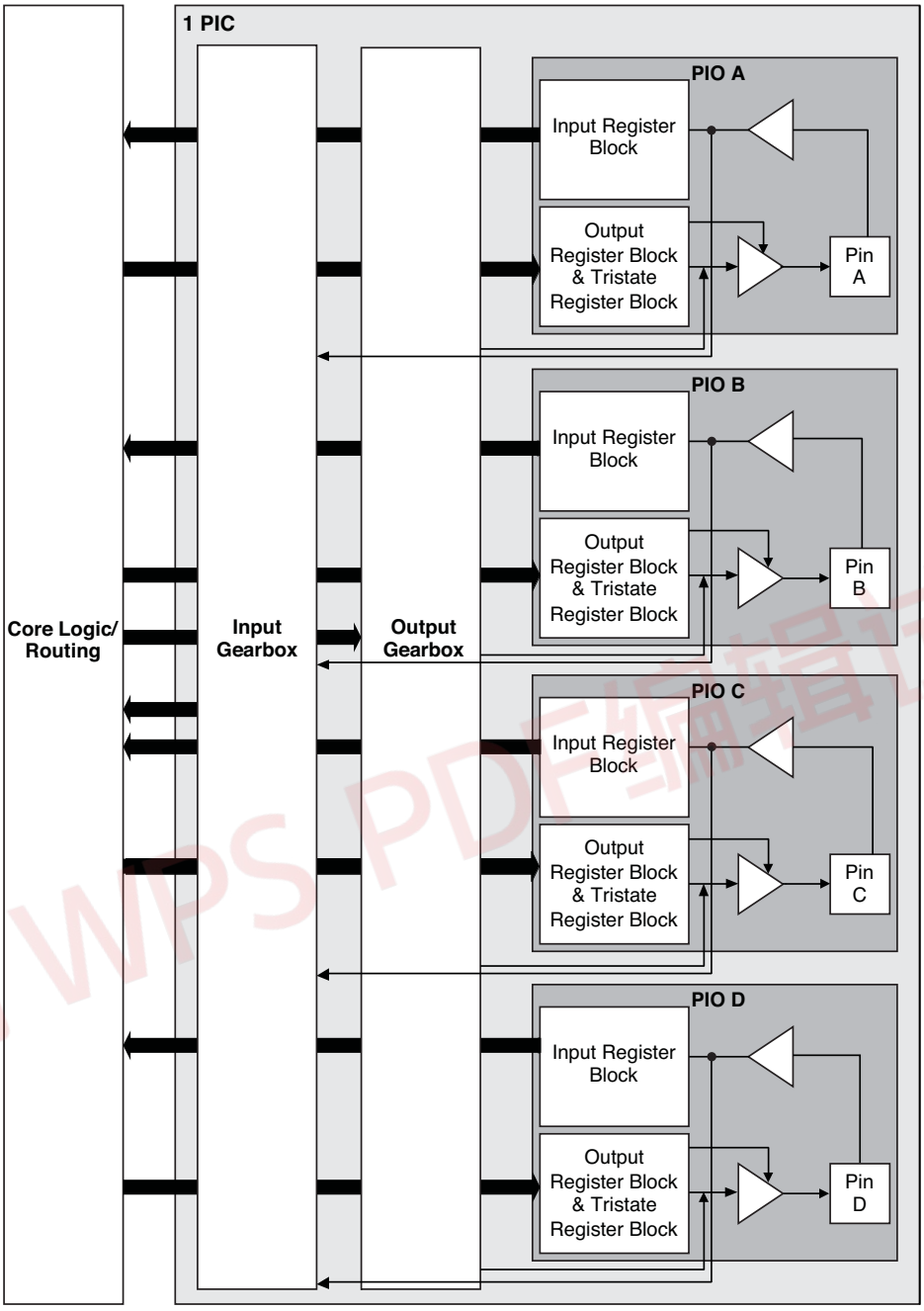
Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO2 devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO2 devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

The MachXO2-640U, MachXO2-1200/U and higher density devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these higher density devices have on-chip differential termination and also provide PCI support.

Figure 2-11. Group of Four Programmable I/O Cells



Notes:
1. Input gearbox is available only in PIC on the bottom edge of MachXO2-640U, MachXO2-1200/U and larger devices.
2. Output gearbox is available only in PIC on the top edge of MachXO2-640U, MachXO2-1200/U and larger devices.

PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Table 2-8. PIO Signal List

Pin Name	I/O Type	Description
CE	Input	Clock Enable
D	Input	Pin input from sysIO buffer.
INDD	Output	Register bypassed input.
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysIO Buffer
TQ	Output	Tri-state output signals to sysIO Buffer
DQSR90[1]	Input	DQS shift 90-degree read clock
DQSW90[1]	Input	DQS shift 90-degree write clock
DDRCLKPOL[1]	Input	DDR input register polarity control signal from DQS
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

1. Available in PIO on right edge only.

Input Register Block

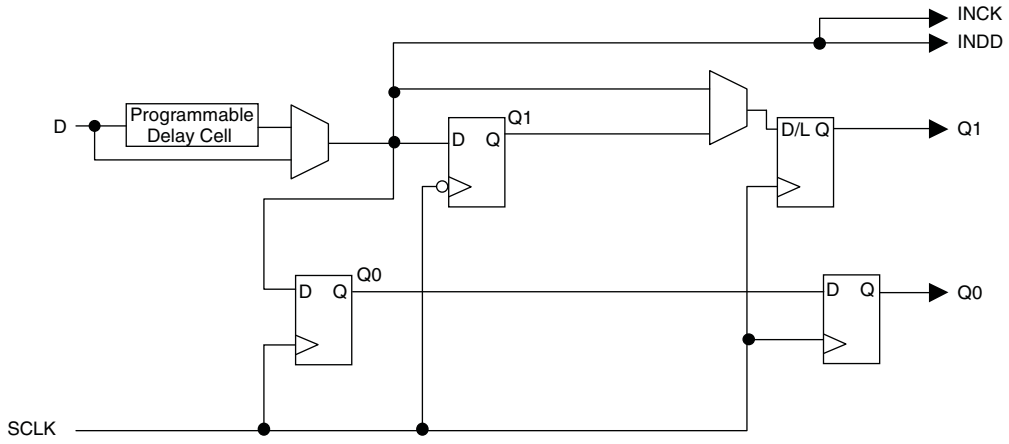
The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition to this functionality, the input register blocks for the PIOs on the right edge include built-in logic to interface to DDR memory.

Figure 2-12 shows the input register block for the PIOs located on the left, top and bottom edges. Figure 2-13 shows the input register block for the PIOs on the right edge.

Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

Figure 2-12. MachXO2 Input Register Block Diagram (PIO on Left, Top and Bottom Edges)



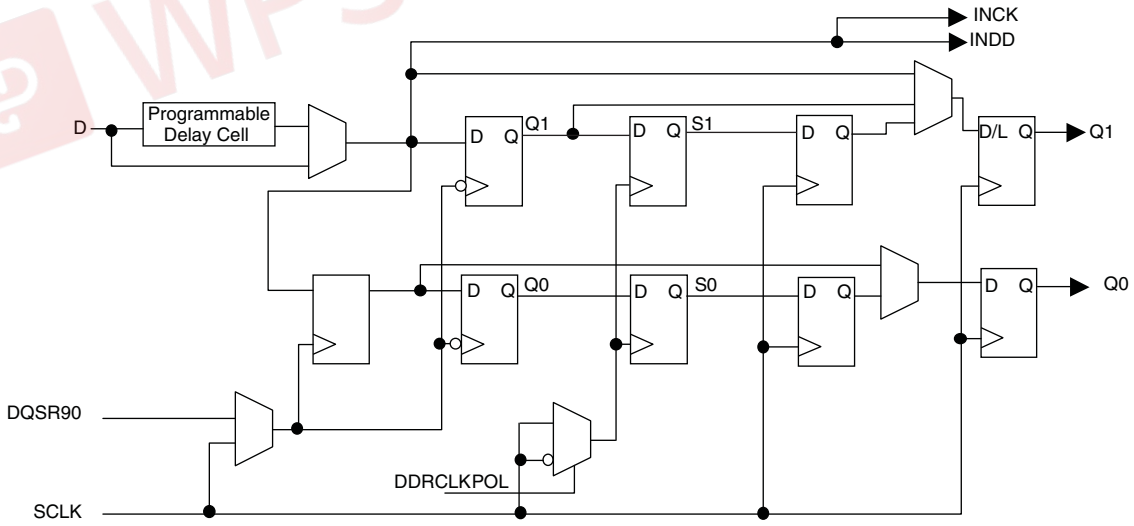
Right Edge

The input register block on the right edge is a superset of the same block on the top, bottom, and left edges. In addition to the modes described above, the input register block on the right edge also supports DDR memory mode.

In DDR memory mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (DQSR90) in the DDR Memory mode creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the DQS domain. The DQSR90 and DDRCLKPOL signals are generated in the DQS read-write block.

Figure 2-13. MachXO2 Input Register Block Diagram (PIO on Right Edge)



Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

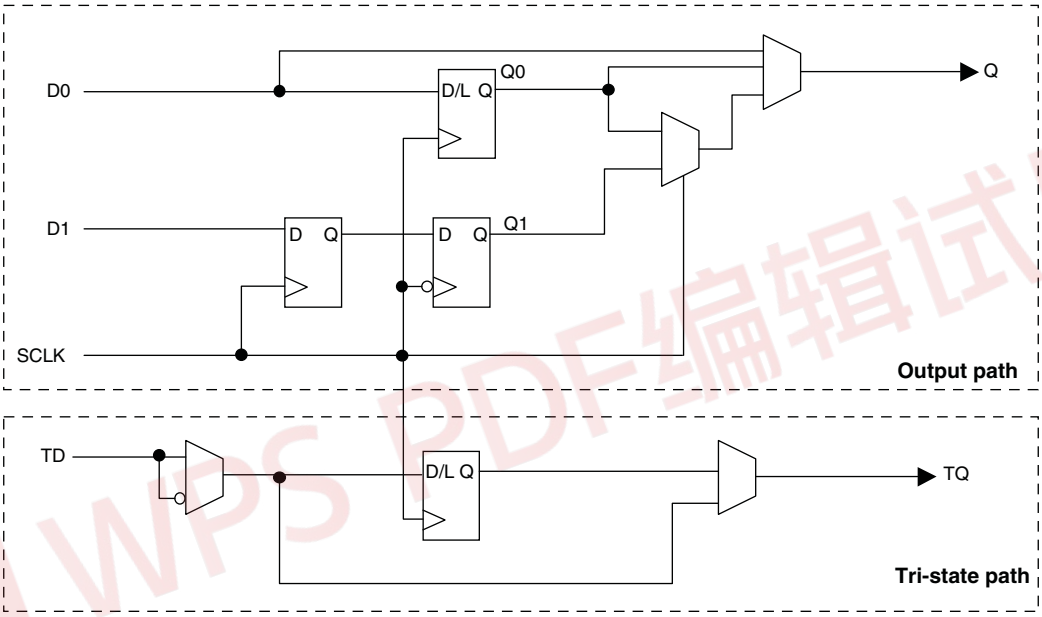
Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-14 shows the output register block on the left, top and bottom edges.

Figure 2-14. MachXO2 Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)



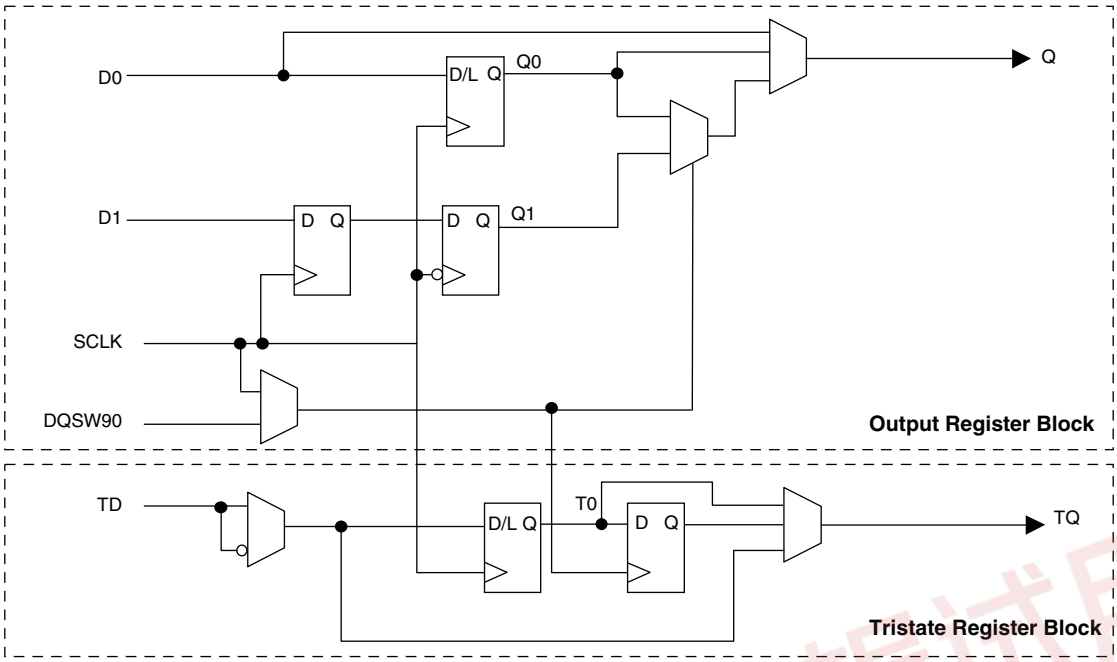
Right Edge

The output register block on the right edge is a superset of the output register on left, top and bottom edges of the device. In addition to supporting SDR and Generic DDR modes, the output register blocks for PIOs on the right edge include additional logic to support DDR-memory interfaces. Operation of this block is similar to that of the output register block on other edges.

In DDR memory mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the DQSW90 signal is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-15 shows the output register block on the right edge.

Figure 2-15. MachXO2 Output Register Block Diagram (PIO on the Right Edges)



Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

The tri-state register blocks on the right edge contain an additional register for DDR memory operation. In DDR memory mode, the register TS input is fed into another register that is clocked using the DQSW90 signal. The output of this register is used as a tri-state control.

Input Gearbox

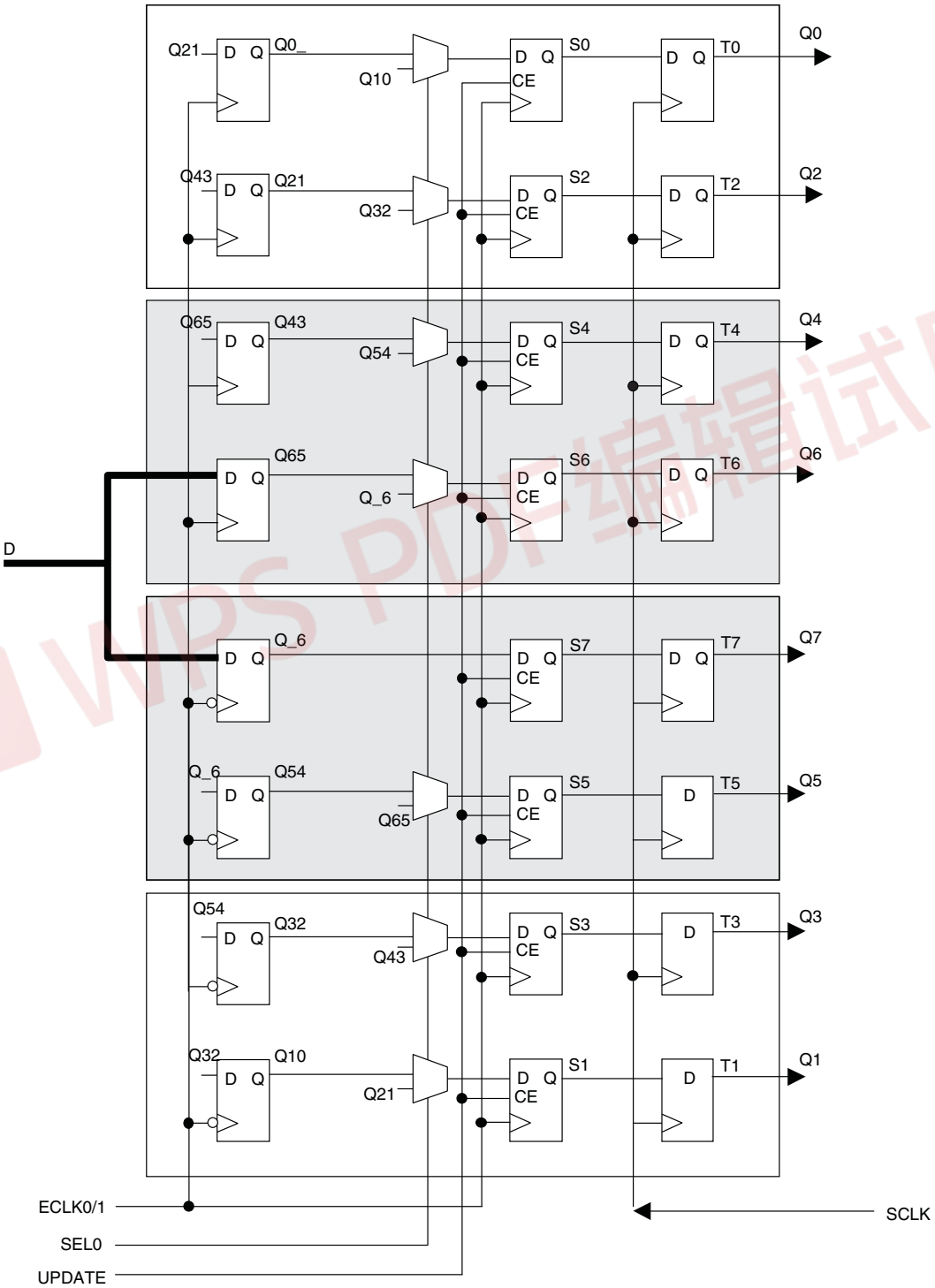
Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

Table 2-9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-16 shows a block diagram of the input gearbox.

Figure 2-16. Input Gearbox



More information on the input gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.

Output Gearbox

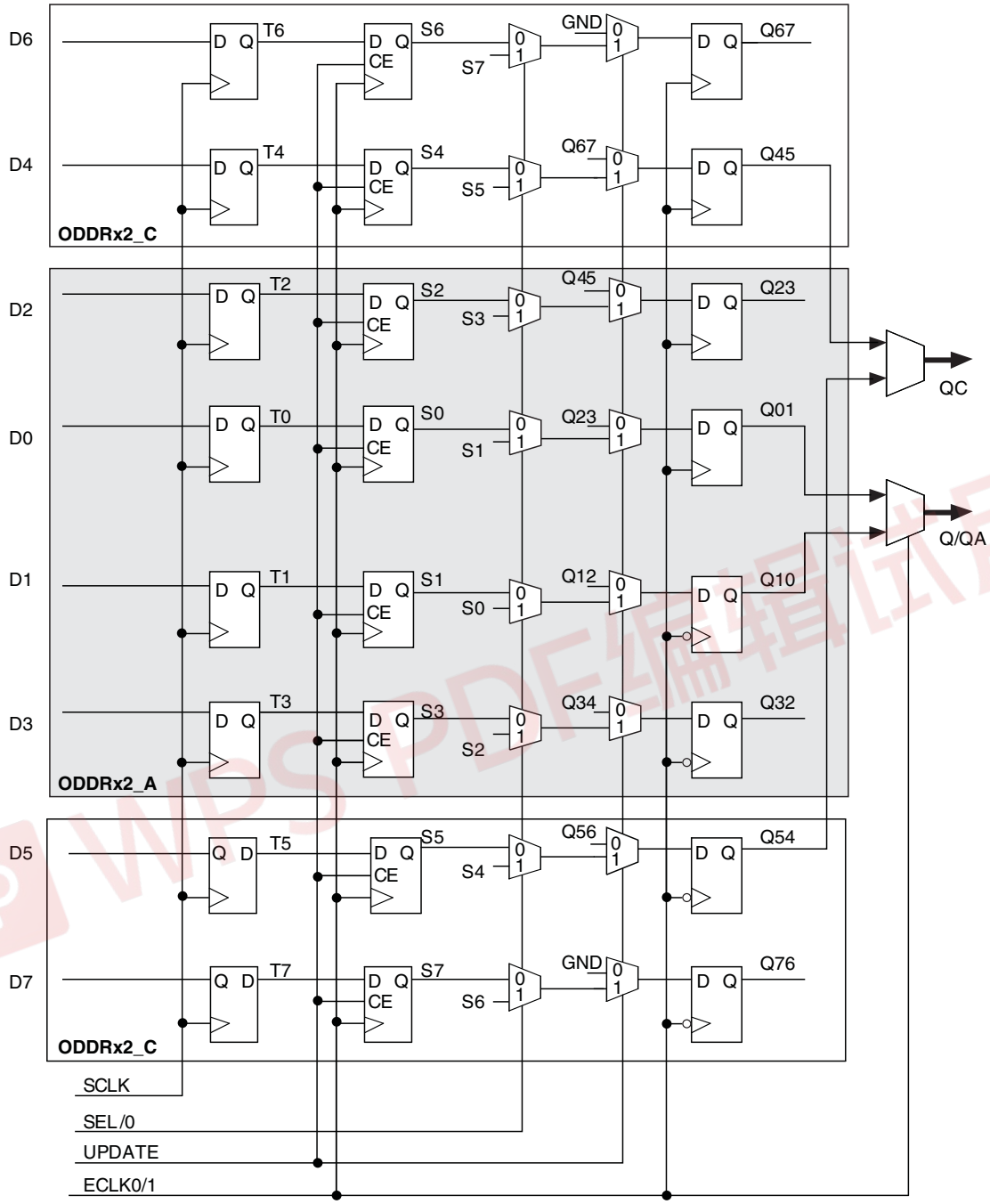
Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

Table 2-10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDRX4(8:1): D[7:0]		
GDDRX2(4:1)(IOL-A): D[3:0]		
GDDRX2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-17 shows the output gearbox block diagram.

Figure 2-17. Output Gearbox



More information on the output gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.

DDR Memory Support

Certain PICs on the right edge of MachXO2-640U, MachXO2-1200/U and larger devices, have additional circuitry to allow the implementation of DDR memory interfaces. There are two groups of 14 or 12 PIOs each on the right edge with additional circuitry to implement DDR memory interfaces. This capability allows the implementation of up to 16-bit wide memory interfaces. One PIO from each group contains a control element, the DQS Read/Write Block, to facilitate the generation of clock and control signals (DQSR90, DQSW90, DDRCLKPOL and DATAVALID). These clock and control signals are distributed to the other PIO in the group through dedicated low skew routing.

DQS Read Write Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Read Write block provides the required clock alignment for DDR memory interfaces. DQSR90 and DQSW90 signals are generated by the DQS Read Write block from the DQS input.

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the read cycle) is unknown. The MachXO2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This circuit changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each read cycle for the correct clock polarity. Prior to the read operation in DDR memories, DQS is in tri-state (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit in the DQS Read Write block detects the first DQS rising edge after the preamble state and generates the DDRCLKPOL signal. This signal is used to control the polarity of the clock to the synchronizing registers.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration signals (6-bit bus) from a DLL on the right edge of the device. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, PCI, SSTL, HSTL, LVDS, BLVDS, MLVDS and LVPECL.

Each bank is capable of supporting multiple I/O standards. In the MachXO2 devices, single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS and PCI), differential (LVDS) and referenced input buffers (SSTL and HSTL) are powered using I/O supply voltage (V_{CCIO}). Each sysIO bank has its own V_{CCIO}. In addition, each bank has a voltage reference, V_{REF}, which allows the use of referenced input buffers independent of the bank V_{CCIO}.

MachXO2-256 and MachXO2-640 devices contain single-ended ratioed input buffers and single-ended output buffers with complementary outputs on all the I/O banks. Note that the single-ended input buffers on these devices do not contain PCI clamps. In addition to the single-ended I/O buffers these two devices also have differential and referenced input buffers on all I/Os. The I/Os are arranged in pairs, the two pads in the pair are described as "T" and "C", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 devices contain three types of sysIO buffer pairs.

1. **Left and Right sysIO Buffer Pairs**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential and referenced input buffers.

2. **Bottom sysIO Buffer Pairs**
   The sysIO buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential and referenced input buffers. Only the I/Os on the bottom banks have programmable PCI clamps and differential input termination. The PCI clamp is enabled after V_{CC} and V_{CCIO} are at valid operating levels and the device has been configured.

3. **Top sysIO Buffer Pairs**
   The sysIO buffer pairs in the top bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential and referenced I/O buffers. Half of the sysIO buffer pairs on the top edge have true differential outputs. The sysIO buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver. The referenced input buffer can also be configured as a differential input buffer.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCIO0} have reached V_{PORUP} level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-down to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to V_{CCIO} as the default functionality). The I/O pins will maintain the blank configuration until V_{CC} and V_{CCIO} (for I/O banks containing configuration I/Os) have reached V_{PORUP} levels at which time the I/Os will take on the user-configured settings only after a proper download/configuration.

Supported Standards

The MachXO2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL, and PCI. The buffer supports the LVTTL, PCI, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO2-640U, MachXO2-1200/U and higher devices support on-chip LVDS output buffers on approximately 50% of the I/Os on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO2 devices. PCI support is provided in the bottom bank of theMachXO2-640U, MachXO2-1200/U and higher density devices. Table 2-11 summarizes the I/O characteristics of the MachXO2 PLDs.

Tables 2-11 and 2-12 show the I/O standards (together with their supply and reference voltages) supported by the MachXO2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1202, MachXO2 sysIO Usage Guide.

Table 2-11. I/O Support Device by Device

	MachXO2-256, MachXO2-640	MachXO2-640U, MachXO2-1200	MachXO2-1200U MachXO2-2000/U, MachXO2-4000, MachXO2-7000
Number of I/O Banks	4	4	6
Type of Input Buffers	Single-ended (all I/O banks) Differential Receivers (all I/O banks)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)
Types of Output Buffers	Single-ended buffers with complementary outputs (all I/O banks)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)
Differential Output Emulation Capability	All I/O banks	All I/O banks	All I/O banks
PCI Clamp Support	No	Clamp on bottom side only	Clamp on bottom side only

Table 2-12. Supported Input Standards

	VCCIO (Typ.)				
Input Standard	**3.3 V**	**2.5 V**	**1.8 V**	**1.5**	**1.2 V**
Single-Ended Interfaces					
LVTTL	✓	✓[2]	✓[2]	✓[2]	
LVCMOS33	✓	✓[2]	✓[2]	✓[2]	
LVCMOS25	✓[2]	✓	✓[2]	✓[2]	
LVCMOS18	✓[2]	✓[2]	✓	✓[2]	
LVCMOS15	✓[2]	✓[2]	✓[2]	✓	✓[2]
LVCMOS12	✓[2]	✓[2]	✓[2]	✓[2]	✓
PCI[1]	✓				
SSTL18 (Class I, Class II)	✓	✓	✓		
SSTL25 (Class I, Class II)	✓	✓			
HSTL18 (Class I, Class II)	✓	✓	✓		
Differential Interfaces					
LVDS	✓	✓			
BLVDS, MVDS, LVPECL, RSDS	✓	✓			
MIPI[3]	✓	✓			
Differential SSTL18 Class I, II	✓	✓	✓		
Differential SSTL25 Class I, II	✓	✓			
Differential HSTL18 Class I, II	✓	✓	✓		

1. Bottom banks of MachXO2-640U, MachXO2-1200/U and higher density devices only.
2. Reduced functionality. Refer to TN1202, MachXO2 sysIO Usage Guide for more detail.
3. These interfaces can be emulated with external resistors in all devices.

Table 2-13. Supported Output Standards

Output Standard	V_{CCIO} (Typ.)
Single-Ended Interfaces	
LVTTL	3.3
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8
LVCMOS15	1.5
LVCMOS12	1.2
LVCMOS33, Open Drain	—
LVCMOS25, Open Drain	—
LVCMOS18, Open Drain	—
LVCMOS15, Open Drain	—
LVCMOS12, Open Drain	—
PCI33	3.3
SSTL25 (Class I)	2.5
SSTL18 (Class I)	1.8
HSTL18(Class I)	1.8
Differential Interfaces	
LVDS[1, 2]	2.5, 3.3
BLVDS, MLVDS, RSDS [2]	2.5
LVPECL[2]	3.3
MIPI[2]	2.5
Differential SSTL18	1.8
Differential SSTL25	2.5
Differential HSTL18	1.8

1. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.

sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO2-1200U, MachXO2-2000/U and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO2-1200 and lower density devices have four banks (one bank per side). Figures 2-18 and 2-19 show the sysIO banks and their associated supplies for all devices.

Figure 2-18. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 Banks

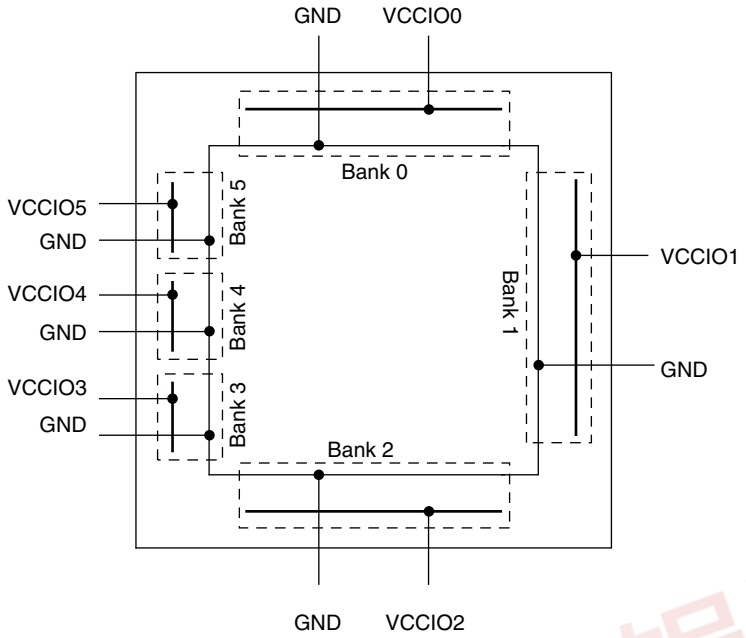
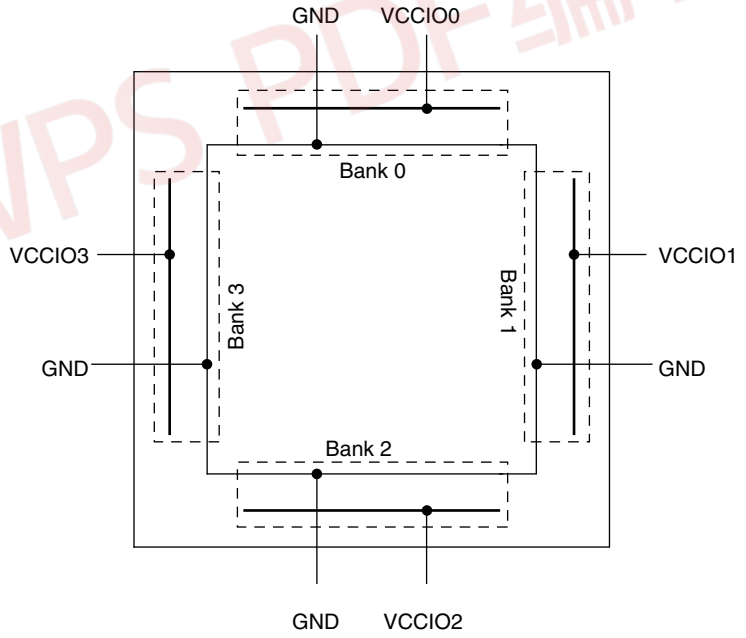


Figure 2-19. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks



Hot Socketing

The MachXO2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO2 ideal for many multiple power supply and hot-swap applications.

On-chip Oscillator

Every MachXO2 device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
2. During configuration, users select a different master clock frequency.
3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-14 lists all the available MCLK frequencies.

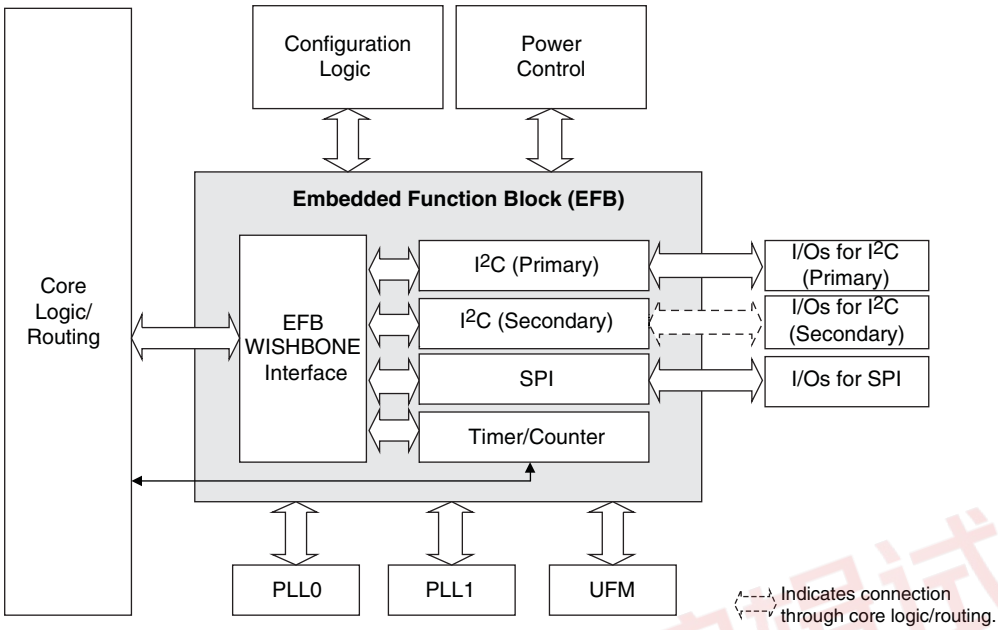
Table 2-14. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

Embedded Hardened IP Functions and User Flash Memory

All MachXO2 devices provide embedded hardened functions such as SPI, I^2C and Timer/Counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2-20.

Figure 2-20. Embedded Function Block Interface



Hardened I²C IP Core

Every MachXO2 device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I²C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface

Figure 2-21. I²C Core Block Diagram

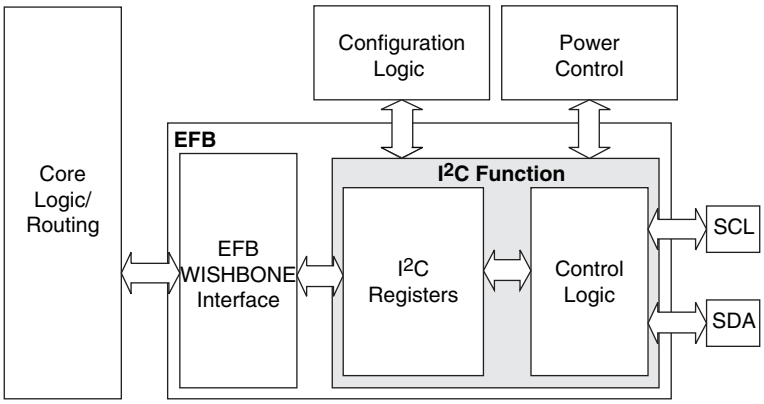


Table 2-15 describes the signals interfacing with the I²C cores.

Table 2-15. I²C Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I²C core. The signal is an output if the I²C core is in master mode. The signal is an input if the I²C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device.
i2c_sda	Bi-directional	Bi-directional data line of the I²C core. The signal is an output when data is transmitted from the I²C core. The signal is an input when data is received into the I²C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device.
i2c_irqo	Output	Interrupt request output signal of the I²C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I²C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.

Hardened SPI IP Core

Every MachXO2 device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO2 devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface

There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology (Appendix B)
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices

Figure 2-22. SPI Core Block Diagram

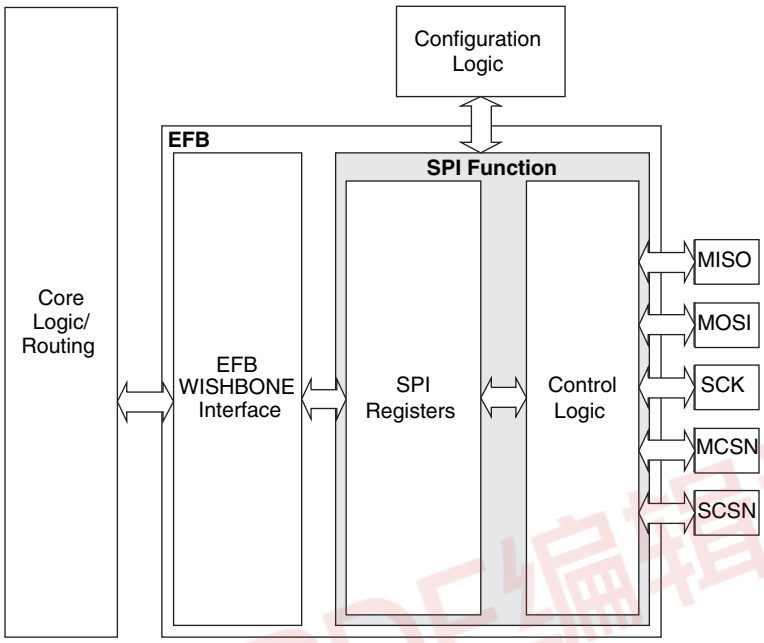


Table 2-16 describes the signals interfacing with the SPI cores.

Table 2-16. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	O	Master	SPI master chip-select output
spi_csn[1..7]	O	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	O	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
ufm_sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the User Flash Memory (UFM).
cfg_stdby	O	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.
cfg_wake	O	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.

Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  - — Watchdog timer
  - — Clear timer on compare match
  - — Fast PWM
  - — Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

Figure 2-23. Timer/Counter Block Diagram

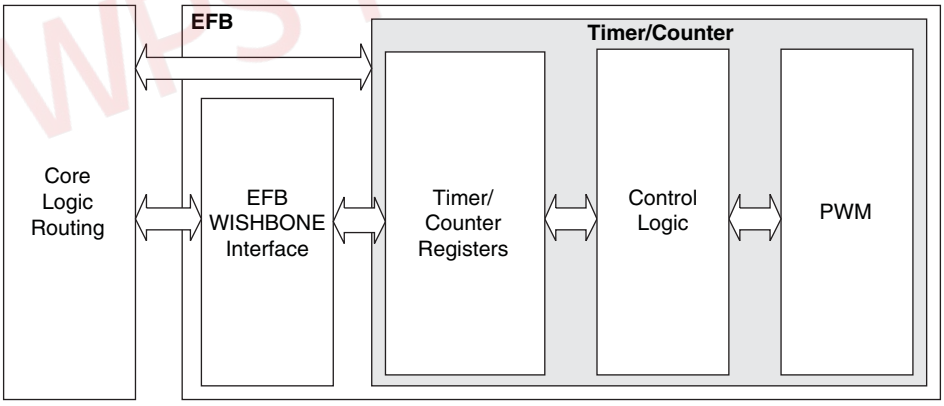


Table 2-17. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	O	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	O	Timer counter output signal

For more details on these embedded functions, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

User Flash Memory (UFM)

MachXO2-640/U and higher density devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I^2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

Standby Mode and Power Saving Options

MachXO2 devices are available in three options for maximum flexibility: ZE, HC and HE devices. The ZE devices have ultra low static and dynamic power consumption. These devices use a 1.2 V core voltage that further reduces power consumption. The HC and HE devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the HE devices operate at 1.2 V V_{CC}.

MachXO2 devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO2 devices support an ultra low power Stand-by mode. While most of these features are available in all three device types, these features are mainly intended for use with MachXO2 ZE devices to manage power consumption.

In the stand-by mode the MachXO2 devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I^2C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO2 devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

Table 2-18. MachXO2 Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe V_{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1198, Power Estimation and Management for MachXO2 Devices.

Power On Reset

MachXO2 devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the V_{PORUP} level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices), V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators (HC devices), V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time ($t_{REFRESH}$) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tristate. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min) they should not shut down the bandgap or POR circuit.

Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I^2C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

1. Internal Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I^2C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, MachXO2 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

TransFR (Transparent Field Reconfiguration)
TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

When implementing background programming of the on-chip Flash, care must be taken for the operation of the PLL. For devices that have two PLLs (XO2-2000U, -4000 and -7000), the system must put the RPLL (Right-side PLL) in reset state during the background Flash programming. More detailed description can be found in TN1204, MachXO2 Programming and Configuration Usage Guide.

Security and One-Time Programmable Mode (OTP)
For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO2 devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile Flash memory spaces. The device can be in one of two modes:

1. Unlocked – Readback of the SRAM configuration and non-volatile Flash memory spaces is allowed.

2. Permanently Locked – The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Dual Boot
MachXO2 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the on-chip Flash. The golden image MUST reside in an external SPI Flash. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Soft Error Detection
The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1206, MachXO2 Soft Error Detection Usage Guide.

TraceID

Each MachXO2 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I^2C, or JTAG interfaces.

Density Shifting

The MachXO2 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO2 migration files.

MachXO2 Family Data Sheet DC and Switching Characteristics

March 2017 Data Sheet DS1035

Absolute Maximum Ratings[1, 2, 3]

	MachXO2 ZE/HE (1.2 V)	MachXO2 HC (2.5 V / 3.3 V)
Supply Voltage V_{CC}	–0.5 V to 1.32 V	–0.5 V to 3.75 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied[4, 5]	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied[4]	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T_J)	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to (V_{IHMAX} + 2) volts is permitted for a duration of <20 ns.
5. The dual function I^2C pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.

Recommended Operating Conditions[1]

Symbol	Parameter	Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V / 3.3 V Devices	2.375	3.6	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	1.14	3.6	V
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature Industrial Operation	–40	100	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

Power Supply Ramp Rates[1]

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.01	—	100	V/ms

1. Assumes monotonic ramp rates.

Power-On-Reset Voltage Levels[1, 2, 3, 4, 5]

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and V_{CCIO0})	0.9	—	1.06	V
$V_{PORUPEXT}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	—	2.1	V
$V_{PORDNBG}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CCINT})	0.75	—	0.93	V
$V_{PORDNBGEXT}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	—	1.33	V
$V_{PORDNSRAM}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CCINT})	—	0.6	—	V
$V_{PORDNSRAMEXT}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	—	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.
3. Note that V_{PORUP} (min.) and $V_{PORDNBG}$ (max.) are in different process corners. For any given process corner $V_{PORDNBG}$ (max.) is always 12.0 mV below V_{PORUP} (min.).
4. $V_{PORUPEXT}$ is for HC devices only. In these devices a separate POR circuit monitors the external V_{CC} power supply.
5. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

Programming/Erase Specifications

Symbol	Parameter	Min.	Max.[1]	Units
$N_{PROGCYC}$	Flash Programming cycles per $t_{RETENTION}$	—	10,000	Cycles
	Flash functional programming cycles	—	100,000	
$t_{RETENTION}$	Data retention at 100 °C junction temperature	10	—	Years
	Data retention at 85 °C junction temperature	20	—	

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Max.	Units
I_{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/–1000	µA

1. Insensitive to sequence of V_{CC} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO}.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

ESD Performance

Please refer to the MachXO2 Product Family Qualification Summary for complete qualification data, including ESD performance.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4]	Input or I/O Leakage	Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX)	—	—	+175	µA
		Clamp OFF and $V_{IN} = V_{CCIO}$	–10	—	10	µA
		Clamp OFF and V_{CCIO} –0.97 V < V_{IN} < V_{CCIO}	–175	—	—	µA
		Clamp OFF and 0 V < V_{IN} < V_{CCIO} –0.97 V	—	—	10	µA
		Clamp OFF and V_{IN} = GND	—	—	10	µA
		Clamp ON and 0 V < V_{IN} < V_{CCIO}	—	—	10	µA
I_{PU}	I/O Active Pull-up Current	0 < V_{IN} < 0.7 V_{CCIO}	–30	—	-309	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) < V_{IN} < V_{CCIO}	30	—	305	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	–30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	305	µA
I_{BHHO}	Bus Hold High Overdrive current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	–309	µA
V_{BHT}[3]	Bus Hold Trip Points		V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	3	5	9	pF
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	3	5.5	7	pF
V_{HYST}	Hysteresis for Schmitt Trigger Inputs[5]	V_{CCIO} = 3.3 V, Hysteresis = Large	—	450	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Large	—	250	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Large	—	125	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Large	—	100	—	mV
		V_{CCIO} = 3.3 V, Hysteresis = Small	—	250	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Small	—	150	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Small	—	60	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Small	—	40	—	mV

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. When V_{IH} is higher than V_{CCIO}, a transient current typically of 30 ns in duration or less with a peak current of 6 mA can occur on the high-to-low transition. For true LVDS output pins in MachXO2-640U, MachXO2-1200/U and larger devices, V_{IH} must be less than or equal to V_{CCIO}.
5. With bus keeper circuit turned on. For more details, refer to TN1202, MachXO2 sysIO Usage Guide.

Static Supply Current – ZE Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO2-256ZE	18	µA
		LCMXO2-640ZE	28	µA
		LCMXO2-1200ZE	56	µA
		LCMXO2-2000ZE	80	µA
		LCMXO2-4000ZE	124	µA
		LCMXO2-7000ZE	189	µA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	1	µA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off. To estimate the impact of turning each of these items on, please refer to the following table or for more detail with your specific design use the Power Calculator tool.
3. Frequency = 0 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Static Power Consumption Contribution of Different Components – ZE Devices

The table below can be used for approximating static power consumption. For a more accurate power analysis for your design please use the Power Calculator tool.

Symbol	Parameter	Typ.	Units
I_{DCBG}	Bandgap DC power contribution	101	µA
I_{DCPOR}	POR DC power contribution	38	µA
$I_{DCIOBANKCONTROLLER}$	DC power contribution per I/O bank controller	143	µA

Static Supply Current – HC/HE Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO2-256HC	1.15	mA
		LCMXO2-640HC	1.84	mA
		LCMXO2-640UHC	3.48	mA
		LCMXO2-1200HC	3.49	mA
		LCMXO2-1200UHC	4.80	mA
		LCMXO2-2000HC	4.80	mA
		LCMXO2-2000UHC	8.44	mA
		LCMXO2-4000HC	8.45	mA
		LCMXO2-7000HC	12.87	mA
		LCMXO2-2000HE	1.39	mA
		LCMXO2-4000HE	2.55	mA
		LCMXO2-7000HE	4.06	mA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
3. Frequency = 0 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Programming and Erase Flash Supply Current – HC/HE Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO2-256HC	14.6	mA
		LCMXO2-640HC	16.1	mA
		LCMXO2-640UHC	18.8	mA
		LCMXO2-1200HC	18.8	mA
		LCMXO2-1200UHC	22.1	mA
		LCMXO2-2000HC	22.1	mA
		LCMXO2-2000UHC	26.8	mA
		LCMXO2-4000HC	26.8	mA
		LCMXO2-7000HC	33.2	mA
		LCMXO2-2000HE	18.3	mA
		LCMXO2-2000UHE	20.4	mA
		LCMXO2-4000HE	20.4	mA
		LCMXO2-7000HE	23.9	mA
I_{CCIO}	Bank Power Supply[6]	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. T_J = 25 °C, power supplies at nominal voltage.
6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

Programming and Erase Flash Supply Current – ZE Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO2-256ZE	13	mA
		LCMXO2-640ZE	14	mA
		LCMXO2-1200ZE	15	mA
		LCMXO2-2000ZE	17	mA
		LCMXO2-4000ZE	18	mA
		LCMXO2-7000ZE	20	mA
I_{CCIO}	Bank Power Supply[6]	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. TJ = 25 °C, power supplies at nominal voltage.
6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.6	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.6	—	—	—
PCI[3]	3.135	3.3	3.6	—	—	—
SSTL25	2.375	2.5	2.625	1.15	1.25	1.35
SSTL18	1.71	1.8	1.89	0.833	0.9	0.969
HSTL18	1.71	1.8	1.89	0.816	0.9	1.08
LVCMOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVCMOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVCMOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVCMOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVCMOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVCMOS12R33[4]	3.135	3.3	3.6	0.45	0.6	0.75
LVCMOS12R25[4]	2.375	2.5	2.625	0.45	0.6	0.75
LVCMOS10R33[4]	3.135	3.3	3.6	0.35	0.5	0.65
LVCMOS10R25[4]	2.375	2.5	2.625	0.35	0.5	0.65
LVDS25[1, 2]	2.375	2.5	2.625	—	—	—
LVDS33[1, 2]	3.135	3.3	3.6	—	—	—
LVPECL[1]	3.135	3.3	3.6	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—
RSDS[1]	2.375	2.5	2.625	—	—	—
SSTL18D	1.71	1.8	1.89	—	—	—
SSTL25D	2.375	2.5	2.625	—	—	—
HSTL18D	1.71	1.8	1.89	—	—	—

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
3. Input on the bottom bank of the MachXO2-640U, MachXO2-1200/U and larger devices only.
4. Supported only for inputs and BIDIs for all ZE devices, and –6 speed grade for HE and HC devices.

sysIO Single-Ended DC Electrical Characteristics[1, 2]

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max.[4] (mA)	I_{OH} Max.[4] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3 LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
							16	–16
							24	–24
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
							16	–16
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.5	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.2	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} – 0.4	4	–2
							8	–6
					0.2	V_{CCIO} – 0.2	0.1	–0.1
PCI	–0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	–0.5
SSTL25 Class I	–0.3	V_{REF} – 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	8	8
SSTL25 Class II	–0.3	V_{REF} – 0.18	V_{REF} + 0.18	3.6	NA	NA	NA	NA
SSTL18 Class I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	3.6	0.40	V_{CCIO} - 0.40	8	8
SSTL18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	3.6	NA	NA	NA	NA
HSTL18 Class I	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	V_{CCIO} - 0.40	8	8
HSTL18 Class II	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS25R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS12R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max.[4] (mA)	I_{OH} Max.[4] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS10R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain

1. MachXO2 devices allow LVCMOS inputs to be placed in I/O banks where V_{CCIO} is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO2 devices do not meet the relevant JEDEC specification are documented in the table below.
2. MachXO2 devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1202, MachXO2 sysIO Usage Guide.
3. The dual function I^2C pins SCL and SDA are limited to a V_{IL} min of –0.25 V or to –0.3 V with a duration of <10 ns.
4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive VCCIO or GND pad connections, or between the last VCCIO or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n * 8 mA. “n” is the number of I/O pads between the two consecutive bank VCCIO or GND connections or between the last VCCIO and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

Input Standard	V_{CCIO} (V)	V_{IL} Max. (V)
LVCMOS 33	1.5	0.685
LVCMOS 25	1.5	0.687
LVCMOS 18	1.5	0.655

sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of MachXO2-640U, MachXO2-1200/U and higher density devices in the MachXO2 PLD family.

LVDS

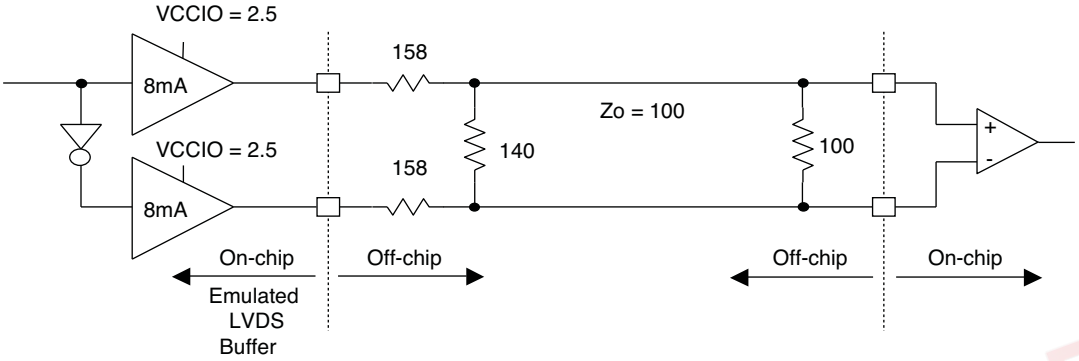
Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO} = 3.3 V	0	—	2.605	V
		V_{CCIO} = 2.5 V	0	—	2.05	V
V_{THD}	Differential Input Threshold		±100	—		mV
V_{CM}	Input Common Mode Voltage	V_{CCIO} = 3.3 V	0.05	—	2.6	V
		V_{CCIO} = 2.5 V	0.05	—	2.0	V
I_{IN}	Input current	Power on	—	—	±10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.375	—	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.90	1.025	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.395	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0 V driver outputs shorted	—	—	24	mA

LVDS Emulation

MachXO2 devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

Figure 3-1. LVDS Using External Resistors (LVDS25E)



Note: All resistors are ±1%.

Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	158	Ohms
R_P	Driver parallel resistor	140	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	6.03	mA

BLVDS

The MachXO2 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

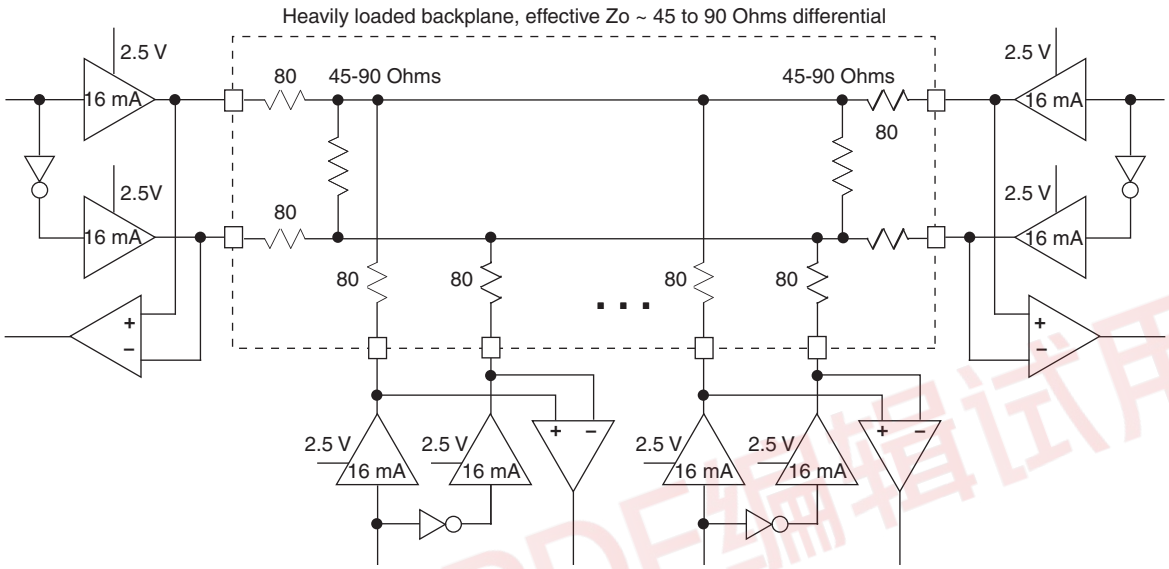


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	20	20	Ohms
R_S	Driver series resistance	80	80	Ohms
R_{TLEFT}	Left end termination	45	90	Ohms
R_{TRIGHT}	Right end termination	45	90	Ohms
V_{OH}	Output high voltage	1.376	1.480	V
V_{OL}	Output low voltage	1.124	1.020	V
V_{OD}	Output differential voltage	0.253	0.459	V
V_{CM}	Output common mode voltage	1.250	1.250	V
I_{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.

LVPECL

The MachXO2 family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

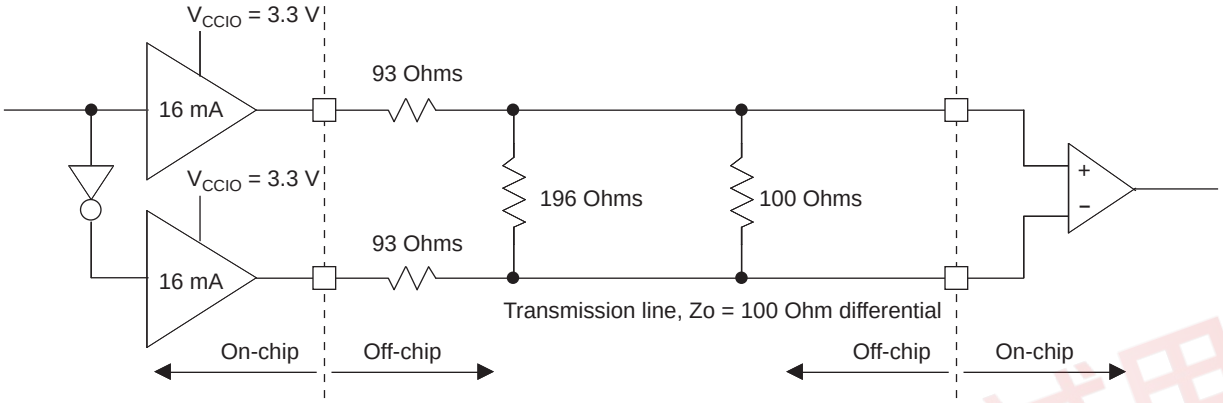


Table 3-3. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	93	Ohms
R_P	Driver parallel resistor	196	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	2.05	V
V_{OL}	Output low voltage	1.25	V
V_{OD}	Output differential voltage	0.80	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	12.11	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

RSDS

The MachXO2 family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

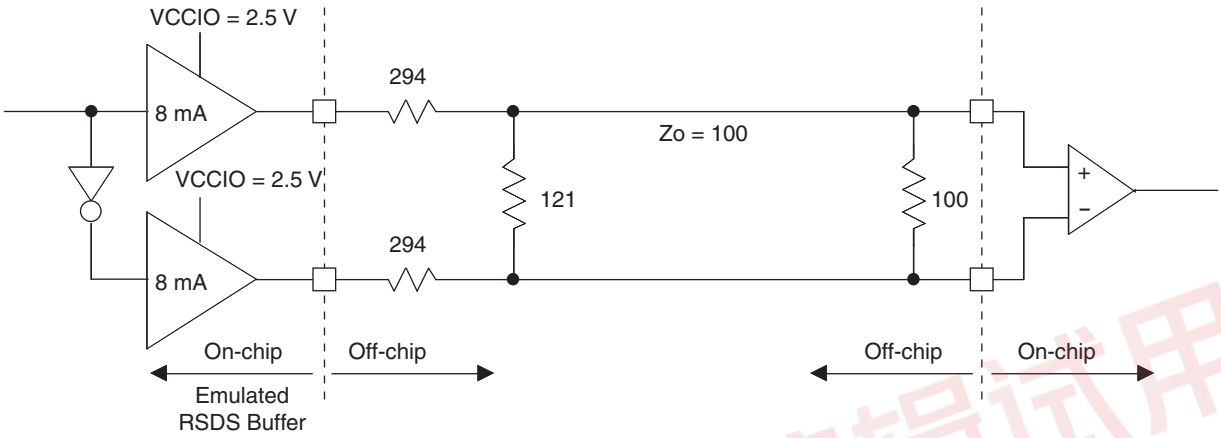


Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	294	Ohms
R_P	Driver parallel resistor	121	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	Ohms
I_{DC}	DC output current	3.66	mA

Typical Building Block Function Performance – HC/HE Devices[1]

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	-6 Timing	Units
Basic Functions		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

Register-to-Register Performance

Function	-6 Timing	Units
Basic Functions		
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

Typical Building Block Function Performance – ZE Devices[1]

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–3 Timing	Units
Basic Functions		
16-bit decoder	13.9	ns
4:1 MUX	10.9	ns
16:1 MUX	12.0	ns

Register-to-Register Performance

Function	–3 Timing	Units
Basic Functions		
16:1 MUX	191	MHz
16-bit adder	134	MHz
16-bit counter	148	MHz
64-bit counter	77	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	90	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	214	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
LVDS25	400	MHz
LVDS25E	150	MHz
RSDS25	150	MHz
RSDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
SSTL25_I	150	MHz
SSTL25_II	150	MHz
SSTL25D_I	150	MHz
SSTL25D_II	150	MHz
SSTL18_I	150	MHz
SSTL18_II	150	MHz
SSTL18D_I	150	MHz
SSTL18D_II	150	MHz
HSTL18_I	150	MHz
HSTL18_II	150	MHz
HSTL18D_I	150	MHz
HSTL18D_II	150	MHz
PCI33	134	MHz
LVTTL33	150	MHz
LVTTL33D	150	MHz
LVCMOS33	150	MHz
LVCMOS33D	150	MHz
LVCMOS25	150	MHz
LVCMOS25D	150	MHz
LVCMOS25R33	150	MHz
LVCMOS18	150	MHz
LVCMOS18D	150	MHz
LVCMOS18R33	150	MHz
LVCMOS18R25	150	MHz
LVCMOS15	150	MHz
LVCMOS15D	150	MHz
LVCMOS15R33	150	MHz
LVCMOS15R25	150	MHz
LVCMOS12	91	MHz
LVCMOS12D	91	MHz

MachXO2 External Switching Characteristics – HC/HE Devices[1, 2, 3, 4, 5, 6, 7]

Over Recommended Operating Conditions

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f_{MAX_PRI}[8]	Frequency for Primary Clock Tree	All MachXO2 devices	—	388	—	323	—	269	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	0.5	—	0.6	—	0.7	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO2-256HC-HE	—	912	—	939	—	975	ps
		MachXO2-640HC-HE	—	844	—	871	—	908	ps
		MachXO2-1200HC-HE	—	868	—	902	—	951	ps
		MachXO2-2000HC-HE	—	867	—	897	—	941	ps
		MachXO2-4000HC-HE	—	865	—	892	—	931	ps
		MachXO2-7000HC-HE	—	902	—	942	—	989	ps
Edge Clock									
f_{MAX_EDGE}[8]	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	400	—	333	—	278	MHz
Pin-LUT-Pin Propagation Delay									
t_{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	—	6.72	—	6.96	—	7.24	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t_{CO}	Clock to Output – PIO Output Register	MachXO2-256HC-HE	—	7.13	—	7.30	—	7.57	ns
		MachXO2-640HC-HE	—	7.15	—	7.30	—	7.57	ns
		MachXO2-1200HC-HE	—	7.44	—	7.64	—	7.94	ns
		MachXO2-2000HC-HE	—	7.46	—	7.66	—	7.96	ns
		MachXO2-4000HC-HE	—	7.51	—	7.71	—	8.01	ns
		MachXO2-7000HC-HE	—	7.54	—	7.75	—	8.06	ns
t_{SU}	Clock to Data Setup – PIO Input Register	MachXO2-256HC-HE	–0.06	—	–0.06	—	–0.06	—	ns
		MachXO2-640HC-HE	–0.06	—	–0.06	—	–0.06	—	ns
		MachXO2-1200HC-HE	–0.17	—	–0.17	—	–0.17	—	ns
		MachXO2-2000HC-HE	–0.20	—	–0.20	—	–0.20	—	ns
		MachXO2-4000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-7000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	MachXO2-256HC-HE	1.75	—	1.95	—	2.16	—	ns
		MachXO2-640HC-HE	1.75	—	1.95	—	2.16	—	ns
		MachXO2-1200HC-HE	1.88	—	2.12	—	2.36	—	ns
		MachXO2-2000HC-HE	1.89	—	2.13	—	2.37	—	ns
		MachXO2-4000HC-HE	1.94	—	2.18	—	2.43	—	ns
		MachXO2-7000HC-HE	1.98	—	2.23	—	2.49	—	ns

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-256HC-HE	1.42	—	1.59	—	1.96	—	ns
		MachXO2-640HC-HE	1.41	—	1.58	—	1.96	—	ns
		MachXO2-1200HC-HE	1.63	—	1.79	—	2.17	—	ns
		MachXO2-2000HC-HE	1.61	—	1.76	—	2.13	—	ns
		MachXO2-4000HC-HE	1.66	—	1.81	—	2.19	—	ns
		MachXO2-7000HC-HE	1.53	—	1.67	—	2.03	—	ns
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-256HC-HE	–0.24	—	–0.24	—	–0.24	—	ns
		MachXO2-640HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-1200HC-HE	–0.24	—	–0.24	—	–0.24	—	ns
		MachXO2-2000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000HC-HE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-7000HC-HE	–0.21	—	–0.21	—	–0.21	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices	—	388	—	323	—	269	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
t_{COE}	Clock to Output – PIO Output Register	MachXO2-1200HC-HE	—	7.53	—	7.76	—	8.10	ns
		MachXO2-2000HC-HE	—	7.53	—	7.76	—	8.10	ns
		MachXO2-4000HC-HE	—	7.45	—	7.68	—	8.00	ns
		MachXO2-7000HC-HE	—	7.53	—	7.76	—	8.10	ns
t_{SUE}	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
		MachXO2-2000HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
		MachXO2-4000HC-HE	–0.16	—	–0.16	—	–0.16	—	ns
		MachXO2-7000HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
t_{HE}	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	1.97	—	2.24	—	2.52	—	ns
		MachXO2-2000HC-HE	1.97	—	2.24	—	2.52	—	ns
		MachXO2-4000HC-HE	1.89	—	2.16	—	2.43	—	ns
		MachXO2-7000HC-HE	1.97	—	2.24	—	2.52	—	ns
t_{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	1.56	—	1.69	—	2.05	—	ns
		MachXO2-2000HC-HE	1.56	—	1.69	—	2.05	—	ns
		MachXO2-4000HC-HE	1.74	—	1.88	—	2.25	—	ns
		MachXO2-7000HC-HE	1.66	—	1.81	—	2.17	—	ns
t_{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-2000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000HC-HE	–0.34	—	–0.34	—	–0.34	—	ns
		MachXO2-7000HC-HE	–0.29	—	–0.29	—	–0.29	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t_{COPLL}	Clock to Output – PIO Output Register	MachXO2-1200HC-HE	—	5.97	—	6.00	—	6.13	ns
		MachXO2-2000HC-HE	—	5.98	—	6.01	—	6.14	ns
		MachXO2-4000HC-HE	—	5.99	—	6.02	—	6.16	ns
		MachXO2-7000HC-HE	—	6.02	—	6.06	—	6.20	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	0.36	—	0.36	—	0.65	—	ns
		MachXO2-2000HC-HE	0.36	—	0.36	—	0.63	—	ns
		MachXO2-4000HC-HE	0.35	—	0.35	—	0.62	—	ns
		MachXO2-7000HC-HE	0.34	—	0.34	—	0.59	—	ns

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HPLL}	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	0.41	—	0.48	—	0.55	—	ns
		MachXO2-2000HC-HE	0.42	—	0.49	—	0.56	—	ns
		MachXO2-4000HC-HE	0.43	—	0.50	—	0.58	—	ns
		MachXO2-7000HC-HE	0.46	—	0.54	—	0.62	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	2.88	—	3.19	—	3.72	—	ns
		MachXO2-2000HC-HE	2.87	—	3.18	—	3.70	—	ns
		MachXO2-4000HC-HE	2.96	—	3.28	—	3.81	—	ns
		MachXO2-7000HC-HE	3.05	—	3.35	—	3.87	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-2000HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-4000HC-HE	–0.87	—	–0.87	—	–0.87	—	ns
		MachXO2-7000HC-HE	–0.91	—	–0.91	—	–0.91	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.317	—	0.344	—	0.368	UI
t_{DVE}	Input Data Hold After CLK		0.742	—	0.702	—	0.668	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	All MachXO2 devices, all sides	0.566	—	0.560	—	0.538	—	ns
t_{HO}	Input Data Hold After CLK		0.778	—	0.879	—	1.090	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.316	—	0.342	—	0.364	UI
t_{DVE}	Input Data Hold After CLK		0.710	—	0.675	—	0.679	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.233	—	0.219	—	0.198	—	ns
t_{HO}	Input Data Hold After CLK		0.287	—	0.287	—	0.344	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only.[11]	—	0.290	—	0.320	—	0.345	UI
t_{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	0.703	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only.[11]	0.233	—	0.219	—	0.198	—	ns
t_{HO}	Input Data Hold After ECLK		0.287	—	0.287	—	0.344	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1)[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only.[11]	—	0.290	—	0.320	—	0.345	UI
t_{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	0.703	—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	All MachXO2 devices, all sides.	—	0.520	—	0.550	—	0.580	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.520	—	0.550	—	0.580	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK frequency		—	150	—	125	—	104	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	All MachXO2 devices, all sides.	1.210	—	1.510	—	1.870	—	ns
t_{DVA}	Output Data Valid After CLK Output		1.210	—	1.510	—	1.870	—	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		—	150	—	125	—	104	MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.535	—	0.670	—	0.830	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	0.830	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.455	—	0.570	—	0.710	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.455	—	0.570	—	0.710	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[9, 12]									
t_{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.160	—	0.180	—	0.200	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.160	—	0.180	—	0.200	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.369	—	0.395	—	0.421	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.529	—	0.530	—	0.527	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM LPDDR Serial Data Speed		—	280	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	140	—	125	—	104	MHz
f_{LPDDR}	LPDDR Data Transfer Rate		0	280	0	250	0	208	Mbps
DDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.350	—	0.387	—	0.414	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.545	—	0.538	—	0.532	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	150	—	125	—	104	MHz
f_{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps
DDR2[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.360	—	0.378	—	0.406	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.555	—	0.549	—	0.542	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	150	—	125	—	104	MHz
f_{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
7. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps (–6), 113 ps (–5), 120 ps (–4).
8. This number for general purpose usage. Duty cycle tolerance is +/– 10%.
9. Duty cycle is +/–5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32 QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

MachXO2 External Switching Characteristics – ZE Devices[1, 2, 3, 4, 5, 6, 7]

Over Recommended Operating Conditions

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f_{MAX_PRI}[8]	Frequency for Primary Clock Tree	All MachXO2 devices	—	150	—	125	—	104	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	1.00	—	1.20	—	1.40	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO2-256ZE	—	1250	—	1272	—	1296	ps
		MachXO2-640ZE	—	1161	—	1183	—	1206	ps
		MachXO2-1200ZE	—	1213	—	1267	—	1322	ps
		MachXO2-2000ZE	—	1204	—	1250	—	1296	ps
		MachXO2-4000ZE	—	1195	—	1233	—	1269	ps
		MachXO2-7000ZE	—	1243	—	1268	—	1296	ps
Edge Clock									
f_{MAX_EDGE}[8]	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	210	—	175	—	146	MHz
Pin-LUT-Pin Propagation Delay									
t_{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	—	9.35	—	9.78	—	10.21	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t_{CO}	Clock to Output – PIO Output Register	MachXO2-256ZE	—	10.46	—	10.86	—	11.25	ns
		MachXO2-640ZE	—	10.52	—	10.92	—	11.32	ns
		MachXO2-1200ZE	—	11.24	—	11.68	—	12.12	ns
		MachXO2-2000ZE	—	11.27	—	11.71	—	12.16	ns
		MachXO2-4000ZE	—	11.28	—	11.78	—	12.28	ns
		MachXO2-7000ZE	—	11.22	—	11.76	—	12.30	ns
t_{SU}	Clock to Data Setup – PIO Input Register	MachXO2-256ZE	–0.21	—	–0.21	—	–0.21	—	ns
		MachXO2-640ZE	–0.22	—	–0.22	—	–0.22	—	ns
		MachXO2-1200ZE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-2000ZE	–0.27	—	–0.27	—	–0.27	—	ns
		MachXO2-4000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-7000ZE	–0.33	—	–0.33	—	–0.33	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	MachXO2-256ZE	3.96	—	4.25	—	4.65	—	ns
		MachXO2-640ZE	4.01	—	4.31	—	4.71	—	ns
		MachXO2-1200ZE	3.95	—	4.29	—	4.73	—	ns
		MachXO2-2000ZE	3.94	—	4.29	—	4.74	—	ns
		MachXO2-4000ZE	3.96	—	4.36	—	4.87	—	ns
		MachXO2-7000ZE	3.93	—	4.37	—	4.91	—	ns

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-256ZE	2.62	—	2.91	—	3.14	—	ns
		MachXO2-640ZE	2.56	—	2.85	—	3.08	—	ns
		MachXO2-1200ZE	2.30	—	2.57	—	2.79	—	ns
		MachXO2-2000ZE	2.25	—	2.50	—	2.70	—	ns
		MachXO2-4000ZE	2.39	—	2.60	—	2.76	—	ns
		MachXO2-7000ZE	2.17	—	2.33	—	2.43	—	ns
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-256ZE	–0.44	—	–0.44	—	–0.44	—	ns
		MachXO2-640ZE	–0.43	—	–0.43	—	–0.43	—	ns
		MachXO2-1200ZE	–0.28	—	–0.28	—	–0.28	—	ns
		MachXO2-2000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-4000ZE	–0.34	—	–0.34	—	–0.34	—	ns
		MachXO2-7000ZE	–0.21	—	–0.21	—	–0.21	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices	—	150	—	125	—	104	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
t_{COE}	Clock to Output – PIO Output Register	MachXO2-1200ZE	—	11.10	—	11.51	—	11.91	ns
		MachXO2-2000ZE	—	11.10	—	11.51	—	11.91	ns
		MachXO2-4000ZE	—	10.89	—	11.28	—	11.67	ns
		MachXO2-7000ZE	—	11.10	—	11.51	—	11.91	ns
t_{SUE}	Clock to Data Setup – PIO Input Register	MachXO2-1200ZE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-2000ZE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000ZE	–0.15	—	–0.15	—	–0.15	—	ns
		MachXO2-7000ZE	–0.23	—	–0.23	—	–0.23	—	ns
t_{HE}	Clock to Data Hold – PIO Input Register	MachXO2-1200ZE	3.81	—	4.11	—	4.52	—	ns
		MachXO2-2000ZE	3.81	—	4.11	—	4.52	—	ns
		MachXO2-4000ZE	3.60	—	3.89	—	4.28	—	ns
		MachXO2-7000ZE	3.81	—	4.11	—	4.52	—	ns
t_{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200ZE	2.78	—	3.11	—	3.40	—	ns
		MachXO2-2000ZE	2.78	—	3.11	—	3.40	—	ns
		MachXO2-4000ZE	3.11	—	3.48	—	3.79	—	ns
		MachXO2-7000ZE	2.94	—	3.30	—	3.60	—	ns
t_{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200ZE	–0.29	—	-0.29	—	–0.29	—	ns
		MachXO2-2000ZE	–0.29	—	-0.29	—	–0.29	—	ns
		MachXO2-4000ZE	–0.46	—	-0.46	—	–0.46	—	ns
		MachXO2-7000ZE	–0.37	—	-0.37	—	–0.37	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t_{COPLL}	Clock to Output – PIO Output Register	MachXO2-1200ZE	—	7.95	—	8.07	—	8.19	ns
		MachXO2-2000ZE	—	7.97	—	8.10	—	8.22	ns
		MachXO2-4000ZE	—	7.98	—	8.10	—	8.23	ns
		MachXO2-7000ZE	—	8.02	—	8.14	—	8.26	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO2-1200ZE	0.85	—	0.85	—	0.89	—	ns
		MachXO2-2000ZE	0.84	—	0.84	—	0.86	—	ns
		MachXO2-4000ZE	0.84	—	0.84	—	0.85	—	ns
		MachXO2-7000ZE	0.83	—	0.83	—	0.81	—	ns

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HPLL}	Clock to Data Hold – PIO Input Register	MachXO2-1200ZE	0.66	—	0.68	—	0.80	—	ns
		MachXO2-2000ZE	0.68	—	0.70	—	0.83	—	ns
		MachXO2-4000ZE	0.68	—	0.71	—	0.84	—	ns
		MachXO2-7000ZE	0.73	—	0.74	—	0.87	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200ZE	5.14	—	5.69	—	6.20	—	ns
		MachXO2-2000ZE	5.11	—	5.67	—	6.17	—	ns
		MachXO2-4000ZE	5.27	—	5.84	—	6.35	—	ns
		MachXO2-7000ZE	5.15	—	5.71	—	6.23	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200ZE	–1.36	—	–1.36	—	–1.36	—	ns
		MachXO2-2000ZE	–1.35	—	–1.35	—	–1.35	—	ns
		MachXO2-4000ZE	–1.43	—	–1.43	—	–1.43	—	ns
		MachXO2-7000ZE	–1.41	—	–1.41	—	–1.41	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.382	—	0.401	—	0.417	UI
t_{DVE}	Input Data Hold After CLK		0.670	—	0.684	—	0.693	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	All MachXO2 devices, all sides	1.319	—	1.412	—	1.462	—	ns
t_{HO}	Input Data Hold After CLK		0.717	—	1.010	—	1.340	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.361	—	0.346	—	0.334	UI
t_{DVE}	Input Data Hold After CLK		0.602	—	0.625	—	0.648	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.472	—	0.672	—	0.865	—	ns
t_{HO}	Input Data Hold After CLK		0.363	—	0.501	—	0.743	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input - GDDRX4_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.307	—	0.316	—	0.326	UI
t_{DVE}	Input Data Hold After ECLK		0.662	—	0.650	—	0.649	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.434	—	0.535	—	0.630	—	ns
t_{HO}	Input Data Hold After ECLK		0.385	—	0.395	—	0.463	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz
7:1 LVDS Inputs – GDDR71_RX.ECLK.7.1[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.307	—	0.316	—	0.326	UI
t_{DVE}	Input Data Hold After ECLK		0.662	—	0.650	—	0.649	—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	210	—	176	—	146	MHz
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	60	—	50	—	42	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	All MachXO2 devices, all sides	—	0.850	—	0.910	—	0.970	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.850	—	0.910	—	0.970	ns
f_{DATA}	DDRX1 Output Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK frequency		—	70	—	58	—	49	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	All MachXO2 devices, all sides	2.720	—	3.380	—	4.140	—	ns
t_{DVA}	Output Data Valid After CLK Output		2.720	—	3.380	—	4.140	—	ns
f_{DATA}	DDRX1 Output Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		—	70	—	58	—	49	MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	—	0.270	—	0.300	—	0.330	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.270	—	0.300	—	0.330	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	1.445	—	1.760	—	2.140	—	ns
t_{DVA}	Output Data Valid After CLK Output		1.445	—	1.760	—	2.140	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	—	0.270	—	0.300	—	0.330	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.270	—	0.300	—	0.330	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	0.873	—	1.067	—	1.319	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.873	—	1.067	—	1.319	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[9, 12]									
t_{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.240	—	0.270	—	0.300	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.240	—	0.270	—	0.300	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	420	—	352	—	292	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	210	—	176	—	146	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	60	—	50	—	42	MHz

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.349	—	0.381	—	0.396	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.630	—	0.613	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM LPDDR Serial Data Speed		—	120	—	110	—	96	Mbps
f_{SCLK}	SCLK Frequency		—	60	—	55	—	48	MHz
f_{LPDDR}	LPDDR Data Transfer Rate		0	120	0	110	0	96	Mbps
DDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.347	—	0.374	—	0.393	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.637	—	0.616	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f_{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f_{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps
DDR2[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.372	—	0.394	—	0.410	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.690	—	0.658	—	0.618	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f_{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f_{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
7. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 167 ps (–3), 182 ps (–2), 195 ps (–1).
8. This number for general purpose usage. Duty cycle tolerance is +/–10%.
9. Duty cycle is +/– 5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

Figure 3-5. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms

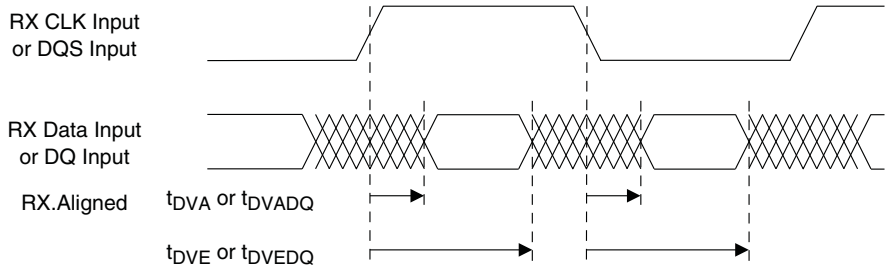


Figure 3-6. Receiver RX.CLK.Centered Waveforms

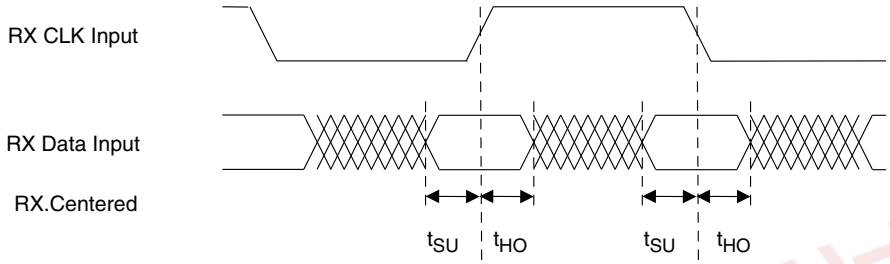


Figure 3-7. Transmitter TX.CLK.Aligned Waveforms

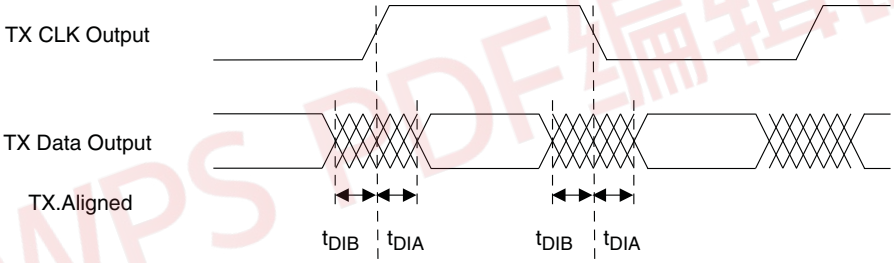


Figure 3-8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms

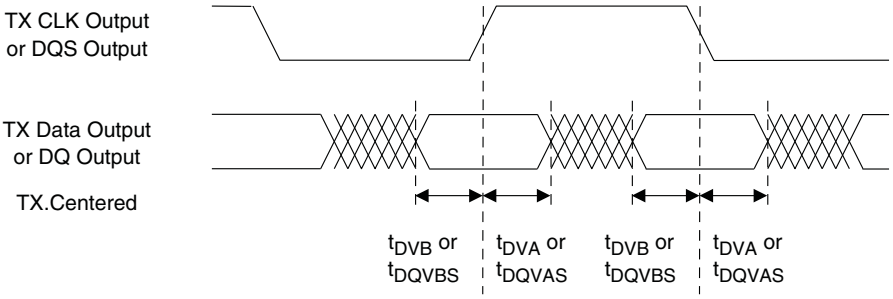


Figure 3-9. GDDR71 Video Timing Waveforms

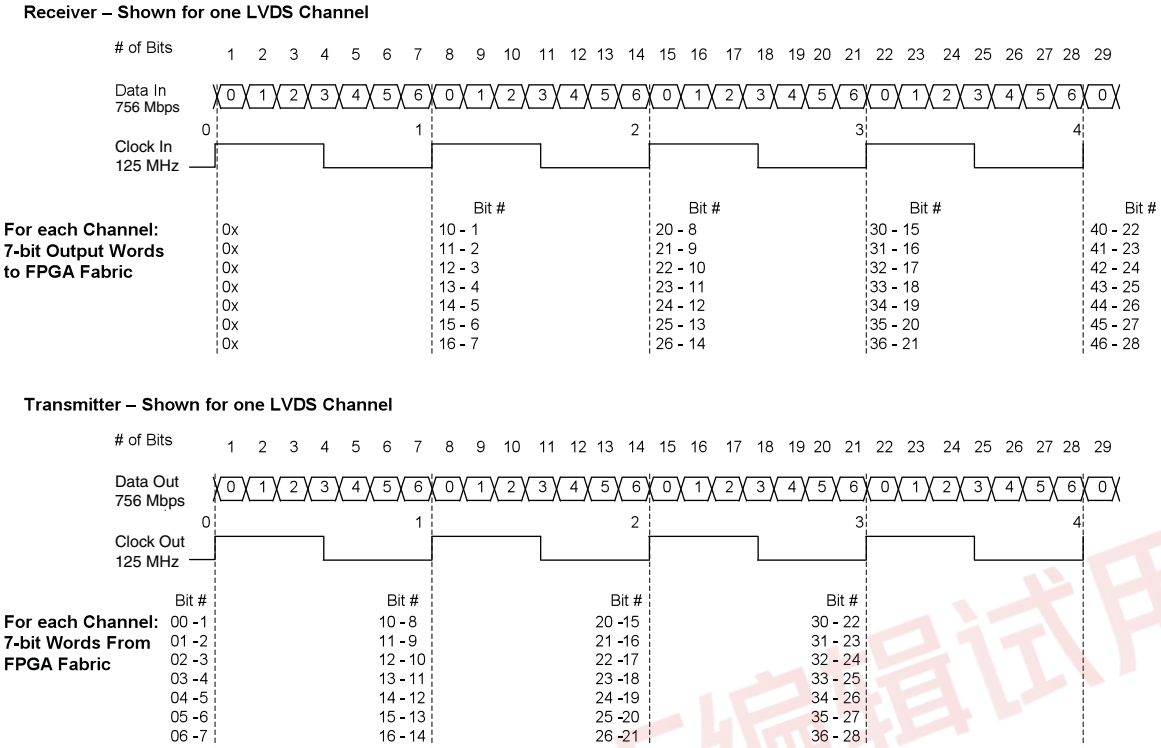


Figure 3-10. Receiver GDDR71_RX. Waveforms

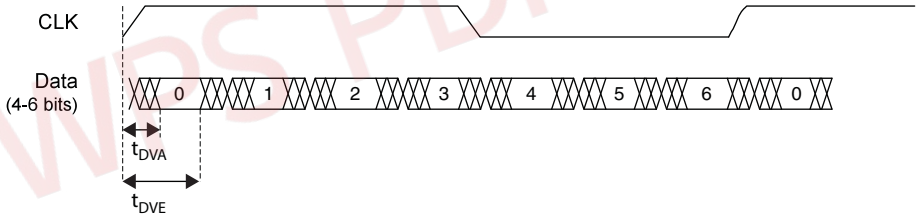
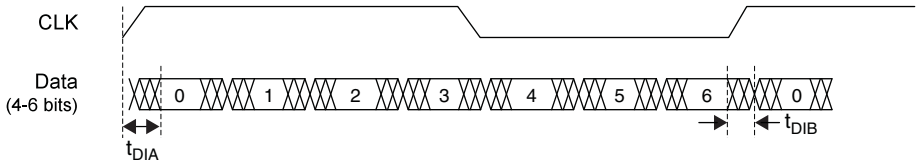


Figure 3-11. Transmitter GDDR71_TX. Waveforms



sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)		1.5625	400	MHz
f_{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f_{VCO}	PLL VCO Frequency		200	800	MHz
f_{PFD}	Phase Detector Input Frequency		7	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Without duty trim selected[3]	45	55	%
t_{DT_TRIM}[7]	Edge Duty Trim Accuracy		–75	75	%
t_{PH}[4]	Output Phase Accuracy		–6	6	%
t_{OPJIT}[1, 8]	Output Clock Period Jitter	f_{OUT} > 100 MHz	—	150	ps p-p
		f_{OUT} < 100 MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} > 100 MHz	—	180	ps p-p
		f_{OUT} < 100 MHz	—	0.009	UIPP
	Output Clock Phase Jitter	f_{PFD} > 100 MHz	—	160	ps p-p
		f_{PFD} < 100 MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	230	ps p-p
		f_{OUT} < 100 MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	230	ps p-p
		f_{OUT} < 100 MHz	—	0.12	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	–120	120	ps
t_W	Output Clock Pulse Width	At 90% or 10%[3]	0.9	—	ns
t_{LOCK}[2, 5]	PLL Lock-in Time		—	15	ms
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[6]	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{STABLE}[5]	STANDBY High to PLL Stable		—	15	ms
t_{RST}	RST/RESETM Pulse Width		1	—	ns
t_{RSTREC}	RST Recovery Time		1	—	ns
t_{RST_DIV}	RESETC/D Pulse Width		10	—	ns
t_{RSTREC_DIV}	RESETC/D Recovery Time		1	—	ns
$t_{ROTATE-SETUP}$	PHASESTEP Setup Time		10	—	ns

sysCLOCK PLL Timing (Continued)

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
t_{ROTATE_WD}	PHASESTEP Pulse Width		4	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide for more details.
5. At minimum $f_{PFD.}$ As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

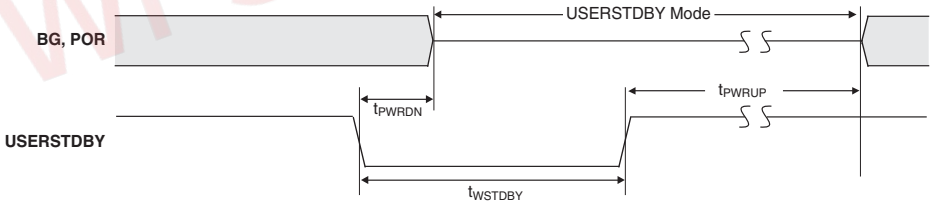
MachXO2 Oscillator Output Frequency

Symbol	Parameter	Min.	Typ.	Max	Units
f_{MAX}	Oscillator Output Frequency (Commercial Grade Devices, 0 to 85°C)	125.685	133	140.315	MHz
	Oscillator Output Frequency (Industrial Grade Devices, –40 °C to 100 °C)	124.355	133	141.645	MHz
t_{DT}	Output Clock Duty Cycle	43	50	57	%
t_{OPJIT}[1]	Output Clock Period Jitter	0.01	0.012	0.02	UIPP
$t_{STABLEOSC}$	STDBY Low to Oscillator Stable	0.01	0.05	0.1	µs

1. Output Clock Period Jitter specified at 133 MHz. The values for lower frequencies will be smaller UIPP. The typical value for 133 MHz is 95 ps and for 2.08 MHz the typical value is 1.54 ns.

MachXO2 Standby Mode Timing – HC/HE Devices

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	USERSTDBY High to Stop	All	—	—	9	ns
t_{PWRUP}	USERSTDBY Low to Power Up	LCMXO2-256		—		µs
		LCMXO2-640		—		µs
		LCMXO2-640U		—		µs
		LCMXO2-1200	20	—	50	µs
		LCMXO2-1200U		—		µs
		LCMXO2-2000		—		µs
		LCMXO2-2000U		—		µs
		LCMXO2-4000		—		µs
		LCMXO2-7000		—		µs
t_{WSTDBY}	USERSTDBY Pulse Width	All	18	—	—	ns



MachXO2 Standby Mode Timing – ZE Devices

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	USERSTDBY High to Stop	All	—	—	13	ns
t_{PWRUP}	USERSTDBY Low to Power Up	LCMXO2-256		—		µs
		LCMXO2-640		—		µs
		LCMXO2-1200	20	—	50	µs
		LCMXO2-2000		—		µs
		LCMXO2-4000		—		µs
		LCMXO2-7000		—		µs
t_{WSTDBY}	USERSTDBY Pulse Width	All	19	—	—	ns
$t_{BNDGAPSTBL}$	USERSTDBY High to Bandgap Stable	All	—	—	15	ns

Flash Download Time[1, 2]

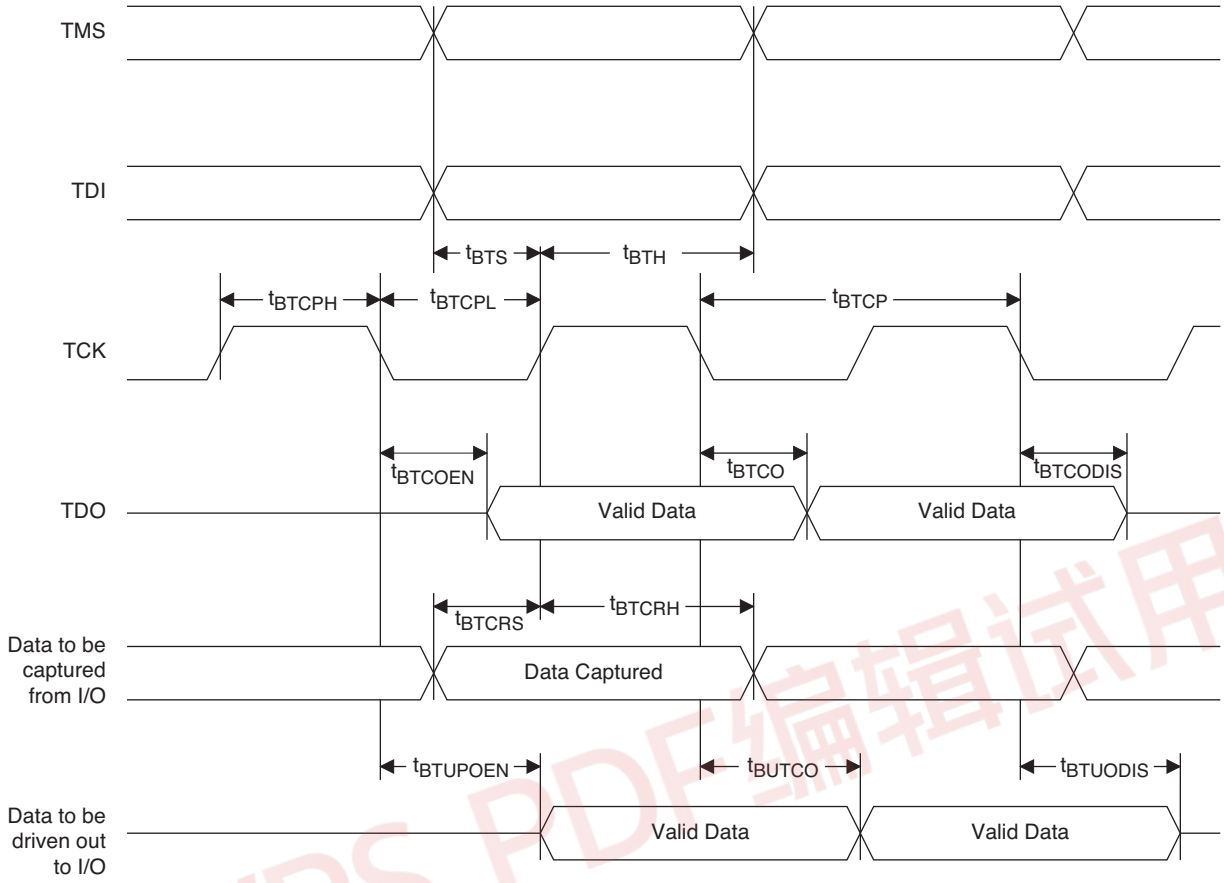
Symbol	Parameter	Device	Typ.	Units
$t_{REFRESH}$	POR to Device I/O Active	LCMXO2-256	0.6	ms
		LCMXO2-640	1.0	ms
		LCMXO2-640U	1.9	ms
		LCMXO2-1200	1.9	ms
		LCMXO2-1200U	1.4	ms
		LCMXO2-2000	1.4	ms
		LCMXO2-2000U	2.4	ms
		LCMXO2-4000	2.4	ms
		LCMXO2-7000	3.8	ms

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.
2. The Flash download time is measured starting from the maximum voltage of POR trip point.

JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	20	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-12. JTAG Port Timing Waveforms



sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Modes					
t_{PRGM}	PROGRAMN low pulse accept		55	—	ns
t_{PRGMJ}	PROGRAMN low pulse rejection		—	25	ns
t_{INITL}	INITN low time	LCMXO2-256	—	30	µs
		LCMXO2-640	—	35	µs
		LCMXO2-640U/ LCMXO2-1200	—	55	µs
		LCMXO2-1200U/ LCMXO2-2000	—	70	µs
		LCMXO2-2000U/ LCMXO2-4000	—	105	µs
		LCMXO2-7000	—	130	µs
$t_{DPPINIT}$	PROGRAMN low to INITN low		—	150	ns
$t_{DPPDONE}$	PROGRAMN low to DONE low		—	150	ns
t_{IODISS}	PROGRAMN low to I/O disable		—	120	ns
Slave SPI					
f_{MAX}	CCLK clock frequency		—	66	MHz
t_{CCLKH}	CCLK clock pulse width high		7.5	—	ns
t_{CCLKL}	CCLK clock pulse width low		7.5	—	ns
t_{STSU}	CCLK setup time		2	—	ns
t_{STH}	CCLK hold time		0	—	ns
t_{STCO}	CCLK falling edge to valid output		—	10	ns
t_{STOZ}	CCLK falling edge to valid disable		—	10	ns
t_{STOV}	CCLK falling edge to valid enable		—	10	ns
t_{SCS}	Chip select high time		25	—	ns
t_{SCSS}	Chip select setup time		3	—	ns
t_{SCSH}	Chip select hold time		3	—	ns
Master SPI					
f_{MAX}	MCLK clock frequency		—	133	MHz
t_{MCLKH}	MCLK clock pulse width high		3.75	—	ns
t_{MCLKL}	MCLK clock pulse width low		3.75	—	ns
t_{STSU}	MCLK setup time		5	—	ns
t_{STH}	MCLK hold time		1	—	ns
t_{CSSPI}	INITN high to chip select low		100	200	ns
t_{MCLK}	INITN high to first MCLK edge		0.75	1	µs

I²C Port Timing Specifications[1, 2]

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCL clock frequency	—	400	kHz

1. MachXO2 supports the following modes:
   • Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
   • Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
2. Refer to the I²C specification for timing requirements.

SPI Port Timing Specifications[1]

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCK clock frequency	—	45	MHz

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

Switching Test Conditions

Figure 3-13 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-5.

Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards

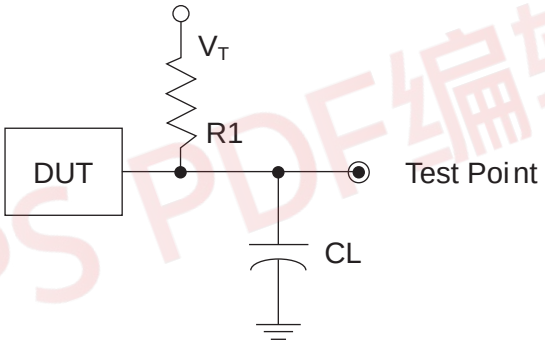


Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R1	CL	Timing Ref.	VT
LVTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5 V	V_{OL}
LVTTL and LVCMOS 3.3 (Z -> L)			1.5 V	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVTTL + LVCMOS (H -> Z)			V_{OH} – 0.15 V	V_{OL}
LVTTL + LVCMOS (L -> Z)			V_{OL} – 0.15 V	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the group to which the pad is connected. Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic. During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.
NC	—	No connect.
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together. For QFN 48 package, the exposed die pad is the device ground.
VCC	—	V_{CC} – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIOx	—	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.
PLL and Clock Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)		
[LOC]_GPLL[T, C]_IN	—	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.
Test and Programming (Dual function pins used for test access port and during sysCONFIG™)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
JTAGENB	I	Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then: If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O. If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.
Configuration (Dual function pins used during sysCONFIG)		
PROGRAMN	I	Initiates configuration sequence when asserted low. During configuration, or when reserved as PROGRAMN in user mode, this pin always has an active pull-up.

Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, or when reserved as INITn in user mode, this pin has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress. During configuration, or when reserved as DONE in user mode, this pin has an active pull-up.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.
SCL	I/O	Slave I^2C clock input and master I^2C clock output.
SDA	I/O	Slave I^2C data input and master I^2C data output.

Pinout Information Summary

	MachXO2-256					MachXO2-640			MachXO2-640U
	32 QFN[1]	48 QFN[3]	64 ucBGA	100 TQFP	132 csBGA	48 QFN[3]	100 TQFP	132 csBGA	144 TQFP
General Purpose I/O per Bank									
Bank 0	8	10	9	13	13	10	18	19	27
Bank 1	2	10	12	14	14	10	20	20	26
Bank 2	9	10	11	14	14	10	20	20	28
Bank 3	2	10	12	14	14	10	20	20	26
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Single Ended I/O	21	40	44	55	55	40	78	79	107
Differential I/O per Bank									
Bank 0	4	5	5	7	7	5	9	10	14
Bank 1	1	5	6	7	7	5	10	10	13
Bank 2	4	5	5	7	7	5	10	10	14
Bank 3	1	5	6	7	7	5	10	10	13
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Differential I/O	10	20	22	28	28	20	39	40	54
Dual Function I/O	22	25	27	29	29	25	29	29	33
High-speed Differential I/O									
Bank 0	0	0	0	0	0	0	0	0	7
Gearboxes									
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	0	0	0	0	0	0	0	0	7
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	0	0	0	0	0	0	0	0	7
DQS Groups									
Bank 1	0	0	0	0	0	0	0	0	2
VCCIO Pins									
Bank 0	2	2	2	2	2	2	2	2	3
Bank 1	1	1	2	2	2	1	2	2	3
Bank 2	2	2	2	2	2	2	2	2	3
Bank 3	1	1	2	2	2	1	2	2	3
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
VCC	2	2	2	2	2	2	2	2	4
GND[2]	2	1	8	8	8	1	8	10	12
NC	0	0	1	26	58	0	3	32	8
Reserved for Configuration	1	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	32	49	64	100	132	49	100	132	144

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.
2. For 48 QFN package, exposed die pad is the device ground.
3. 48-pin QFN information is 'Advanced'.

	MachXO2-1200					MachXO2-1200U
	100 TQFP	132 csBGA	144 TQFP	25 WLCSP	32 QFN[1]	256 ftBGA
General Purpose I/O per Bank						
Bank 0	18	25	27	11	9	50
Bank 1	21	26	26	0	2	52
Bank 2	20	28	28	7	9	52
Bank 3	20	25	26	0	2	16
Bank 4	0	0	0	0	0	16
Bank 5	0	0	0	0	0	20
Total General Purpose Single Ended I/O	79	104	107	18	22	206
Differential I/O per Bank						
Bank 0	9	13	14	5	4	25
Bank 1	10	13	13	0	1	26
Bank 2	10	14	14	2	4	26
Bank 3	10	12	13	0	1	8
Bank 4	0	0	0	0	0	8
Bank 5	0	0	0	0	0	10
Total General Purpose Differential I/O	39	52	54	7	10	103
Dual Function I/O	31	33	33	18	22	33
High-speed Differential I/O						
Bank 0	4	7	7	0	0	14
Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	4	7	7	0	0	14
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	5	7	7	0	2	14
DQS Groups						
Bank 1	1	2	2	0	0	2
VCCIO Pins						
Bank 0	2	3	3	1	2	4
Bank 1	2	3	3	0	1	4
Bank 2	2	3	3	1	2	4
Bank 3	3	3	3	0	1	1
Bank 4	0	0	0	0	0	2
Bank 5	0	0	0	0	0	1
VCC	2	4	4	2	2	8
GND	8	10	12	2	2	24
NC	1	1	8	0	0	1
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	100	132	144	25	32	256

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.

	MachXO2-2000						MachXO2-2000U
	49 WLCSP	100 TQFP	132 csBGA	144 TQFP	256 caBGA	256 ftBGA	484 ftBGA
General Purpose I/O per Bank							
Bank 0	19	18	25	27	50	50	70
Bank 1	0	21	26	28	52	52	68
Bank 2	13	20	28	28	52	52	72
Bank 3	0	6	7	8	16	16	24
Bank 4	0	6	8	10	16	16	16
Bank 5	6	8	10	10	20	20	28
Total General Purpose Single-Ended I/O	38	79	104	111	206	206	278
Differential I/O per Bank							
Bank 0	7	9	13	14	25	25	35
Bank 1	0	10	13	14	26	26	34
Bank 2	6	10	14	14	26	26	36
Bank 3	0	3	3	4	8	8	12
Bank 4	0	3	4	5	8	8	8
Bank 5	3	4	5	5	10	10	14
Total General Purpose Differential I/O	16	39	52	56	103	103	139
Dual Function I/O	24	31	33	33	33	33	37
High-speed Differential I/O							
Bank 0	5	4	8	9	14	14	18
Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	4	8	9	14	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	10	14	14	14	14	18
DQS Groups							
Bank 1	0	1	2	2	2	2	2
VCCIO Pins							
Bank 0	2	2	3	3	4	4	10
Bank 1	0	2	3	3	4	4	10
Bank 2	1	2	3	3	4	4	10
Bank 3	0	1	1	1	1	1	3
Bank 4	0	1	1	1	2	2	4
Bank 5	1	1	1	1	1	1	3
VCC	2	2	4	4	8	8	12
GND	4	8	10	12	24	24	48
NC	0	1	1	4	1	1	105
Reserved for Configuration	1	1	1	1	v	1	1
Total Count of Bonded Pins	39	100	132	144	256	256	484

	MachXO2-4000							
	84 QFN	132 csBGA	144 TQFP	184 csBGA	256 caBGA	256 ftBGA	332 caBGA	484 fpBGA
General Purpose I/O per Bank								
Bank 0	27	25	27	37	50	50	68	70
Bank 1	10	26	29	37	52	52	68	68
Bank 2	22	28	29	39	52	52	70	72
Bank 3	0	7	9	10	16	16	24	24
Bank 4	9	8	10	12	16	16	16	16
Bank 5	0	10	10	15	20	20	28	28
Total General Purpose Single Ended I/O	68	104	114	150	206	206	274	278
Differential I/O per Bank								
Bank 0	13	13	14	18	25	25	34	35
Bank 1	4	13	14	18	26	26	34	34
Bank 2	11	14	14	19	26	26	35	36
Bank 3	0	3	4	4	8	8	12	12
Bank 4	4	4	5	6	8	8	8	8
Bank 5	0	5	5	7	10	10	14	14
Total General Purpose Differential I/O	32	52	56	72	103	103	137	139
Dual Function I/O	28	37	37	37	37	37	37	37
High-speed Differential I/O								
Bank 0	8	8	9	8	18	18	18	18
Gearboxes								
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	8	8	9	9	18	18	18	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	11	14	14	12	18	18	18	18
DQS Groups								
Bank 1	1	2	2	2	2	2	2	2
VCCIO Pins								
Bank 0	3	3	3	3	4	4	4	10
Bank 1	1	3	3	3	4	4	4	10
Bank 2	2	3	3	3	4	4	4	10
Bank 3	1	1	1	1	1	1	2	3
Bank 4	1	1	1	1	2	2	1	4
Bank 5	1	1	1	1	1	1	2	3
VCC	4	4	4	4	8	8	8	12
GND	4	10	12	16	24	24	27	48
NC	1	1	1	1	1	1	5	105
Reserved for configuration	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	84	132	144	184	256	256	332	484

	MachXO2-7000					
	144 TQFP	**256 caBGA**	**256 ftBGA**	**332 caBGA**	**400 caBGA**	**484 fpBGA**
General Purpose I/O per Bank						
Bank 0	27	50	50	68	83	82
Bank 1	29	52	52	70	84	84
Bank 2	29	52	52	70	84	84
Bank 3	9	16	16	24	28	28
Bank 4	10	16	16	16	24	24
Bank 5	10	20	20	30	32	32
Total General Purpose Single Ended I/O	114	206	206	278	335	334
Differential I/O per Bank						
Bank 0	14	25	25	34	42	41
Bank 1	14	26	26	35	42	42
Bank 2	14	26	26	35	42	42
Bank 3	4	8	8	12	14	14
Bank 4	5	8	8	8	12	12
Bank 5	5	10	10	15	16	16
Total General Purpose Differential I/O	56	103	103	139	168	167
Dual Function I/O	37	37	37	37	37	37
High-speed Differential I/O						
Bank 0	9	20	20	21	21	21
Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	9	20	20	21	21	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	14	20	20	21	21	21
DQS Groups						
Bank 1	2	2	2	2	2	2
VCCIO Pins						
Bank 0	3	4	4	4	5	10
Bank 1	3	4	4	4	5	10
Bank 2	3	4	4	4	5	10
Bank 3	1	1	1	2	2	3
Bank 4	1	2	2	1	2	4
Bank 5	1	1	1	2	2	3
VCC	4	8	8	8	10	12
GND	12	24	24	27	33	48
NC	1	1	1	1	0	49
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	144	256	256	332	400	484

For Further Information

For further information regarding logic signal connections for various packages please refer to the MachXO2 Device Pinout Files.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Users must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1198, Power Estimation and Management for MachXO2 Devices
- The Power Calculator tool is included with the Lattice design tools, or as a standalone download from www.latticesemi.com/software

MachXO2 Family Data Sheet Ordering Information

March 2017 Data Sheet DS1035

MachXO2 Part Number Description

LCMXO2 – XXXX X X X – X XXXXXX X XX XX

Device Family
MachXO2 PLD

Logic Capacity
256 = 256 LUTs
640 = 640 LUTs
1200 = 1280 LUTs
2000 = 2112 LUTs
4000 = 4320 LUTs
7000 = 6864 LUTs

I/O Count
Blank = Standard Device
U = Ultra High I/O Device

Power/Performance
Z = Low Power
H = High Performance

Supply Voltage
C = 2.5 V / 3.3 V
E = 1.2 V

Speed
1 = Slowest
2
3 = Fastest
} Low Power

4 = Slowest
5
6 = Fastest
} High Performance

Device Status
Blank = Production Device
ES = Engineering Sample
R1 = Production Release 1 Device
1K = WLCSP Package, 1,000 parts per reel

Shipping Method
Blank = Trays
TR = Tape and Reel

Grade
C = Commercial
I = Industrial

Package
UWG25 = 25-Ball Halogen-Free WLCSP (0.4 mm Pitch)
SG32 = 32-Pin Halogen-Free QFN (0.5 mm Pitch)
SG48 = 48-Pin Halogen-Free QFN (0.5 mm Pitch)
UWG49 = 49-ball Halogen-Free WLCSP (0.4 mm Pitch)
UMG64 = 64-Ball Halogen-Free ucBGA (0.4 mm Pitch)
QN84 = 84-Pin Halogen-Free QFN (0.5 mm Pitch)
TG100 = 100-Pin Halogen-Free TQFP
TG144 = 144-Pin Halogen-Free TQFP
MG132 = 132-Ball Halogen-Free csBGA (0.5 mm Pitch)
MG184 = 184-Ball Halogen-Free csBGA (0.5 mm Pitch)
BG256 = 256-Ball Halogen-Free caBGA (0.8 mm Pitch)
FTG256 = 256-Ball Halogen-Free ftBGA (1.0 mm Pitch)
BG332 = 332-Ball Halogen-Free caBGA (0.8 mm Pitch)
FG484 = 484-Ball Halogen-Free fpBGA (1.0 mm Pitch)

* 48-pin QFN information is 'Advanced'.

Ordering Information

MachXO2 devices have top-side markings, for commercial and industrial grades, as shown below:

Notes:

1. Markings are abbreviated for small packages.

2. See PCN 05A-12 for information regarding a change to the top-side mark logo.

Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32C	256	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-256ZE-2SG32C	256	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-256ZE-3SG32C	256	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-256ZE-1UMG64C	256	1.2 V	–1	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-2UMG64C	256	1.2 V	–2	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-3UMG64C	256	1.2 V	–3	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-1TG100C	256	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-2TG100C	256	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-3TG100C	256	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-1MG132C	256	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-2MG132C	256	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-3MG132C	256	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100C	640	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-2TG100C	640	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-3TG100C	640	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-1MG132C	640	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-2MG132C	640	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-3MG132C	640	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1SG32C	1280	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-2SG32C	1280	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-3SG32C	1280	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-1TG100C	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100C	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100C	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132C	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132C	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132C	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144C	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144C	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144C	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1TG100C	2112	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-2TG100C	2112	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-3TG100C	2112	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-1MG132C	2112	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-2MG132C	2112	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-3MG132C	2112	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-1TG144C	2112	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-2TG144C	2112	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-3TG144C	2112	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-1BG256C	2112	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-2BG256C	2112	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-3BG256C	2112	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-1FTG256C	2112	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-2000ZE-2FTG256C	2112	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-2000ZE-3FTG256C	2112	1.2 V	–3	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000ZE-1QN84C	4320	1.2 V	–1	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-2QN84C	4320	1.2 V	–2	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-3QN84C	4320	1.2 V	–3	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-1MG132C	4320	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-2MG132C	4320	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-3MG132C	4320	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-1TG144C	4320	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-2TG144C	4320	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-3TG144C	4320	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-1BG256C	4320	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-2BG256C	4320	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-3BG256C	4320	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-1FTG256C	4320	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-2FTG256C	4320	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-3FTG256C	4320	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-1BG332C	4320	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-2BG332C	4320	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-3BG332C	4320	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-1FG484C	4320	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-4000ZE-2FG484C	4320	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-4000ZE-3FG484C	4320	1.2 V	–3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144C	6864	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-2TG144C	6864	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-3TG144C	6864	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-1BG256C	6864	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-2BG256C	6864	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-3BG256C	6864	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-1FTG256C	6864	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-2FTG256C	6864	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-3FTG256C	6864	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-1BG332C	6864	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-2BG332C	6864	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-3BG332C	6864	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-1FG484C	6864	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-2FG484C	6864	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-3FG484C	6864	1.2 V	–3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100CR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100CR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100CR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132CR1[1]	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132CR1[1]	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132CR1[1]	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144CR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144CR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144CR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200ZE-speed package CR1” are the same as the “LCMXO2-1200ZE-speed package C” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32C	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	COM
LCMXO2-256HC-5SG32C	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	COM
LCMXO2-256HC-6SG32C	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	COM
LCMXO2-256HC-4SG48C	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	COM
LCMXO2-256HC-5SG48C	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	COM
LCMXO2-256HC-6SG48C	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	COM
LCMXO2-256HC-4UMG64C	256	2.5 V / 3.3 V	–4	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-5UMG64C	256	2.5 V / 3.3 V	–5	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-6UMG64C	256	2.5 V / 3.3 V	–6	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-4TG100C	256	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-256HC-5TG100C	256	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-256HC-6TG100C	256	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-256HC-4MG132C	256	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-256HC-5MG132C	256	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-256HC-6MG132C	256	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48C	640	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	COM
LCMXO2-640HC-5SG48C	640	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	COM
LCMXO2-640HC-6SG48C	640	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	COM
LCMXO2-640HC-4TG100C	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-640HC-5TG100C	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-640HC-6TG100C	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-640HC-4MG132C	640	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-640HC-5MG132C	640	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-640HC-6MG132C	640	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144C	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-5TG144C	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-6TG144C	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32C	1280	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	COM
LCMXO2-1200HC-5SG32C	1280	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	COM
LCMXO2-1200HC-6SG32C	1280	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	COM
LCMXO2-1200HC-4TG100C	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100C	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100C	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132C	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132C	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132C	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144C	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144C	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144C	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256C	1280	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-1200UHC-5FTG256C	1280	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-1200UHC-6FTG256C	1280	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100C	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-5TG100C	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-6TG100C	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-4MG132C	2112	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-5MG132C	2112	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-6MG132C	2112	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-4TG144C	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-5TG144C	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-6TG144C	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-4BG256C	2112	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-5BG256C	2112	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-6BG256C	2112	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-4FTG256C	2112	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HC-5FTG256C	2112	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HC-6FTG256C	2112	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484C	2112	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-5FG484C	2112	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-6FG484C	2112	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84C	4320	2.5 V / 3.3 V	–4	Halogen-Free QFN	84	COM
LCMXO2-4000HC-5QN84C	4320	2.5 V / 3.3 V	–5	Halogen-Free QFN	84	COM
LCMXO2-4000HC-6QN84C	4320	2.5 V / 3.3 V	–6	Halogen-Free QFN	84	COM
LCMXO2-4000HC-4MG132C	4320	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-5MG132C	4320	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-6MG132C	4320	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-4TG144C	4320	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-5TG144C	4320	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-6TG144C	4320	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-4BG256C	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-5BG256C	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-6BG256C	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-4FTG256C	4320	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-5FTG256C	4320	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-6FTG256C	4320	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-4BG332C	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-5BG332C	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-6BG332C	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-4FG484C	4320	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-5FG484C	4320	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-6FG484C	4320	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144C	6864	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-5TG144C	6864	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-6TG144C	6864	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-4BG256C	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-5BG256C	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-6BG256C	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-4FTG256C	6864	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-5FTG256C	6864	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-6FTG256C	6864	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-4BG332C	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-5BG332C	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-6BG332C	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-4FG400C	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-5FG400C	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-6FG400C	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-4FG484C	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-5FG484C	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-6FG484C	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100CR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100CR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100CR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132CR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132CR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132CR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144CR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144CR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144CR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200HC-speed package CR1” are the same as the “LCMXO2-1200HC-speed package C” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100C	2112	1.2 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-5TG100C	2112	1.2 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-6TG100C	2112	1.2 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-4TG144C	2112	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-5TG144C	2112	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-6TG144C	2112	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-4MG132C	2112	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-5MG132C	2112	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-6MG132C	2112	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-4BG256C	2112	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-5BG256C	2112	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-6BG256C	2112	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-4FTG256C	2112	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-5FTG256C	2112	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-6FTG256C	2112	1.2 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484C	2112	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-5FG484C	2112	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-6FG484C	2112	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4TG144C	4320	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-5TG144C	4320	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-6TG144C	4320	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-4MG132C	4320	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-5MG132C	4320	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-6MG132C	4320	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-4BG256C	4320	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4MG184C	4320	1.2 V	–4	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5MG184C	4320	1.2 V	–5	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-6MG184C	4320	1.2 V	–6	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5BG256C	4320	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-6BG256C	4320	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4FTG256C	4320	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-5FTG256C	4320	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-6FTG256C	4320	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-4BG332C	4320	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-5BG332C	4320	1.2 V	–5	Halogen-Free caBGA	332	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-6BG332C	4320	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-4FG484C	4320	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-5FG484C	4320	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-6FG484C	4320	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144C	6864	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-5TG144C	6864	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-6TG144C	6864	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-4BG256C	6864	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-5BG256C	6864	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-6BG256C	6864	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-4FTG256C	6864	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-5FTG256C	6864	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-6FTG256C	6864	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-4BG332C	6864	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-5BG332C	6864	1.2 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-6BG332C	6864	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-4FG484C	6864	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-5FG484C	6864	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-6FG484C	6864	1.2 V	–6	Halogen-Free fpBGA	484	COM

Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32I	256	1.2 V	–1	Halogen-Free QFN	32	IND
LCMXO2-256ZE-2SG32I	256	1.2 V	–2	Halogen-Free QFN	32	IND
LCMXO2-256ZE-3SG32I	256	1.2 V	–3	Halogen-Free QFN	32	IND
LCMXO2-256ZE-1UMG64I	256	1.2 V	–1	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-2UMG64I	256	1.2 V	–2	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-3UMG64I	256	1.2 V	–3	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-1TG100I	256	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-2TG100I	256	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-3TG100I	256	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-1MG132I	256	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-2MG132I	256	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-3MG132I	256	1.2 V	–3	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100I	640	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-2TG100I	640	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-3TG100I	640	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-1MG132I	640	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-2MG132I	640	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-3MG132I	640	1.2 V	–3	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1UWG25ITR[1]	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR50[3]	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR1K[2]	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1SG32I	1280	1.2 V	–1	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-2SG32I	1280	1.2 V	–2	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-3SG32I	1280	1.2 V	–3	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-1TG100I	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100I	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100I	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132I	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132I	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132I	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144I	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144I	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144I	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1UWG49ITR[1]	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR50[3]	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR1K[2]	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1TG100I	2112	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-2TG100I	2112	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-3TG100I	2112	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-1MG132I	2112	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-2MG132I	2112	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-3MG132I	2112	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-1TG144I	2112	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-2TG144I	2112	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-3TG144I	2112	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-1BG256I	2112	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-2BG256I	2112	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-3BG256I	2112	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-1FTG256I	2112	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-2FTG256I	2112	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-3FTG256I	2112	1.2 V	–3	Halogen-Free ftBGA	256	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000ZE-1QN84I	4320	1.2 V	–1	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-2QN84I	4320	1.2 V	–2	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-3QN84I	4320	1.2 V	–3	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-1MG132I	4320	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-2MG132I	4320	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-3MG132I	4320	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-1TG144I	4320	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-2TG144I	4320	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-3TG144I	4320	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-1BG256I	4320	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-2BG256I	4320	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-3BG256I	4320	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-1FTG256I	4320	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-2FTG256I	4320	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-3FTG256I	4320	1.2 V	–3	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-1BG332I	4320	1.2 V	–1	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-2BG332I	4320	1.2 V	–2	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-3BG332I	4320	1.2 V	–3	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-1FG484I	4320	1.2 V	–1	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-2FG484I	4320	1.2 V	–2	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-3FG484I	4320	1.2 V	–3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144I	6864	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-2TG144I	6864	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-3TG144I	6864	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-1BG256I	6864	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-2BG256I	6864	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-3BG256I	6864	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-1FTG256I	6864	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-2FTG256I	6864	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-3FTG256I	6864	1.2 V	–3	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-1BG332I	6864	1.2 V	–1	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-2BG332I	6864	1.2 V	–2	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-3BG332I	6864	1.2 V	–3	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-1FG484I	6864	1.2 V	–1	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-2FG484I	6864	1.2 V	–2	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-3FG484I	6864	1.2 V	–3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100IR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100IR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100IR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132IR1[1]	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132IR1[1]	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132IR1[1]	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144IR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144IR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144IR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200ZE-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32I	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	IND
LCMXO2-256HC-5SG32I	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	IND
LCMXO2-256HC-6SG32I	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	IND
LCMXO2-256HC-4SG48I	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	IND
LCMXO2-256HC-5SG48I	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	IND
LCMXO2-256HC-6SG48I	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	IND
LCMXO2-256HC-4UMG64I	256	2.5 V / 3.3 V	–4	Halogen-Free ucBGA	64	IND
LCMXO2-256HC-5UMG64I	256	2.5 V / 3.3 V	–5	Halogen-Free ucBGA	64	IND
LCMXO2-256HC-6UMG64I	256	2.5 V / 3.3 V	–6	Halogen-Free ucBGA	64	IND
LCMXO2-256HC-4TG100I	256	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-256HC-5TG100I	256	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-256HC-6TG100I	256	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-256HC-4MG132I	256	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-256HC-5MG132I	256	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-256HC-6MG132I	256	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48I	640	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	IND
LCMXO2-640HC-5SG48I	640	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	IND
LCMXO2-640HC-6SG48I	640	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	IND
LCMXO2-640HC-4TG100I	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-640HC-5TG100I	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-640HC-6TG100I	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-640HC-4MG132I	640	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-640HC-5MG132I	640	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-640HC-6MG132I	640	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144I	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-640UHC-5TG144I	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-640UHC-6TG144I	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32I	1280	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	IND
LCMXO2-1200HC-5SG32I	1280	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	IND
LCMXO2-1200HC-6SG32I	1280	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	IND
LCMXO2-1200HC-4TG100I	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100I	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100I	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132I	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132I	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132I	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144I	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144I	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144I	1280	2.5 V/ 3.3 V	–6	Halogen-Free TQFP	144	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256I	1280	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-5FTG256I	1280	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-6FTG256I	1280	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100I	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-5TG100I	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-6TG100I	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-4MG132I	2112	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-5MG132I	2112	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-6MG132I	2112	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-4TG144I	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-5TG144I	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-6TG144I	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-4BG256I	2112	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-5BG256I	2112	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-6BG256I	2112	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-4FTG256I	2112	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-5FTG256I	2112	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-6FTG256I	2112	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484I	2112	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-5FG484I	2112	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-6FG484I	2112	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84I	4320	2.5 V / 3.3 V	–4	Halogen-Free QFN	84	IND
LCMXO2-4000HC-5QN84I	4320	2.5 V / 3.3 V	–5	Halogen-Free QFN	84	IND
LCMXO2-4000HC-6QN84I	4320	2.5 V / 3.3 V	–6	Halogen-Free QFN	84	IND
LCMXO2-4000HC-4TG144I	4320	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-5TG144I	4320	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-6TG144I	4320	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-4MG132I	4320	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-5MG132I	4320	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-6MG132I	4320	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-4BG256I	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-5BG256I	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-6BG256I	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-4FTG256I	4320	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-5FTG256I	4320	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-6FTG256I	4320	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-4BG332I	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-5BG332I	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-6BG332I	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-4FG484I	4320	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-5FG484I	4320	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-6FG484I	4320	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144I	6864	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-5TG144I	6864	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-6TG144I	6864	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-4BG256I	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-5BG256I	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-6BG256I	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-4FTG256I	6864	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-5FTG256I	6864	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-6FTG256I	6864	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-4BG332I	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-5BG332I	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-6BG332I	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-4FG400I	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-5FG400I	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-6FG400I	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-4FG484I	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-5FG484I	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-6FG484I	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100IR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100IR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100IR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132IR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132IR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132IR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144IR1[1]	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144IR1[1]	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144IR1[1]	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200HC-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High Performance Industrial Grade Devices Without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100I	2112	1.2 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-5TG100I	2112	1.2 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-6TG100I	2112	1.2 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-4MG132I	2112	1.2 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-5MG132I	2112	1.2 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-6MG132I	2112	1.2 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-4TG144I	2112	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-5TG144I	2112	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-6TG144I	2112	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-4BG256I	2112	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-5BG256I	2112	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-6BG256I	2112	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-4FTG256I	2112	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-5FTG256I	2112	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-6FTG256I	2112	1.2 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484I	2112	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-5FG484I	2112	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-6FG484I	2112	1.2 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4MG132I	4320	1.2 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-5MG132I	4320	1.2 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-6MG132I	4320	1.2 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-4TG144I	4320	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-5TG144I	4320	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-6TG144I	4320	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-4MG184I	4320	1.2 V	–4	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-5MG184I	4320	1.2 V	–5	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-6MG184I	4320	1.2 V	–6	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-4BG256I	4320	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-5BG256I	4320	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-6BG256I	4320	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-4FTG256I	4320	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-5FTG256I	4320	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-6FTG256I	4320	1.2 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-4BG332I	4320	1.2 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-5BG332I	4320	1.2 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-6BG332I	4320	1.2 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-4FG484I	4320	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-5FG484I	4320	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-6FG484I	4320	1.2 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144I	6864	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-5TG144I	6864	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-6TG144I	6864	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-4BG256I	6864	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-5BG256I	6864	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-6BG256I	6864	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-4FTG256I	6864	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-5FTG256I	6864	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-6FTG256I	6864	1.2 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-4BG332I	6864	1.2 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-5BG332I	6864	1.2 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-6BG332I	6864	1.2 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-4FG484I	6864	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-5FG484I	6864	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-6FG484I	6864	1.2 V	–6	Halogen-Free fpBGA	484	IND

R1 Device Specifications

The LCMXO2-1200ZE/HC "R1" devices have the same specifications as their Standard (non-R1) counterparts except as listed below. For more details on the R1 to Standard migration refer to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard Non-R1) Devices.

- The User Flash Memory (UFM) cannot be programmed through the internal WISHBONE interface. It can still be programmed through the JTAG/SPI/I^{2}C ports.
- The on-chip differential input termination resistor value is higher than intended. It is approximately 200Ω as opposed to the intended 100Ω. It is recommended to use external termination resistors for differential inputs. The on-chip termination resistors can be disabled through Lattice design software.
- Soft Error Detection logic may not produce the correct result when it is run for the first time after configuration. To use this feature, discard the result from the first operation. Subsequent operations will produce the correct result.
- Under certain conditions, IIH exceeds data sheet specifications. The following table provides more details:

Condition	Clamp	Pad Rising IIH Max.	Pad Falling IIH Min.	Steady State Pad High IIH	Steady State Pad Low IIL
VPAD > VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD = VCCIO	ON	10 µA	–10 µA	10 µA	10 µA
VPAD = VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD < VCCIO	OFF	10 µA	–10 µA	10 µA	10 µA

- The user SPI interface does not operate correctly in some situations. During master read access and slave write access, the last byte received does not generate the RRDY interrupt.
- In GDDRX2, GDDRX4 and GDDR71 modes, ECLKSYNC may have a glitch in the output under certain conditions, leading to possible loss of synchronization.
- When using the hard I^{2}C IP core, the I^{2}C status registers I2C_1_SR and I2C_2_SR may not update correctly.
- PLL Lock signal will glitch high when coming out of standby. This glitch lasts for about 10 µsec before returning low.
- Dual boot only available on HC devices, requires tying VCC and VCCIO2 to the same 3.3 V or 2.5 V supply.

MachXO2 Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the MachXO2 family are available on the Lattice web site.

- TN1198, Power Estimation and Management for MachXO2 Devices
- TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide
- TN1201, Memory Usage Guide for MachXO2 Devices
- TN1202, MachXO2 sysIO Usage Guide
- TN1203, Implementing High-Speed Interfaces with MachXO2 Devices
- TN1204, MachXO2 Programming and Configuration Usage Guide
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices
- TN1206, MachXO2 SRAM CRC Error Detection Usage Guide
- TN1207, Using TraceID in MachXO2 Devices
- TN1074, PCB Layout Recommendations for BGA Packages
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices
- AN8066, Boundary Scan Testability with Lattice sysIO Capability
- MachXO2 Device Pinout Files
- Thermal Management document
- Lattice design tools

For further information on interface standards, refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, LVDS, DDR, DDR2, LPDDR): www.jedec.org
- PCI: www.pcisig.com

MachXO2 Family Data Sheet Revision History

March 2017 **Data Sheet DS1035**

Date	Version	Section	Change Summary
March 2017	3.3	DC and Switching Characteristics	Updated the Absolute Maximum Ratings section. Added standards.
			Updated the sysIO Recommended Operating Conditions section. Added standards.
			Updated the sysIO Single-Ended DC Electrical Characteristics section. Added standards.
			Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA}. The parameter descriptions were also modified.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA}. The parameter descriptions were also modified.
			Updated the sysCONFIG Port Timing Specifications section. Corrected the t_{INITL} units from ns to µs.
		Pinout Information	Updated the Signal Descriptions section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals.
			Updated the Pinout Information Summary section. Added footnote to MachXO2-1200 32 QFN.
		Ordering Information	Updated the MachXO2 Part Number Description section. Corrected the MG184, BG256, FTG256 package information. Added “(0.8 mm Pitch)” to BG332.
			Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. — Updated LCMXO2-1200ZE-1UWG25ITR50 footnote. — Corrected footnote numbering typo. — Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2-2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s.

Date	Version	Section	Change Summary
May 2016	3.2	All	Moved designation for 84 QFN package information from 'Advanced' to 'Final'.
		Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added ‘Advanced’ 48 QFN package. — Revised footnote 6. — Added footnote 9.
		DC and Switching Characteristics	Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Added footnote 12.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Added footnote 12.
		Pinout Information	Updated the Signal Descriptions section. Added information on GND signal.
			Updated the Pinout Information Summary section. — Added ‘Advanced’ MachXO2-256 48 QFN values. — Added ‘Advanced’ MachXO2-640 48 QFN values. — Added footnote to GND. — Added footnotes 2 and 3.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added ‘Advanced’ SG48 package and revised footnote.
			Updated the Ordering Information section. — Added part numbers for ‘Advanced’ QFN 48 package.
March 2016	3.1	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 32 QFN value for XO2-1200. — Added 84 QFN (7 mm x 7 mm, 0.5 mm) package. — Modified package name to 100-pin TQFP. — Modified package name to 144-pin TQFP. — Added footnote.
		Architecture	Updated the Typical I/O Behavior During Power-up section. Removed reference to TN1202.
		DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications section. Revised $t_{DPPDONE}$ and $t_{DPPINIT}$ Max. values per PCN 03A-16, released March 2016.
		Pinout Information	Updated the Pinout Information Summary section. — Added MachXO2-1200 32 QFN values. — Added ‘Advanced’ MachXO2-4000 84 QFN values.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added ‘Advanced’ QN84 package and footnote.
			Updated the Ordering Information section. — Added part numbers for 1280 LUTs QFN 32 package. — Added part numbers for 4320 LUTs QFN 84 package.
March 2015	3.0	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Changed 64-ball ucBGA dimension.
		Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.

Date	Version	Section	Change Summary
December 2014	2.9	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Removed XO2-4000U data. — Removed 400-ball ftBGA. — Removed 25-ball WLCSP value for XO2-2000U.
		DC and Switching Characteristics	Updated the Recommended Operating Conditions section. Adjusted Max. values for V_{CC} and V_{CCIO}.
			Updated the sysIO Recommended Operating Conditions section. Adjusted Max. values for LVCMOS 3.3, LVTTL, PCI, LVDS33 and LVPECL.
		Pinout Information	Updated the Pinout Information Summary section. Removed MachXO2-4000U.
		Ordering Information	Updated the MachXO2 Part Number Description section. Removed BG400 package.
			Updated the High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
			Updated the High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
November 2014	2.8	Introduction	Updated the Features section. — Revised I/Os under Flexible Logic Architecture. — Revised standby power under Ultra Low Power Devices. — Revise input frequency range under Flexible On-Chip Clocking.
			Updated Table 1-1, MachXO2 Family Selection Guide. — Added XO2-4000U data. — Removed HE and ZE device options for XO2-4000. — Added 400-ball ftBGA.
		Pinout Information	Updated the Pinout Information Summary section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added BG400 package.
			Updated the Ordering Information section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400 part numbers.
October 2014	2.7	Ordering Information	Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Fixed typo in LCMXO2-2000ZE-1UWG49ITR part number package.
		Architecture	Updated the Supported Standards section. Added MIPI information to Table 2-12. Supported Input Standards and Table 2-13. Supported Output Standards.
		DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition.
			Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition.
			Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.
July 2014	2.6	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics[1, 2] section. Updated footnote 4.
			Updated Register-to-Register Performance section. Updated footnote.
		Ordering Information	Updated UW49 package to UWG49 in MachXO2 Part Number Description.
			Updated LCMXO2-2000ZE-1UWG49CTR package in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging.

Date	Version	Section	Change Summary
May 2014	2.5	Architecture	Updated TransFR (Transparent Field Reconfiguration) section. Updated TransFR description for PLL use during background Flash programming.
February 2014	02.4	Introduction	Included the 49 WLCSP package in the MachXO2 Family Selection Guide table.
		Architecture	Added information to Standby Mode and Power Saving Options section.
		Pinout Information	Added the XO2-2000 49 WLCSP in the Pinout Information Summary table.
		Ordering Information	Added UW49 package in MachXO2 Part Number Description.
			Added and LCMXO2-2000ZE-1UWG49CTR in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging section.
			Added and LCMXO2-2000ZE-1UWG49ITR in Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section.
December 2013	02.3	Architecture	Updated information on CLKOS output divider in sysCLOCK Phase Locked Loops (PLLs) section.
		DC and Switching Characteristics	Updated Static Supply Current – ZE Devices table.
			Updated footnote 4 in sysIO Single-Ended DC Electrical Characteristics table; Updated V_{IL} Max. (V) data for LVCMOS 25 and LVCMOS 28.
			Updated V_{OS} test condition in sysIO Differential Electrical Characteristics - LVDS table.
September 2013	02.2	Architecture	Removed I^2C Clock-Stretching feature per PCN #10A-13.
			Removed information on PDPR memory in RAM Mode section.
			Updated Supported Input Standards table.
		DC and Switching Characteristics	Updated Power-On-Reset Voltage Levels table.
June 2013	02.1	Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.
			sysCLOCK Phase Locked Loops (PLLs) section – Added missing cross reference to sysCLOCK PLL Timing table.
		DC and Switching Characteristics	Added slew rate information to footnote 2 of the MachXO2 External Switching Characteristics – HC/HE Devices and the MachXO2 External Switching Characteristics – ZE Devices tables.
			Power-On-Reset Voltage Levels table – Added symbols.

Date	Version	Section	Change Summary
January 2013	02.0	Introduction	Updated the total number IOs to include JTAGENB.
		Architecture	Supported Output Standards table – Added 3.3 V_{CCIO} (Typ.) to LVDS row.
			Changed SRAM CRC Error Detection to Soft Error Detection.
		DC and Switching Characteristics	Power Supply Ramp Rates table – Updated Units column for t_{RAMP} symbol.
			Added new Maximum sysIO Buffer Performance table.
			sysCLOCK PLL Timing table – Updated Min. column values for f_{IN}, f_{OUT}, f_{OUT2} and f_{PFD} parameters. Added t_{SPO} parameter. Updated footnote 6.
			MachXO2 Oscillator Output Frequency table – Updated symbol name for $t_{STABLEOSC.}$
			DC Electrical Characteristics table – Updated conditions for $I_{IL,}$ I_{IH} symbols.
			Corrected parameters tDQVBS and tDQVAS
			Corrected MachXO2 ZE parameters tDVADQ and tDVEDQ
		Pinout Information	Included the MachXO2-4000HE 184 csBGA package.
		Ordering Information	Updated part number.
April 2012	01.9	Architecture	Removed references to TN1200.
		Ordering Information	Updated the Device Status portion of the MachXO2 Part Number Description to include the 50 parts per reel for the WLCSP package.
			Added new part number and footnote 2 for LCMXO2-1200ZE-1UWG25ITR50.
			Updated footnote 1 for LCMXO2-1200ZE-1UWG25ITR.
		Supplemental Information	Removed references to TN1200.
March 2012	01.8	Introduction	Added 32 QFN packaging information to Features bullets and MachXO2 Family Selection Guide table.
		DC and Switching Characteristics	Changed ‘STANDBY’ to ‘USERSTDBY’ in Standby Mode timing diagram.
		Pinout Information	Removed footnote from Pin Information Summary tables.
			Added 32 QFN package to Pin Information Summary table.
		Ordering Information	Updated Part Number Description and Ordering Information tables for 32 QFN package.
			Updated topside mark diagram in the Ordering Information section.

Date	Version	Section	Change Summary
February 2012	01.7	All	Updated document with new corporate logo.
	01.6	—	Data sheet status changed from preliminary to final.
		Introduction	MachXO2 Family Selection Guide table – Removed references to 49-ball WLCSP.
		DC and Switching Characteristics	Updated Flash Download Time table.
			Modified Storage Temperature in the Absolute Maximum Ratings section.
			Updated I_{DK} max in Hot Socket Specifications table.
			Modified Static Supply Current tables for ZE and HC/HE devices.
			Updated Power Supply Ramp Rates table.
			Updated Programming and Erase Supply Current tables.
			Updated data in the External Switching Characteristics table.
			Corrected Absolute Maximum Ratings for Dedicated Input Voltage Applied for LCMXO2 HC.
			DC Electrical Characteristics table – Minor corrections to conditions for I_{IL}, I_{IH}.
		Pinout Information	Removed references to 49-ball WLCSP.
			Signal Descriptions table – Updated description for GND, VCC, and VCCIOx.
			Updated Pin Information Summary table – Number of VCCIOs, GNDs, VCCs, and Total Count of Bonded Pins for MachXO2-256, 640, and 640U and Dual Function I/O for MachXO2-4000 332caBGA.
		Ordering Information	Removed references to 49-ball WLCSP
August 2011	01.5	DC and Switching Characteristics	Updated ESD information.
		Ordering Information	Updated footnote for ordering WLCSP devices.
	01.4	Architecture	Updated information in Clock/Control Distribution Network and sysCLOCK Phase Locked Loops (PLLs).
		DC and Switching Characteristics	Updated I_{IL} and I_{IH} conditions in the DC Electrical Characteristics table.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Updated Pin Information Summary table: Dual Function I/O, DQS Groups Bank 1, Total General Purpose Single-Ended I/O, Differential I/O Per Bank, Total Count of Bonded Pins, Gearboxes. Added column of data for MachXO2-2000 49 WLCSP.
		Ordering Information	Updated R1 Device Specifications text section with information on migration from MachXO2-1200-R1 to Standard (non-R1) devices.
			Corrected Supply Voltage typo for part numbers: LCMX02-2000UHE-4FG484I, LCMX02-2000UHE-5FG484I, LCMX02-2000UHE-6FG484I.
			Added footnote for WLCSP package parts.
		Supplemental Information	Removed reference to Stand-alone Power Calculator for MachXO2 Devices. Added reference to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices.

Date	Version	Section	Change Summary
May 2011	01.3	Multiple	Replaced “SED” with “SRAM CRC Error Detection” throughout the document.
		DC and Switching Characteristics	Added footnote 1 to Program Erase Specifications table.
		Pinout Information	Updated Pin Information Summary tables.
			Signal name SO/SISPISO changed to SO/SPISO in the Signal Descriptions table.
April 2011	01.2	—	Data sheet status changed from Advance to Preliminary.
		Introduction	Updated MachXO2 Family Selection Guide table.
		Architecture	Updated Supported Input Standards table.
			Updated sysMEM Memory Primitives diagram.
			Added differential SSTL and HSTL IO standards.
		DC and Switching Characteristics	Updates following parameters: POR voltage levels, DC electrical characteristics, static supply current for ZE/HE/HC devices, static power consumption contribution of different components – ZE devices, programming and erase Flash supply current.
			Added VREF specifications to sysIO recommended operating conditions.
			Updating timing information based on characterization.
			Added differential SSTL and HSTL IO standards.
		Ordering Information	Added Ordering Part Numbers for R1 devices, and devices in WLCSP packages.
			Added R1 device specifications.
January 2011	01.1	All	Included ultra-high I/O devices.
		DC and Switching Characteristics	Recommended Operating Conditions table – Added footnote 3.
			DC Electrical Characteristics table – Updated data for I_{IL}, I_{IH}. V_{HYST} typical values updated.
			Generic DDRX2 Outputs with Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB}.
			Generic DDRX4 Outputs with Clock and Data Aligned at Pin (GDDRX4_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB}.
			Power-On-Reset Voltage Levels table - clarified note 3.
			Clarified VCCIO related recommended operating conditions specifications.
			Added power supply ramp rate requirements.
			Added Power Supply Ramp Rates table.
			Updated Programming/Erase Specifications table.
			Removed references to V_{CCP}.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Removed references to V_{CCP}.
November 2010	01.0	—	Initial release.